Interfering DC Component, Suppression and Influence to Digital Signal Processing

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Abstract. *The article concentrates on effects of a digitized audio signal DC component on a typical A/D converter and its influence on further signal processing. This article analyses reasons of the interfering DC component emergence in the A/D converter. Results of the measurement made on Analog Devices converter are presented. The DC component can adversely affect a series of signal processing algorithms such as algorithms for maintaining stable level of signal (e.g. leveler algorithm). The article examines the possibility of a DC component removal by digital filtering. Attention is focused on the choice of a suitable filter type and its parameters in order to avoid any destruction of a transmitted signal, e.g. due to poor group delay characteristic, or by suppressing low frequencies in the filter.*

Keywords

DC component, A/D converter, audio digital signal processing, DSP, digital filtering, FIR, IIR.

1. Introduction

In many cases we are processing audio signal from the analog signal sources in the DSP (Digital Signal Processor). Signal then must be converted into the digital domain. This is done in a A/D converter. The input of the converter is often linked to the previous stage over an RC circuit. Such a circuit suppresses the DC component on the input of the A/D converter completely. It means the code obtained from the output of the A/D converter would not therefore also contain any encoded DC component. The null input signal should correspond to the code "digital zero." In many cases, however, it is not true. Inaccuracy in the implementation of the A/D converter usually causes some offset. In consequence the null input signal corresponds to the non-zero output code. As a result, a number of subsequent signal processing algorithms may not work properly because they can be influenced by the presence of the encoded additional DC component.

2. A/D Conversion and DC Component

Construction of several A/D converters from individual manufacturers is different. Despite the high linearity, which is typical for converters of recent generation, the problem with an encoded DC component persists in almost all audio A/D converters. The input of the converter must be intrinsically very carefully set up to the reference level, which corresponds to zero code on the output of the digital converter. The converter is typically equipped with a voltage reference circuit, usually in the mid-supply voltage. This reference voltage is made by a calibrated divider directly on the chip of the A/D converter. In view of this reference voltage A/D conversion is executed. Signals with a higher voltage than the voltage reference are expressed as a positive value. Similarly signals which are lower than the reference voltage are expressed as a negative value. Null input signal should therefore conform to the "digital zero" on the output code of the A/D converter in ideal case.

Accuracy of the reference voltage is affected by the proper calibration of the resistor divider on the chip and by DC drift of the on-chip input amplifiers. For example, if the A/D converter works with a 20-bit resolution, the input dynamic range is more than 120 dB. However such DC accuracy is virtually impossible to achieve for conventional monolithic integrated circuits. Therefore, the output code of the A/D converter typically carries some DC component, even in the case of null input signal. This DC component in addition may vary with temperature, and even with the A/D converter analog input load. An example of the signal with 10 mV DC component is in Fig. 1. The dependence of DC component on the amplitude of the input signal for the Analog Devices AD 1836 converter device (24-bits high-end audio, more in [1]) is in Fig. 2 (for harmonic signal of 1 kHz frequency). The value of DC component is expressed in dB relative to the full loading of the A/D converter (0 dBFS).

The existence of encoded DC component can affect a number of signal processing algorithms, often in a quite unexpected way. For example it affects the algorithm which is to detect a signal to fall close to zero. Such an algorithm compares the current signal value with a threshold. However if the DC component alone exceeds the value of this threshold, the algorithm completely fails. Another case may be algorithms for strong dynamic audio signal compression. As the DC component is added to all signal values, such algorithms give clearly bad results especially if processing of signals with a low level, which is close to the DC component level, or even less. Then, it is very important to remove the DC component at the beginning of the entire chain of the digital signal processing.

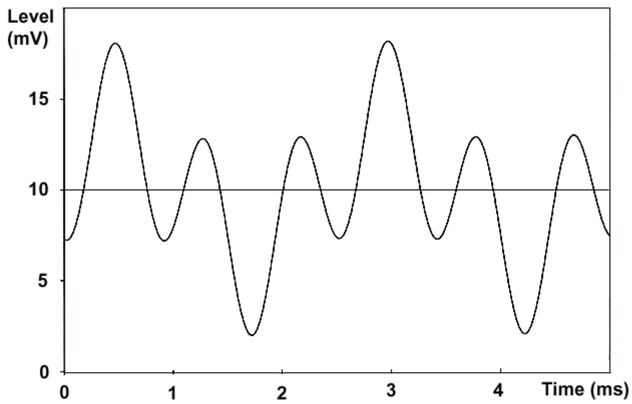

Fig. 1. Example of a signal with 10 mV DC component.

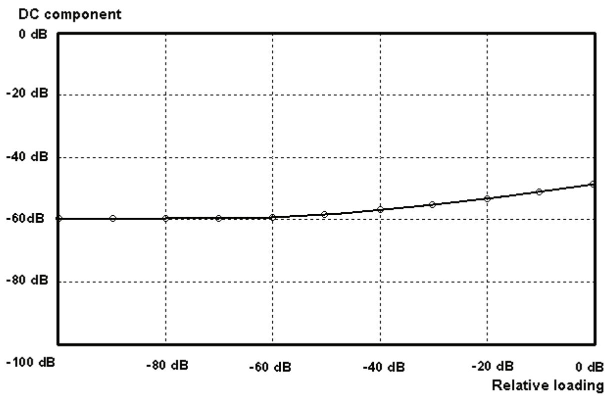

Fig. 2. DC component as a function of relative loading (AD1836).

3. Suppression of the DC Component

The DC component can be suppressed simply by digital filtering. Digital filter has to be a high-pass class. Such filter removes DC component completely. An action of every filter however influences the transmitted signal. The level of this influence depends on the characteristics of the filter and characteristics of the transmitted signals. In order to minimize the influence on the transmitted signal, it is appropriate to use a high-pass class filter with a very low cutoff frequency. The exact value of the optimal cutoff frequency depends on the nature of the processed signal. In case of the audio signal processing, the optimal cutoff frequency will lie in the range from 0.2 Hz to 2 Hz depending on our requirements (e.g. the type of further processing). There is no specific requirement for the order of the filter. The high-pass class filter of the first order is enough. DC component is a signal with zero frequency. For such a signal an infinite attenuation is secured by the high-pass class filter based on any filter type regardless of the cutoff frequency and the order of the filter.

A digital FIR (Finite Impulse Response [2], [3]) filter can be designed with flat group delay characteristic. It can be a noticeable advantage in certain cases. However the disadvantage is an extremely high demand on computing power of the DSP in case of the low cutoff frequency. For sampling rate 48 kHz and 0.2 Hz cutoff frequency, the number of FIR filter taps would be approximately 10^5. FIR filter design is not suitable in this case.

A digital IIR (Infinite Impulse Response [4]) filter is considerably less demanding on the DSP computing power compared with the FIR filter in the case of the very low cutoff frequency. The IIR filter design with the very low cutoff frequency requires high accuracy of the calculations. However this is usually not a major problem, because the most frequently used floating point DSP circuits provide the necessary accuracy.

Simulated amplitude characteristic, phase characteristic and the group delay characteristic of the IIR filter design are shown in Fig. 3 (Butterworth type first order with a cutoff frequency 0.2 Hz). The group delay and phase characteristics are balanced approximately from the frequency 10 Hz above. Therefore it is possible to consider such a filter as virtually perfect for audio signal processing (processing of a signal in frequency range 20 Hz to 20 kHz). Inaccuracies in the transmitted signal are only represented by a very small linear distortion. The extent of this linear distortion is so small that it can be tolerated in virtually all applications where we work with audio signals. If such a digital filter is located as the first block in the digital signal processing chain, it suppresses the DC component of the input signal completely. Other characteristics of the transmitted signal are not influenced in an appreciable way.

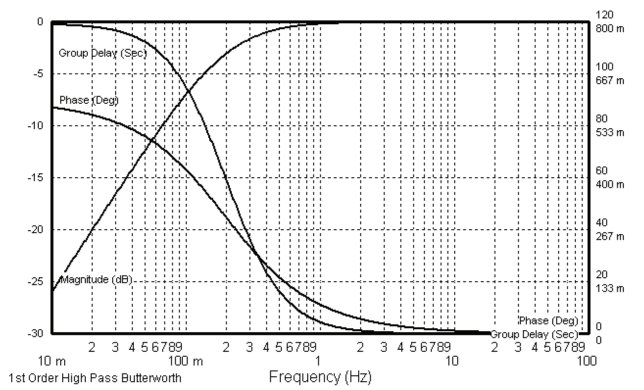

Fig. 3. Characteristics of IIR filter, cutoff frequency 0.2 Hz.

4. Conclusion

The described simple method of suppressing the DC component of a digitized signal has been successfully used in a development of broadcast audio processors and stereophonic encoders. The DC component which can affect the activity of many algorithms has been successfully suppressed without remarkable influence to the transmitted audio signal. The code for DC component suppression was tested on ADSP 21161 Analog Devices DSP device [5] with AD 1836 converter [1], [6]. The measured results for the leveler algorithm (the algorithm for the input signal level stabilization) with a range of 60 dB are in Fig. 4 and Fig. 5. Fig. 4 shows the characteristic of this leveler if suppression of the DC component of the signal is not used. We can see that the activity of the leveler is influenced mainly for the low level signals (for example -60 dBFS input signal is influenced by -6 dB on the leveler output). Fig. 5 shows the characteristic of the leveler if suppression is used. The characteristic in Fig. 5 also corresponds exactly to the theoretical ideal characteristic of such leveler.

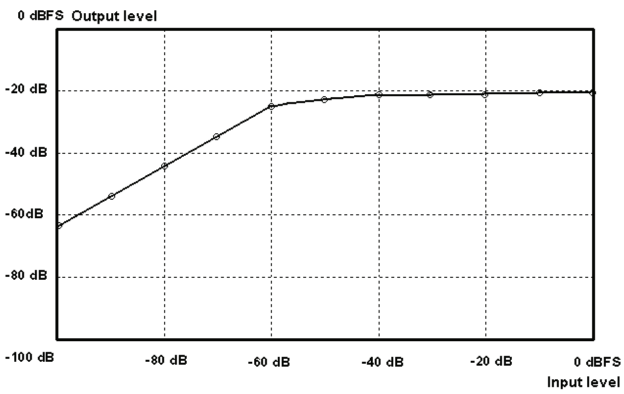

Fig. 4. Leveler characteristic affected by DC component.

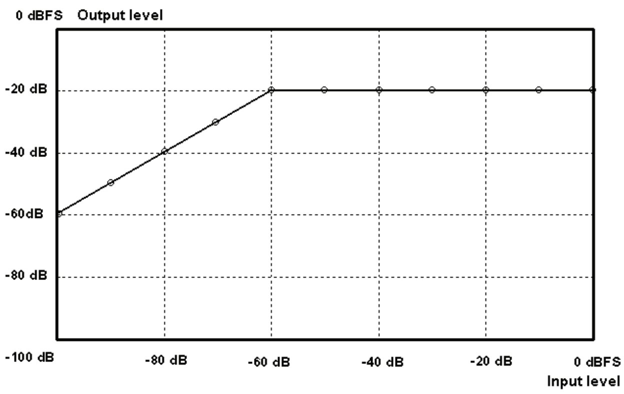

Fig. 5. Leveler characteristic: DC component suppressed.

In summary, the described method for suppression of the DC component creates the conditions for optimal function of audio signal processing algorithms. Therefore, its application is recommend where the digital audio signal comes directly from the A/D converter. The method can be applied before audio signal processing everywhere, where we're unsure that suppression of the DC component in the incoming digital signal is perfect.

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About Author...

Pavel STRAŇÁK was born in Prague, Czech Republic, in 1963. He graduated from the Faculty of Electrical Engineering, Czech Technical University in Prague in 1986 (M.Sc.). He was employed in the Czech Radio, the Czech national broadcaster where he worked on the development of digital audio systems. In 1993 he founded a company which develops and manufactures radio broadcasting equipment. Currently he is engaged in the research and development in the field of digital signal processing in his own company, Phobos Engineering s.r.o. He has published a number of articles on digital signal processing for radio broadcasting. He regularly presents lectures at annual conferences of the Czech section of AES. Currently he is an external postgraduate student (Ph.D.) at the Dept. of Radio Electronics, Czech Technical University in Prague.