Characterization of Nonlinear Integrated Capacitors

Tomáš SUTORÝ, Zdeněk KOLKA

Dept. of Radio Electronics, Brno University of Technology, Purkyňova 118, 612 00 Brno, Czech Republic

tomas.sutory@onsemi.com, kolka@feec.vutbr.cz

Abstract. *The paper deals with a modified CBCM (Charge-Based Capacitance Measurements) method for nonlinear capacitance characterization. The method is characterized by high resolution although it is based on equipment found in any average laboratory. CBCM was originally developed for linear interconnect measurements. The proposed modification uses two DC swept sources to measure the whole nonlinear Q-v characteristic in both polarities without the necessity to switch the measured object. A test-chip implementing the method was designed and manufactured in the 0.35μm CMOS process. Verification against known capacitances proved the correctness and accuracy of the method. It was successfully used for MOSCAPs characterization.*

Keywords

Charge-based capacitance measurements, test structures, MOS capacitors, integrated circuits.

1. Introduction

The usage of off-chip measuring instruments in the femtofarad range is limited due to the parasitic capacitances of probes, which can be in orders of magnitude higher than the capacitances being measured. Thus a part of the measuring circuitry should be integrated with the object being measured.

There are several methods for measuring small on-chip capacitances in the femtofarad range. The method of on-chip capacitive divider formed by the measured object and a reference capacitor [1], [2] is sensitive to parasitic capacitances, manufacturing variance and leakage currents of sensing circuitry. The method of [3] is based on measuring the current flowing through a measured capacitor driven by alternating voltage. The method of ring oscillator is suitable for linear capacitors [4]. In addition, the test structure requires a larger chip area in comparison with other methods.

The CBCM (Charge-Based Capacitance Measurements) method has found extensive use in on-chip capacitor measurements in the femtofarad range [5]. The method is characterized by high resolution although it is based on equipment found in any average laboratory. CBCM was originally developed for linear interconnect capacitance measurements with sub-femtofarad resolution [5]. A charge injection "error-free" variant for linear capacitors has been developed [6], [7]. The method is error-free only for the linear device under test and does not guarantee a large enough voltage swing across the measured device.

This paper deals with a modification of the CBCM method that will enable nonlinear capacitance characterization. Section 2 describes the basic principle, Section 3 deals with design constraints and accuracy, and Section 4 describes a test-chip manufactured in the 0.35μm CMOS process for the verification of the method.

2. Charge-Based Capacitance Measurements

2.1 Basic Method

Fig. 1 shows the principle of the classical version of CBCM [5]. The test structure consists of a pair of NMOS and PMOS transistors connected in a pseudo-inverter configuration. The structure on the left is used as reference. It is identical to the one on the right in every manner except that it does not include the target capacitance C_x to be characterized.

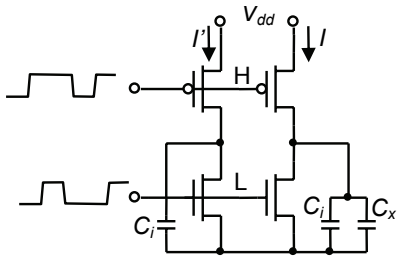

Fig. 1. Basic version of CBCM method.

The left and right structures are both driven by two non-overlapping signals to ensure that only one of the two transistors on either the left or the right side is conducting current at any given time. When the PMOS transistor turns on, it will draw charge Q from V_{dd} to charge up the capacitor under test. This amount of charge will subsequently be discharged through the NMOS transistor into ground. An ammeter can be placed at the source of the PMOS (or, alternatively, at the source of the NMOS) to measure this

charging current. The actual waveform of this current is not important - only its DC component needs to be measured [5]. The difference between the two DC current values is used to extract the measured target capacitance C_x given in the idealized case by

$$I - I' = (Q - Q')\, f = V_{dd}\, C_x f \ . \tag{1}$$

where $Q - Q' = V_{dd}\,((C_i + C_x) - C_i)$, f is the switching frequency. The parasitic capacitance C_i and DC currents I and I' are shown in Fig. 1. The resolution of CBCM is limited by the parasitic properties of switches and leakage currents [5].

2.2 Modified Method

The basic CBCM method is normally used to characterize linear capacitances. Nonlinear capacitors are characterized by the C-v or Q-v characteristics. Although the standard CBCM allows V_{dd} sweeping, for low voltages the measured current decreases and the method resolution becomes unacceptable. This is especially critical for minimum-feature transistors, where it is desirable to use high V_{dd} to obtain a reasonable current.

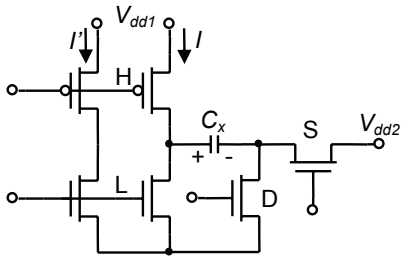

Fig. 2. Modified CBCM method.

The proposed modification of the CBCM method is applicable to the measurement of floating devices. Two DC sources are used to measure the whole nonlinear characteristic in both polarities without the necessity to switch the device under test (C_x). One source is swept while the other is kept constant, and vice versa. For each point of the characteristic, a minimum voltage amplitude and thereby a minimum DC current are guaranteed. The principal schematic of the proposed test structure is shown in Fig. 2.

The basic principle of CBCM with the main (right) and compensation (left) switches as shown in Fig. 1 is the same also for the modified method. The DC source V_{dd} was renamed V_{dd1}. The main difference is in the negative terminal of the measured object. The ground connection is replaced by the switch D and the node can be additionally connected to another DC source V_{dd2} by the bidirectional switch S.

One period of controlling signals can be divided into four non-overlapping phases, see Fig. 3. During phase 1 the measured capacitor is charged to a negative voltage (seen on its terminals) from the source V_{dd2} through the switches L and S. During phase 2, L is switched off and S remains switched on. Activating the switch H results in charging the capacitor to the voltage V_{dd1}-V_{dd2}. The charge drawn is counted by the ammeter. The voltage changes for V_{dd1}. During phase 3, S is switched off and the capacitor is charged to V_{dd1} through the switch D. The voltage changes for V_{dd2} and the charge drawn is again counted by the ammeter. During the last phase C_x is discharged.

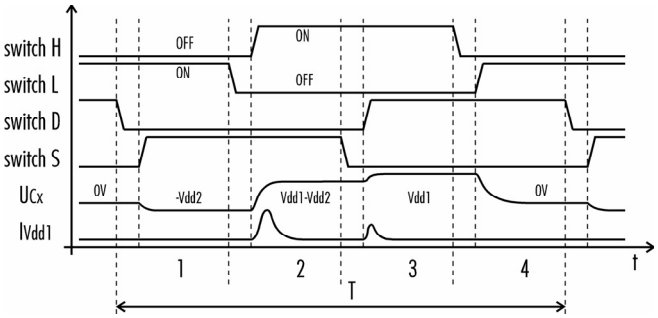

Fig. 3. Waveforms of signals in modified CBCM method.

The capacitor voltage varies during one period from $-V_{dd2}$ to V_{dd1} and the charge variation can be determined from the measured current as

$$\Delta Q(V_{dd2}, V_{dd1}) = \frac{I - I'}{f} = \int_{-Vdd2}^{Vdd1} C_x dv \ . \tag{2}$$

Let us start the reconstruction of Q-v characteristic for negative voltages across C_x. The source V_{dd1} is held constant while the source V_{dd2} is swept. The capacitor charge is then

$$Q(-V_{dd2}) = -\int_{-Vdd2}^{0} C_x dv = -\int_{-Vdd2}^{Vdd1} C_x dv + \int_{0}^{Vdd1} C_x dv \ . \tag{3}$$

Combining (2) and (3) we obtain finally

$$Q(-V_{dd2})_{Vdd1=const} = \Delta Q(0, V_{dd1}) - \Delta Q(V_{dd2}, V_{dd1}), \tag{4}$$

and similarly for the positive voltage

$$Q(V_{dd1})_{Vdd2=const} = \Delta Q(V_{dd2}, V_{dd1}) - \Delta Q(V_{dd2}, 0) \ . \tag{5}$$

Thus the device can be characterized in both polarities. The dynamic capacitance $C_x(v)$ is then

$$C_x(v) = dQ(v)/dv \ . \tag{6}$$

3. Design Constraints

3.1 Switch On-Resistance

It is obvious from (1) that the currents and thus the resolution of the method can be increased by means of increasing V_{dd} and the frequency. V_{dd} is limited by the technology and the maximum frequency is determined by the on-resistance of switching transistors. The capacitance under test must be "completely" charged and discharged during one period. The switching transients can be speeded-up by increasing the switching transistor width, i.e. by decreasing their on-resistance. This can be done

only in a limited range because enlarging the transistor increases the gate capacitances and thus increases the undesirable charge injection from driver circuitry to the device under test.

Fig. 4 shows the steady state voltage across the measured capacitor, where t_{onH} and t_{onL} are the on-periods of high-side and low-side switches, respectively, Fig. 1.

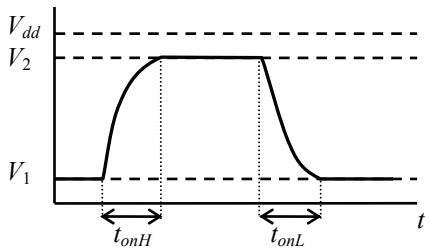

Fig. 4. Steady state of switching process.

Assuming linear switches the steady-state voltage swing across the loading capacitor C_L is

$$V_2 - V_1 = V_{dd}\frac{(1-k_L)(1-k_H)}{1-k_L\,k_H} \tag{7}$$

where $k_L = \exp(-t_{onL}/R_{onL}C_L)$ and $k_H = \exp(-t_{onH}/R_{onH}C_L)$. The symbols R_{onH} and R_{onL} denote the on-resistance of high-side and low-side switches, respectively.

Let us assume, for simplicity, a symmetrical case

$$k_L = k_H = k = \exp(-t_{on}/R_{on}C_L)\ . \tag{8}$$

As the measured current I is

$$I = fC_L(V_2 - V_1) \tag{9}$$

the calculated apparent capacitance C'_L will be

$$C'_L = \frac{I}{fV_{dd}} = C_L\frac{1-k}{1+k}\ . \tag{10}$$

Considering (1), the measurement error for the structure in Fig. 1 caused by non-ideal charging and discharging is

$$\delta_c = \frac{\left[(C_x + C_i)' - C_i'\right] - C_x}{C_x} = (K_x - 1) + \frac{C_i}{C_x}(K_x - K_i) \tag{11}$$

where

$$K_x = \frac{1-k_x}{1+k_x},\ K_i = \frac{1-k_i}{1+k_i} \tag{12a,b}$$

and $k_x = \exp(-t_{on}/R_{on}(C_x+C_i))$, $k_i = \exp(-t_{on}/R_{on}C_i)$.

Fig. 5 shows the relative error (11) as a function of $t_{on}/R_{on}(C_x+C_i)$ for different values of C_i/C_x. To obtain an accuracy better than 1% the ratio t_{on}/τ should be greater than 6 for $C_i/C_x < 1$.

For $-\delta_c < 10\%$ the denominator of (12) is approximately equal to 1, and (11) can be simplified to

$$\delta_c \approx -2k_x\left[1 + \frac{C_i}{C_x}\left(1 - \sqrt[C_i/C_x]{k_x}\right)\right]. \tag{13}$$

The last term in (13) quickly vanishes for $C_i/C_x < 1$ and we finally obtain

$$\delta_c \approx -2\exp(-t_{on}/R_{on}(C_i + C_x))\left[1 + C_i/C_x\right]. \tag{14}$$

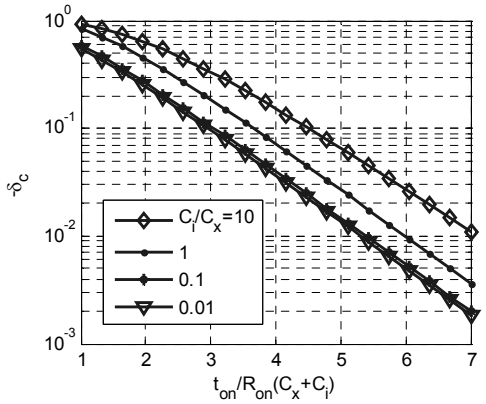

Fig. 5. The effect of nonideal charging and discharging.

3.2 Charge Injection

Another source of error is the parasitic charge injection from driver circuitry to the device under test [8]. Fig. 6 shows schematically the waveforms of switching transients valid for both the left and the right structures in the basic configuration from Fig. 1.

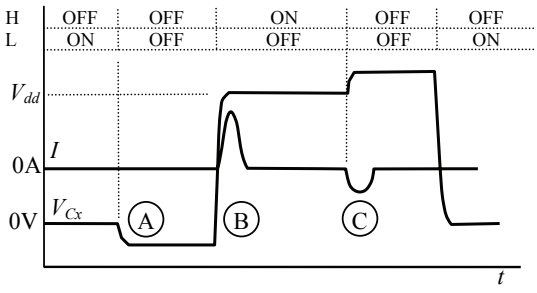

Fig. 6. Switching transients (not to scale).

The undesirable charge injection takes effect both for low-side (L) and high-side (H) switches. At the start of switching cycle, V_{Cx} is zero. The charge injection while switching off the L switch causes V_{Cx} to be negative. The total voltage swing of C_x is then greater than V_{dd}. Another parasitic injection occurs when switching off of H switch, causing a spike on I or I'.

Let us consider the single pseudoinverter from Fig. 1 loaded by a capacitor C_L representing either C_i or C_x+C_i. The charge drawn from the V_{dd} source during one period is

$$Q_{dd}(C_L) = Q_A(C_L) + Q_B(C_L) + Q_C(C_L) \tag{15}$$

where Q_A, Q_B, and Q_C are the contributions for transients A through C, Fig. 6. Since Q_{dd} is a nonlinear function of C_L, the parasitics of the left and the right structures cannot compensate as in (1) even in the case of perfect matching

$$Q - Q' = Q_{dd}(C_x + C_i) - Q_{dd}(C_i) \neq V_{dd}\,C_x\ . \tag{16}$$

This represents the systematic error of CBCM, which is both process- and matching-sensitive.

The approximate analysis of charge injection is based on a simple lumped switching model introduced in [9]. The model is valid if the gate voltage drops much more slowly than the intrinsic carrier transmit time in the transistor ($\tau_C = R_{on}C_{ox}/4$), which is in the order of picoseconds for submicron transistors.

The transistor is characterized by the threshold voltage V_T, the current factor $\beta = \mu C_{ox1} W_{eff}/L_{eff}$ and by the overlap capacitances C_{GDO} and C_{GSO}. The symbol μ represents the carrier mobility and C_{ox1} is the unity gate-oxide capacitance.

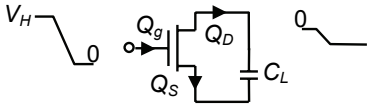

Fig. 7. Model for transients A and C.

The undesirable charge injections A and C occur during the switching off process. For transient times much larger than τ_C, the channel charge is initially split equally between the source and the drain. The redistribution of charge from the drain to the source is determined by their voltage difference and time constants [10].

The initial capacitor voltage is zero. The capacitor voltage will be negative after the transient but small enough not to cause a significant current through the drain-bulk junction, Fig. 7. If the gate voltage is a ramp function which begins to fall at time 0 from the high value V_H toward 0 at a falling rate U [V/s], the charge injected into the drain terminal can be expressed in a closed form as [9]

$$Q_D(C_L) = -\sqrt{\frac{\pi U}{2\beta}} \frac{C_L C_{GD}}{\sqrt{C_L + C_{GD}}} \operatorname{erf}\left(\frac{(V_H - V_T)\sqrt{\beta}}{\sqrt{2U(C_L + C_{GD})}} \right) - C_{GDO} V_T \quad (17)$$

where $C_{ox} = C_{ox1} W_{eff} L_{eff}$, $C_{GD} = C_{GDO} + C_{ox}/2$.

Using the charge-conservation principle, the charge injected into the source terminal will be

$$Q_S(C_L) = -(V_H - V_T) C_{ox} - (C_{GDO} + C_{GSO}) V_H - Q_D(C_L) . \quad (18)$$

The parasitic charges from (15) are then

$$Q_A(C_L) = -Q_D^N(C_L) \ , \ Q_C(C_L) = Q_S^P(C_L) \quad (19a,b)$$

where Q_D^N and Q_S^P are determined from (17) and (18) using the NMOS (A) and PMOS (C) transistor parameters.

Fig. 8 represents the equivalent circuit for transient B when H is switched on. The capacitor is charged from the initial voltage 0 to V_{dd} (the negative initial capacitor voltage has been counted in Q_A).

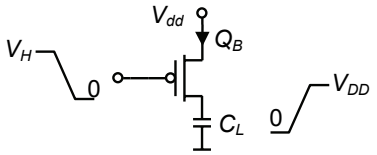

Fig. 8. Equivalent circuit for transient B.

Using the charge-conservation principle, the charge drawn from the V_{dd} source will be simply

$$Q_B(C_L) = C_L V_{dd} + C_{GSO} V_H + C_{GDO}(V_H + V_{dd}) + C_{ox}(V_{dd} - V_T) . \quad (20)$$

In the case of ideal matching, Q_B can be compensated as it depends linearly on C_L.

The injection-induced error is then

$$\delta_i = \frac{C_{calc} - C_x}{C_x} = \frac{Q_{dd}(C_x + C_i) - Q_{dd}(C_i)}{C_x V_{dd}} - 1 \quad (21)$$

where C_{calc} is calculated using (1).

3.3 Switch Dimensioning

The DC current I in Fig. 1 is given as

$$I = V_{dd}(C_x + C_i) f \ . \quad (22)$$

To provide a measurable value I_m of (22) during the characterization of different capacitors it is desirable to keep the product $(C_x + C_i)f$ constant, i.e. to adjust the frequency according to the measured capacitance. As t_{on} is a fixed fraction of one period, the error δ_c (14) can be controlled by the choice of the switch on-resistance

$$R_{on} = K_R \frac{L_{eff}}{W_{eff}} \quad (23)$$

where K_R depends on transistor parameters and gate voltage. As δ_c is proportional to R_{on} the first design constraint can be written as

$$\frac{L_{eff}}{W_{eff}} < C_1 \quad (24)$$

where C_1 depends on δ_c, V_{dd}, I_m and technology.

The charge injection error (21) is proportional to C_{ox}/C_x and does not depend on frequency. It gives the second constraint

$$L_{eff} W_{eff} < C_2 \quad (25)$$

where C_2 depends on δ_i, V_{dd}, C_x and technology.

Fig. 9 shows the design space for dimensioning the switch transistors.

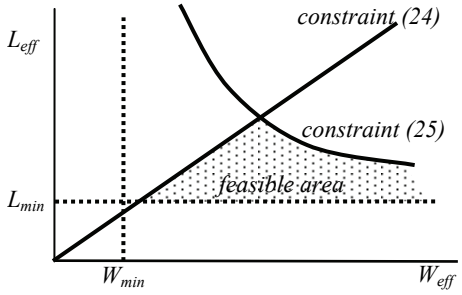

Fig. 9. Design space for switches.

4. Test Chip

The modified CBCM method was implemented in a test-chip to verify its functionality and to characterize nonlinear MOS-gate capacitors and compensation structures. The chip was manufactured in the AMIS I3T80 0.35 μm process.

The test-chip consists of 64 test-cells, whose principal schematic is shown in Fig. 2. Each cell is connected to a device under test (MOS capacitor, metal-metal capacitor or external device). The block diagram of the whole chip is shown in Fig. 10.

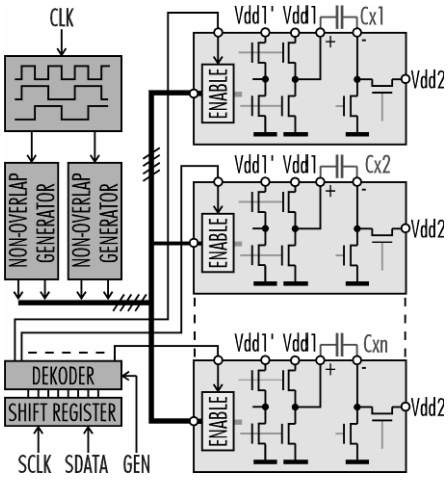

Fig. 10. Block diagram of test-chip.

The supply terminals of all test-cells are connected together and led out from the chip to pads *Vdd1*, *Vdd1'* and *Vdd2*. Fig. 11 shows details of the power supply and biasing of the test-cells. To allow the measurement of only one capacitor, all test-cells have an enabling input. The *Vdd1*, *Vdd1'* and *Vdd2* pins are powered from swept power supplies according to the modified method principle. A sensitive ammeter *A* measures the currents *Idd1* or *Idd1'* according to the position of switch *SW*.

Since the power supply voltages vary from 0 to 3.3 V, the correct driving voltages for MOSFET switches *H*, *L*, *D* and *S* are obtained using level-shifters *LS* supplied from constant-voltage sources relative to *Vdd1* and *Vdd2*. The control signals for switches are generated in a small digital unit supplied from *VDD*.

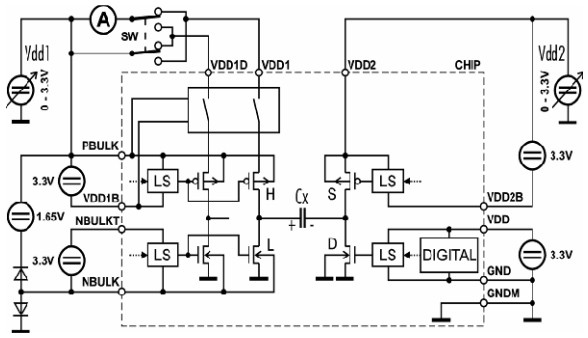

Fig. 11. Schematic diagram of test-chip power supply.

The test-cell topology is universal. It is just the switching sequence generated in the digital unit that determines the actual measuring method. Besides the modified CBCM it is possible to generate sequences for parasitic capacitance measurement [6], [7], classical CBCM and CBCM with a floating capacitance. These additional methods were implemented for verification purposes and as a backup solution.

The chip was manufactured in the AMIS I3T80 0.35μm technology. Dies were assembled in a dual in-line ceramic prototype package with 40 pads, Fig. 12. The package was selected for easy plugging-in to the bench-board through the zero insert-force socket and for the possibility to probe the chip easily for potential debug purposes.

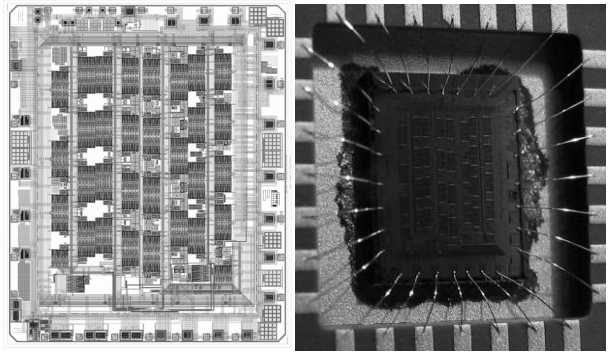

Fig. 12. Top layout and die photograph of test-chip.

One test-cell was dedicated to measuring the external devices. Tab. 1 shows the results for three capacitors, whose capacitance was verified by an LCR meter.

C_{nom} [pF]	C_{RLC} [pF]	$C_{M\text{-}CBCM}$ [pF]
100 pF	99.7	98.96
22 pF	22.0	22.17
10 pF	9.93	10.03

Tab. 1. External capacitor measurement.

The IC pad capacity is about 5 pF, i.e. 50% of the smallest capacitor. Nevertheless, this was compensated by the compensating structure. The clock frequency depends on the capacitance measured, i.e. on switching transients duration. For values from Tab. 1 it was from 2 kHz to 4 kHz.

Integrated linear metal-metal capacitors were used to verify the method linearity for smaller capacitances. The test structures were prepared as 1, 4, 10, and 20 unit capacitors. Although the capacitors are subject to process variations, Tab. 2 shows a very good agreement between the expected and the actually measured values. The values of C_{mon} were determined by statistical fit to linear equation $C_{nom}=aN+b$, where N is the number of units.

Units	1	4	10	20
C_{nom} [pF]	0.9857	3.923	9.797	19.58
C_{CBCM}[pF]	0.9840	3.923	9.799	19.58
error [%]	-0.17	<0.1	<0.1	<0.1

Tab. 2. Metal-metal capacitor measurement.

The main purpose of developing the method was to characterize nonlinear MOS gate capacitors. Such capacitors provide a higher specific capacitance per unit area and do not require additional masks, but the nonlinearity must be carefully compensated. Fig. 13 shows the *C-v* characteristic measured for 1µm x 1µm NMOS transistor. The clock generator frequency was set to 10 MHz.

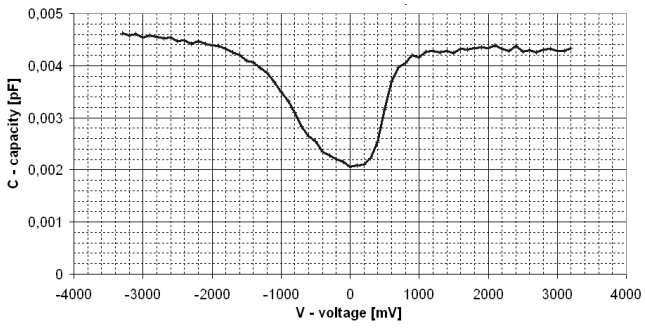

Fig. 13. Nonlinear MOS gate capacitance.

5. Conclusions

A modification of the CBCM method for nonlinear capacitance characterization was developed. Just two DC sources are used to measure the whole nonlinear characteristic in both polarities without the necessity to switch the measured object. A test-chip implementing the method was designed and manufactured in the 0.35µm CMOS process. Verification against known capacitances proved the method to be correct. It was successfully used for MOSCAPs characterization in the full operating range.

Acknowledgements

The research described in the paper was financially supported by the Czech Grant Agency under grant No. 102/08/0784 and by the research program MSM0021630513.

References

[1] KORTEKAAS, C. On-chip quasi-static floating-gate capacitance measurement method. In *Proceedings of the IEEE International Conference on Microelectronic Test Structures*. San Diego (USA), 1990, vol. 3, p. 109-113.

[2] LORIVAL, R., NOUET, P. A test chip for MOS transistor capacitance characterization. In *Proceedings of the IEEE Int. Conference on Microelectronic Test Structure*. Nara (Japan), 1995, vol. 8, p.139-144.

[3] SONG, H., DONS, E., SUN, X.Q., FARMER, K. R. Leakage compensated charge method for determining static C-V characteristics of ultra-thin MOS capacitors. In *Proc. of the NIST Int. Conference on Characterization and Metrology for ULSI Technology*. Gaithersburg (USA), 1998, p. 231-234.

[4] OHKAWA, S., AOKI, M., MASUDA, H. Analysis and characterization of device variations in an LSI chip using an integrated device matrix array. *IEEE Transactions on Semiconductor Manufacturing*, 2004, vol. 17, no. 2, p. 155 – 165.

[5] CHEN, J., SYLVESTER, D., HU, C. An on-chip, interconnect capacitance characterization cethod with sub-femto-farad resolution. *IEEE Trans. on Semiconductor Manufacturing*, 1998, vol. 11, no. 2, p. 204-210.

[6] CHANG, Y. W., CHANG, H. W., HSIEH, C. H., LAI, H. C., LU, T. C., TING, W., KU, J., LU, C. Y. A novel simple CBCM method free from charge injection-induced errors. *IEEE Electron Device Letters*, 2004, vol. 25, no 5, p. 262-264.

[7] CHANG, Y. W., CHANG, H. W., LU, T. C., KING, Y. C., TING, W., KU, J., LU, C. Y. Charge-based capacitance measurement for bias-dependent capacitance. *IEEE Electron Device Letters*, 2006, vol. 27, no 5, p. 390-392.

[8] VENDRAME, L., BORTESI, L., BOGLIOLO, A. Accuracy assessment and improvement of on-chip charge-based capacitance measurements. In *Proceedings of the 7th IEEE SPI Workshop*, Siena (Italy), 2003.

[9] SHEU, B. J., HU, C. M. Modeling the switch-induced error voltage on a switched capacitor. *IEEE Transaction on Circuit and Systems*, 1983, vol. 30, no 12, p. 911-913.

[10] DING, Y., HARJANI, R. A universal analytic charge injection model. In *Proceedings of ISCAS 2000*, Geneva (Switzerland), 2000, p. I-144 – I-147.

About Authors...

Tomáš SUTORÝ was born in Hustopeče, Czech Republic, in 1976. He received the M.Sc. degree in 2003 in Electrical Engineering from the Brno University of Technology. Now he works toward the Ph.D. degree. He is with ON Semiconductor as an IC designer. His research interests are in the design of analog and digital electronic circuits.

Zdeněk KOLKA was born in Brno, Czech Republic, in 1969. He received the M.Sc. degree in 1992 and the Ph.D. degree in 1997, both in Electrical Engineering from the Brno University of Technology. In 1995 he joined the Institute of Radio Electronics, Brno University of Technology, where he has been appointed Associate Professor. His research and teaching interests are in computer-aided design of electronic circuits, modeling, and numerical algorithms.