A Monotonic Precise Current DAC for Sensor Applications

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Abstract. *In this paper a 17 bit monotonic precise current DAC for sensor applications is described. It is working in a harsh automotive environment in a wide temperature range with high output voltage swing and low current consumption. To guarantee monotonicity current division and segmentation techniques are used. To improve the output impedance, the accuracy and the voltage compliance of the DAC, two active cascoding loops and one follower loop are used. The resolution of the DAC is further increased by applying pulse width modulation to one fine LSB current. To achieve low power consumption unused coarse current sources are switched off. Several second order technological effects influencing final performance and circuits dealing with them are discussed.*

Keywords

Digital to analog converter, current output, segmentation, pulse width modulation, cascoding.

1. Introduction

Modern cars are equipped with more and more electronics, which requires also more advanced and precise sensors, which control vital functions in the car. More precise electronics to drive the sensors and measure their outputs is needed. Some sensors work only in a very narrow operating window. They must be kept in optimum operating point by applying very precise voltages or currents.

For an application with a particular gas sensor we designed an application specific integrated circuit (ASIC) which includes a special current DAC. The main requirement for this DAC is 17 bit resolution (16 bit + sign bit) with guaranteed monotonicity and no missing codes. Another requirement is a linear output voltage range from 0.9 V to 3.8 V for a minimum supply voltage of 4.75 V. The absolute accuracy of the full DAC including the on-chip voltage reference is ±1.3 % over the full operating temperature range (-40°C to 150°C die temperature). The current flowing to the sensor must be continuous. It excludes the use of calibration cycles. There are no special requirements for settling time and INL.

2. Inherent Monotonicity

The most demanding requirement is monotonicity and no missing codes over the full converter range, requiring a differential non-linearity (DNL) below 1 LSB.

Fig. 1 shows a current dividing DAC for one polarity of output current. An advantage of this topology is a limited number of used coarse current sources. For high resolution converters it is difficult to achieve monotonicity with this topology. This disadvantage is solved by a segmented current dividing DAC (see Fig. 2) with inherent monotonicity [1], [3], [6].

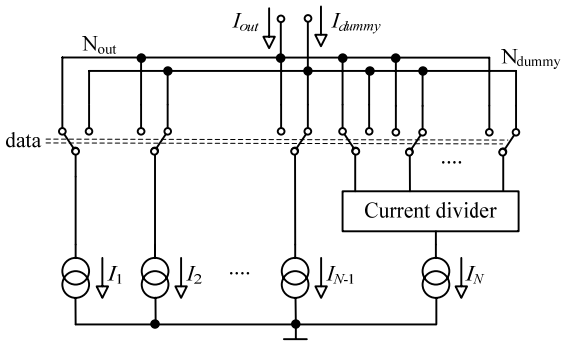

Fig. 1. Block diagram of current dividing DAC.

An array of identical coarse current sources $I_1 \ldots I_N$ (where N is the number of the current sources) is used. The coarse current sources I_1 to I_{Nc} (where N_c is the number of selected coarse current sources) are switched directly to the output I_{out}. The coarse current I_{Nc+1} is switched to the fine current divider. The remaining coarse current sources are switched to the dummy output I_{dummy}. The fine current divider is usually binary weighted [1]. Coarse and fine output currents are added. The total output current is

$$I_{out} = \sum_{i=1}^{N_c} I_i + I_{N_c+1} \sum_{i=1}^{N_f} k_i \,, \tag{1}$$

where k_i is the current dividing factor of the i-th branch of fine current divider (the sum of k_i of the full fine block is equal to 1),

N_c is the number of selected coarse current sources,

N_f is the number of selected fine current divider outputs.

The main advantage of this segmented current dividing DAC is its inherent monotonicity with respect to mismatches of coarse block current sources. The drawbacks of this configuration are the large area of the current source arrays for a 16 bit DAC, the limited output impedance without cascodes or the small output voltage range with cascodes on the current sources and the constant, high power consumption. These drawbacks are discussed in the following points.

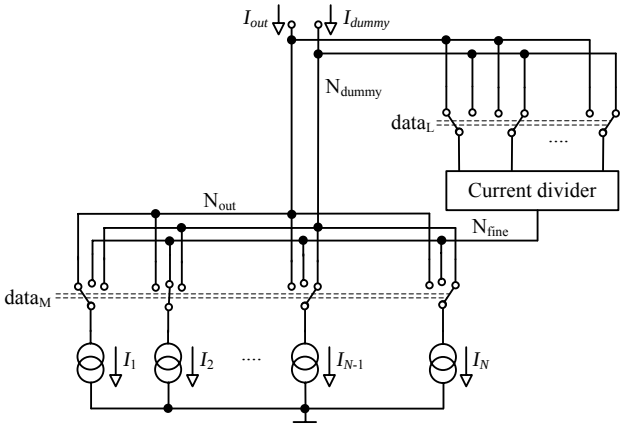

Fig. 2. Block diagram of segmented current dividing DAC.

2.1 Pulse Width Modulation Resolution Enhancement

To decrease the number of current sources in the coarse and fine blocks and also to keep the value of 1 fine LSB current at a reasonable level, a pulse width modulation (PWM) is applied to 1 fine LSB current. This reduces the area of the current source arrays. To preserve the inherent monotonicity of the DAC, the fine current divider has to be linearly weighted and the PWM modulation has to be applied to the first fine output not continuously connected to I_{out}.

The total output current consists of the coarse output current, the fine output current and the PWM modulated current.

$$I_{out} = \sum_{i=1}^{N_c} I_i + I_{N_c+1} \sum_{i=1}^{N_f} k_i + I_{N_c+1} k_{N_f+1} \frac{t_{PWM}}{T_{PWM}} \qquad (2)$$

where t_{PWM} is the PWM pulse width and T_{PWM} is the PWM period.

2.2 Active Cascoding of Current Sources

Contrary to a current DAC with a voltage output, the output voltage is not constant and the output impedance and voltage compliance become important. In our application the voltage headroom for the full DAC is only 0.9 V in the worst case. To achieve high accuracy, high output impedance and low differential non-linearity DNL, active cascodes on the coarse current sources and the fine block divider are required.

By adding operational amplifier OA2 (Fig. 3), the fine block is configured as an active cascode for the coarse block. Operational amplifier OA1 and cascoding transistor MC1 in Fig. 3 form a common active cascode on the coarse current source output. Finally operational amplifier OA3 buffers the voltage on the output pin N_{out} to node N_{dummy}. This makes the same drain voltage for all fine bit transistors and improves the current division accuracy without an extra cascode. Using active cascodes, the coarse or fine bit transistors can be operated close to their linear mode without accuracy and monotonicity degradation.

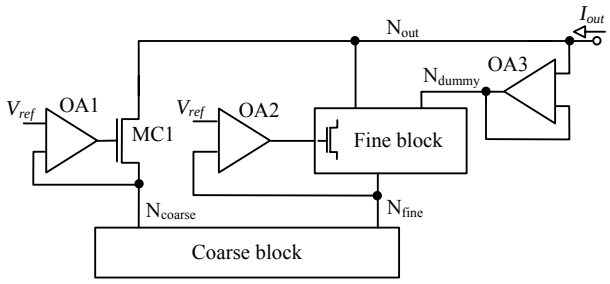

Fig. 3. Block diagram of classical active cascoding structure.

In Fig. 4, the positive input of operational amplifier OA1 is connected to N_{fine} instead of V_{ref}. In this way, the voltage difference between nodes N_{fine} and N_{coarse} is given only by the offset of operational amplifier OA1 and not by the combined offset of OA1 and OA2. Note that the opposite connection is not possible because for currents below 1 coarse LSB, no current is flowing through the MC1 cascode and node N_{coarse} is floating.

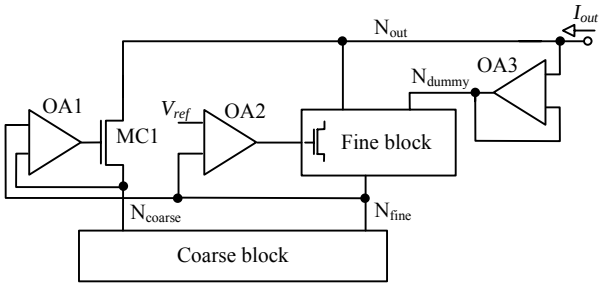

Fig. 4. Block diagram of improved active cascoding structure.

During measurement of the DAC, it was found that for low temperatures impact ionization (hot electrons) in the cascoding transistor MC1 (Fig. 5) caused an error of several LSB when changing the output voltage ±1.3 V (even for long channel NMOS transistor) – see Fig. 6.

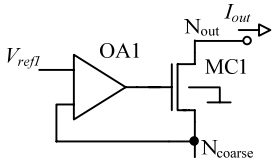

Fig. 5. Active cascoding with one cascoding transistor.

To decrease the influence of the impact ionization a double cascode with two regulation loops was used – see Fig. 7. MC1 and OA1 are creating the original cascode for the coarse current sources, added cascoding transistor MC4 and operational amplifier OA4 are cascoding the MC1 transistor (second reference voltage V_{ref2} is used). Measurement results are shown in Fig. 8.

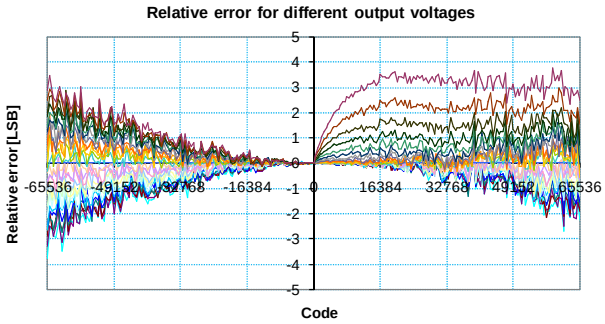

Fig. 6. Measured error caused by impact ionization (hot electrons) in the cascoding transistor MC1 (see positive codes).

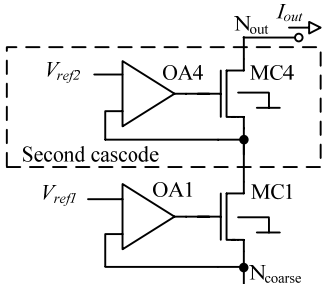

Fig. 7. Active cascoding with two cascoding transistors and two regulation loops.

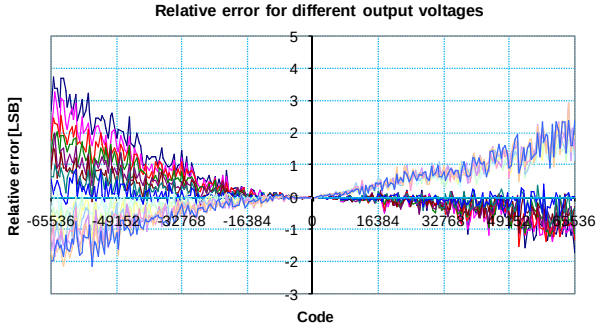

Fig. 8. Measured error caused by impact ionization when using two cascoding transistors (see positive codes).

2.3 Low Power Consumption

It is a well-known approach to achieve good linearity to dump the unused coarse current sources. When doing this the current consumption of the DAC is constant over the code. In our application the DAC is typically working with much lower currents than the maximum output current and low current consumption is important.

To save power, unused coarse current sources are switched-off instead of dumped in a dummy node. This significantly decreases the current consumption when the DAC operates at low output currents. This method is known to be much less linear and requires a very careful analysis of all resistances in the coarse block current mirrors. Even small metallization resistances can significantly influence the absolute accuracy and the DNL of the converter due to changes in the current pattern for successive switching of the coarse current sources. The source side of the current sources is of course very sensitive but also the node N_{coarse} is important since the transistors work close to linear mode. Fig. 9 is showing a simplified schematic of the current mirror with indicated metallization resistance.

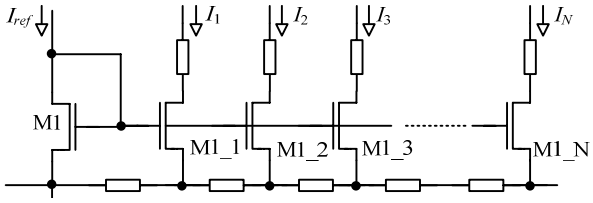

Fig. 9. Simplified schematic of current mirror with metallization resistance.

A manual back annotation of all resistors in the array has been done and the converter accuracy and DNL have been verified. Layout of one coarse current unit is shown in Fig. **10**, the comparison of the simulated and measured DNL error is shown in the measurement section in Fig. 21.

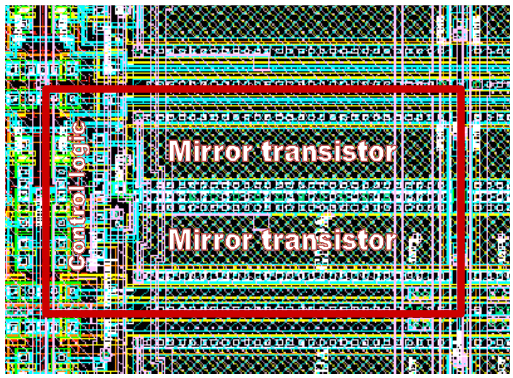

Fig. 10. Layout of one coarse current unit.

In order to limit the series resistances, all mirror transistors inside the coarse blocks are mostly covered by metal (see Fig. 10). Excessive metal coverage over matched transistors can cause MOS transistor threshold voltage shift [5] and significantly degrade matching. To solve this, a special annealing process step was added in the processing.

3. Complete Schematic

Fig. 12 shows splitting of the 17 bit digital input word between coarse, fine and PWM blocks.

To realize the sign (polarity) two complete 16 bit current DACs are constructed, one with NMOS current mirrors sinking current and the other one with PMOS current mirrors sourcing current.

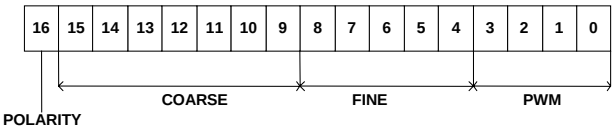

Fig. 12. Separation between coarse block, fine block, and PWM.

The complete block diagram of the NMOS current DAC with active cascode loops and the dummy node buffer is shown in Fig. 11. The coarse block is a linearly weighted low drop current mirror. The outputs of the $I_1 \ldots I_{Nc}$ coarse currents are fed to the cascode MC1. The I_{Nc+1} coarse current is connected to the fine block where the current is further divided. The remaining coarse currents are switched-off. On the outputs of each coarse current source, two switches are used. The first switch SWxa is controlled by a thermometer code and the second switch SWxb is controlled by a code 1 of N. The fine block is also a linearly weighted array and PWM is applied to the first fine output not connected to N_{out}. On the outputs of each fine current source, two-way switches are used, which connect the currents to output N_{out} or to the dummy branch N_{dummy}. The first switch in the fine block not continuously connected to N_{out} is modulated by the PWM signal.

The current offset of the PMOS and the NMOS current DACs is trimmed by adjusting the W/L ratio of reference transistor M1. The optimum trimming code is stored in a one time programmable memory. To find the optimum trimming code and limit the trimming time, only the coarse currents are measured (Fig. 13).

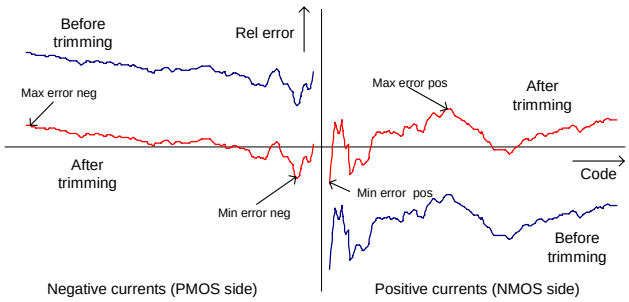

Fig. 13. Trimming of absolute accuracy.

4. Matrix Construction

Both coarse and fine blocks are constructed in a matrix structure.

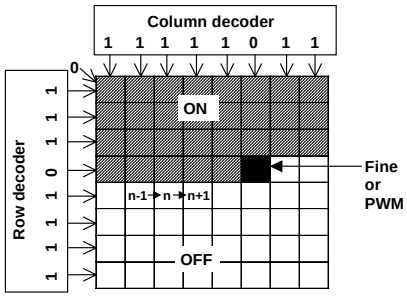

Fig. 14. Realization of decoding and current matrix.

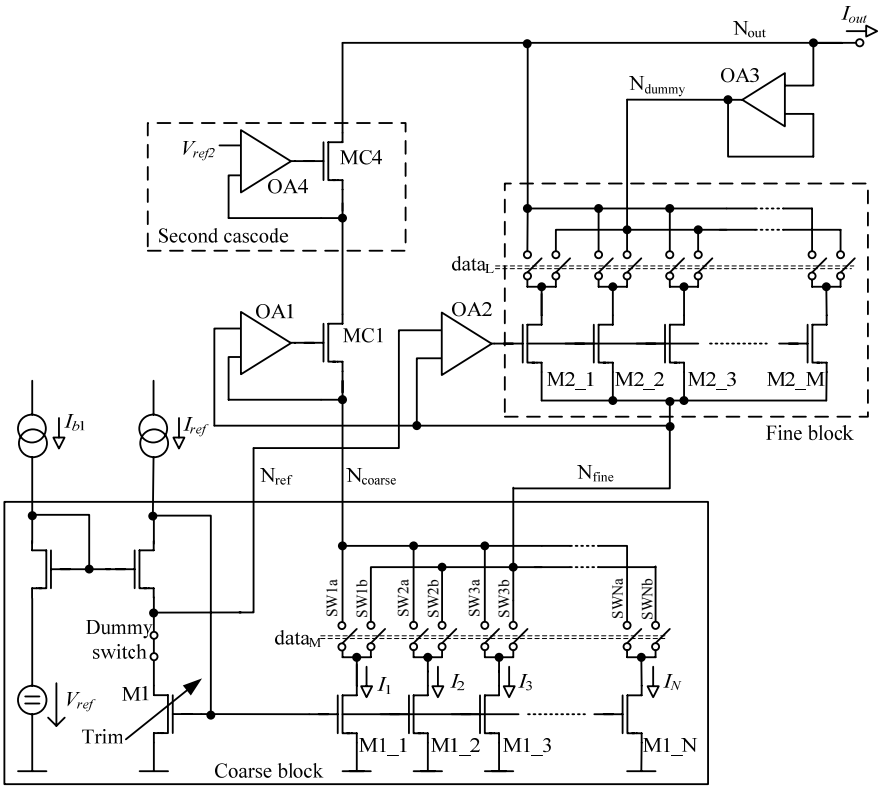

Fig. 11. Simplified schematic diagram of the NMOS current DAC.

Each matrix cell contains the mirror transistor, the two current switches and a logic circuit. It combines the row and column decoder inputs with the status of the previous cell to control the current switches. This embedded logic control decreases the matrix layout and decoder complexity. On the other hand it slows the large signal response of the DAC due to its serial structure. The speed of the DAC was not an important requirement of the system. Fig. 14 shows a simple arrangement for a 6 bit matrix with the row and column decoder signals and the serial input signal for the first cell.

The structure in Fig. 14 is vulnerable to processing gradients. Better linearity is achieved by randomization of the decoders at the expense of more complex layout. A good compromise between complexity and accuracy is obtained by the pseudo-random organization in Fig. 15. The reference transistor M1 is split into four equivalent parts (M1a…M1d), which are placed in the corners of the main matrix (see Fig. 15).

Column decoder switching sequence

		5	6	7	8	1	2	3	4
Row decoder switching sequence	7	M1a	53	54	55	56	49	50	51	52	M1c
	5		37	38	39	40	33	34	35	36	
	3		21	22	23	24	17	18	19	20	
	1		5	6	7	8	1	2	3	4	
	2		13	14	15	16	9	10	11	12	
	4		29	30	31	32	25	26	27	28	
	6		45	46	47	48	41	42	43	44	
	8	M1b	61	62	63	64	57	58	59	60	M1d

Fig. 15. Pseudo-random switching sequence of a 8 x 8 matrix.

The embedded logic for the NMOS coarse matrix is shown in Fig. 186. The row and column decoders are 1 of N decoders with negative logic output (negative logic simplifies the embedded logic). Signal N_{minus1} is the output of the previous cell and is set to zero for the first cell. It propagates a zero and closes switch SWOUT through the matrix until the selected cell is reached. For the selected cell the signal SWFINE is one, SWOUT is zero and N_{plus1} is one. For all following cells N_{minus1} is one, and the current sources are switched off.

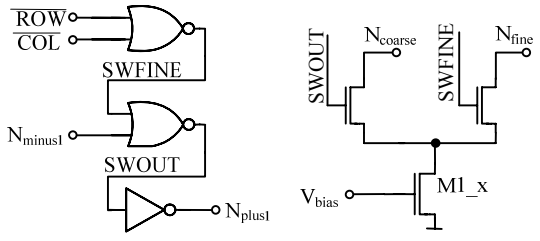

Fig. 16. Coarse block cell including decoder, current source M1 and switches.

During measurement it was found that the NMOS side DNL error increased at high temperatures (see Fig. 17). This error was caused by off-state channel leakage through the coarse block switches. At 150°C the channel leakage increased to 1 nA per switch, causing several LSB DNL error at coarse bit changes for low currents. This was solved by using double switches with middle point connection to the supply – see Fig. 18.

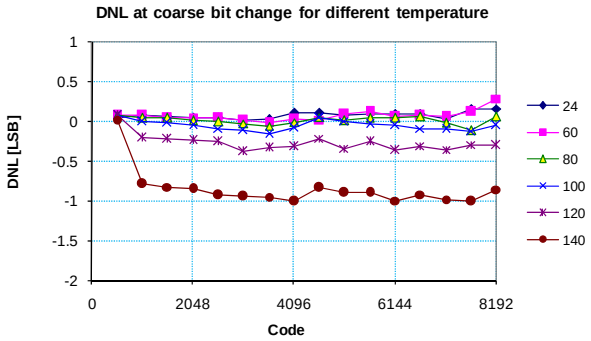

Fig. 17. Measured DNL caused by off state leakage.

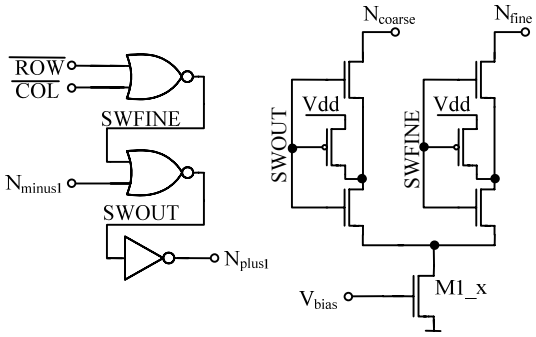

Fig. 18. Improved coarse block cell including decoder, current source M1 and double switches.

The embedded logic for the fine block is shown in Fig. 19. This logic includes a multiplexer, which connects SWOUT to the switches before the selected cell and connects the PWM signal to the switches for the selected cell only. Complementary switches are used to cancel clock feed through.

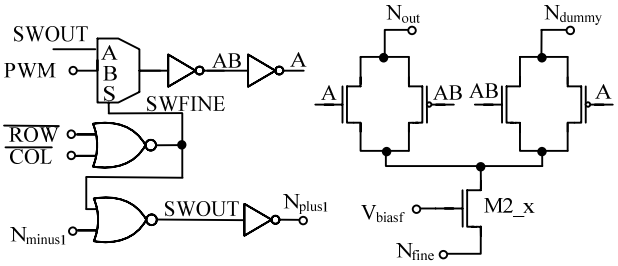

Fig. 19. Fine block cell including decoder, current dividing transistor (M1) and complementary switches.

5. Implementation and Results

The DAC was processed in a 0.7 μm, n-well CMOS technology with single polysilicon and double metal interconnect. Layout area of the DAC is 1.4 mm^2. The die photo showing the DAC with different blocks is in Fig. 20.

The maximum output current is ±6.5 mA and 1 LSB corresponds to a current of 99.2 nA.

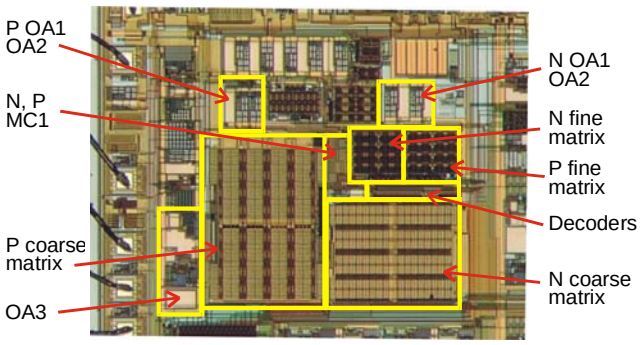

Fig. 20. Photo of the realized 17 bit DAC.

Fig. 21 shows measurement results of DNL at coarse bit changes (where the DNL error is maximum). The measured DNL error is compared with calculated (normalized) DNL error caused by metallization resistance. The residual error is mainly caused by metal resistance of ground and supply tracks. Absolute accuracy over temperature is shown in Fig. 22. Fig. 23 shows dependency of the output current on the output voltage for different codes (given by output impedance of the DAC).

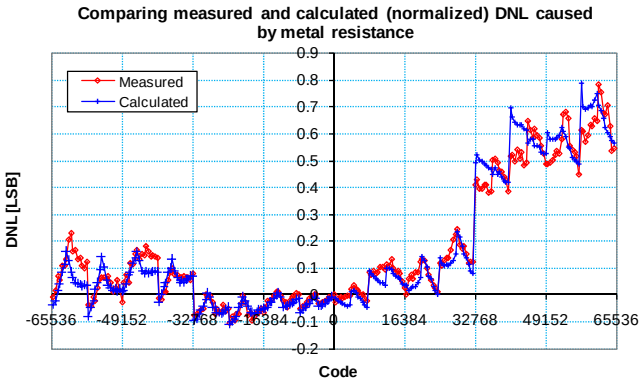

Fig. 21. Measured DNL error compared with calculated (normalized) DNL error caused by metal resistance.

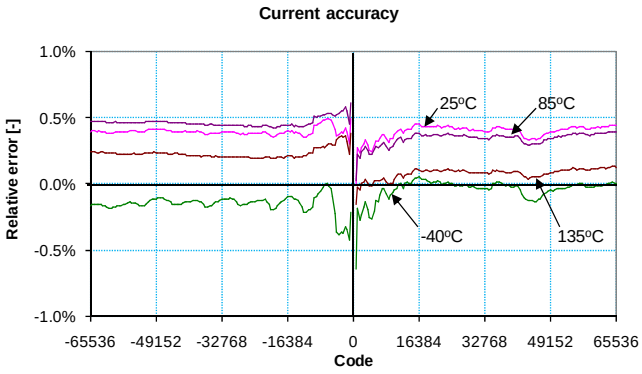

Fig. 22. Measured absolute accuracy.

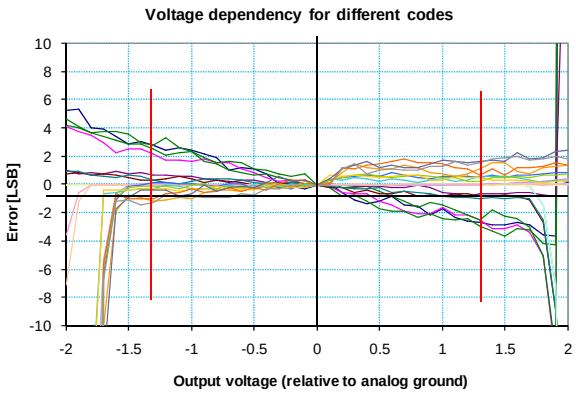

Fig. 23. Measured voltage dependency for different codes.

Finally, an accuracy shift at low temperatures (0°C to -40°C) was observed on some samples. This was caused by package stress, which increases at low temperatures and depends on the package type. For one selected worst case sample currents in the coarse current sources were measured and displayed in a matrix - see Fig. 24. Clear shift of currents of the current sources in one area of the matrix is visible.

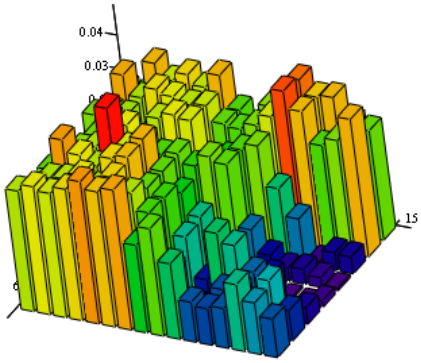

Fig. 24. Relative error of the coarse current sources displayed in a matrix.

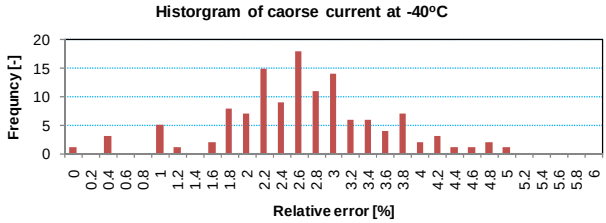

Fig. 25. Histograms of the coarse currents for low temperature.

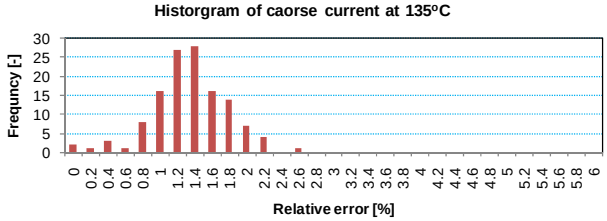

Fig. 26. Histograms of the coarse currents for high temperature.

Histograms of the relative current error for one device at two temperatures are shown in Fig. 25 and Fig. 26. To decrease impact of the package stress to the accuracy of the trimmed DAC, the DAC is trimmed at low temperatures.

Worst case settling time of the DAC happens when the polarity of the current is reversed. It means one part of the DAC is almost switching off to save current consumption and the other part is starting to operate. When switching to maximum output current we need also to charge the biggest capacity on the gates of the coarse block mirror transistors. Measurement results of such a worst case settling time when switching between code –65535 and 65535 is shown in Fig. 27. Measured settling time when switching polarity for maximum current to achieve full accuracy is below 20 μs.

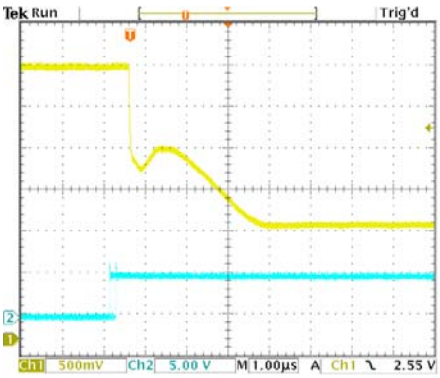

Fig. 27. Measured settling time (channel 1, output is connected to 150 Ω resistor at 2.35 V).

6. Summary

A low power consumption 17 bit monotonic precise DAC with current output was realized in a single polysilicon 0.7 μm CMOS technology. It is currently used in series production as a part of an automotive ASIC and it fulfills all requirements of the harsh automotive environment.

The segmentation technique, linearly weighted blocks and active cascading were used to achieve monotonicity over the full converter output voltage and temperature range.

Higher order effects like metallization resistance, impact ionization, off-state channel leakage, MOS threshold voltage shift due to metal coverage and package stress at cold were discussed and solutions were shown.

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Pavel HORSKÝ was born in 1970. He graduated in 1994 at the Brno University of Technology in Radio Electronics. He got his Ph.D. from the Brno University of Technology in 1998 in the field of metrology. He is working in ON Semiconductor, formerly AMI Semiconductor, Alcatel Microelectronics and CEDO since 1997. He works as analog/mixed signal senior design engineer mainly for automotive products.