# A Novel 2.4GHz CMOS Up-Conversion Current-Mode Mixer

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**Abstract.** *In this paper, a low-power up-conversion current-mode mixer, designed in the chartered 0.18-μm RFCMOS technology, is proposed to realize the transmitter front-end in the frequency band of 2.4 GHz. The proposed mixer can convert a 10 MHz intermediate frequency (IF) signal to a 2.4 GHz RF signal, with a local oscillator power of 2 dBm at 2.39 GHz. A comparison with conventional voltage-mode up-conversion mixer shows that this mixer has advantages of low voltage, low power consumption and high performance. Simulation results demonstrate that at 2.4 GHz, the circuit provides 6.5 dB of conversion gain and the input-referred third-order intercept point (IIP3) of 15.3 dBm, while drawing only 5.7 mA from a 1.2V supply voltage. The chip area is only 0.7 mm × 0.8 mm.*

## Keywords

Current-mode mixer, up-conversion mixer, CMOS, high linearity, low power.

## 1. Introduction

Recently, the growing demand for RF and wireless applications has attracted a great deal of researches on designing high performance and low cost RF integrated circuits and systems with the advanced CMOS technologies. In the RF transmitter front-end, one of the indispensable analog blocks is the up-conversion mixer. The purpose of an up-conversion mixer is to convert the incoming intermediate frequency (IF) signal to a radio frequency component for reliable transmission.

The structure of up-conversion mixer has been reported in many CMOS designs. Passive up-conversion mixers have the advantage of better linearity, but they have conversion loss and require large LO, which will increase power dissipation. To generate large LO signals for passive mixers in low supply voltage is difficult [1, 2]. Voltage-mode up-conversion Gilbert mixers based on the method of current commutating have often been selected. Although Gilbert mixers have larger conversion gains and little noise figure, they require higher voltage headroom and larger power. This makes them difficult to work in low supply voltage and low power [3-6].

Unlike voltage-mode circuits, where the commonly available voltage headroom is limited by the supply voltage, current-mode circuits have low impedance at internal nodes and signal information is carried by the time varying currents. Thus, the voltage at each node can be small, resulting in higher linearity and lower power performance. It is well known that in the design of mixers, linearity and power dissipation are the key performance parameters. Thus, a current-mode technique can be used to improve the linearity of a mixer operating with a low supply voltage and a low power [7-9]. Current-mode mixer circuits therefore have great potential in the design of RF integrated circuits in advanced nanometer CMOS technologies.

In this paper, a novel 2.4 GHz up-conversion current-mode mixer in 0.18-μm RFCMOS technology is proposed. In the proposed current-mode mixer, both input and output ports are current signals produced by current-squaring circuits and current mirrors. Compared to the previously published CMOS voltage-mode up-conversion mixers operating at the similar frequency ranges [4-6] and to other current-mode mixers [7, 8], the proposed up-conversion current-mode mixer has the advantages of larger conversion gain with 6.5 dB, much higher linearity and smaller power consumption, and it operates at lower voltage supply of 1.2 V.

The contents of this paper are as follows. In Sec.2, the operational principle and circuit realizations are presented. The results of post-layout simulation are reported in Sec.3 to verify the performances of the proposed up-conversion current-mode mixer. Finally, the conclusions of this work are given in Sec.4.

## 2. Operational Principle and Circuit Implementation

Based on Gilbert cell, a double balanced CMOS up-conversion current-mode mixer was designed. Compared to the traditional published works, the mixer improves the linearity significantly with input current-squaring circuit

and it shares the output loading with the capacitive cross-coupling techniques that enhance the conversion gain.

## 2.1 Input Current-Squaring Circuit and Class AB Topology

The circuit diagram of the proposed current-squaring circuit is shown in Fig. 1(a) which is modified from [10, 11]. The transistors M1A–M4A are biased to operate in saturation region. Suppose that the threshold voltages of M1A-M4A are $V_{th}$, the relation between $V_{GS,M1A}$, $i_o$ and $i_{IF}$ can be expressed as:

$$V_{GS,M1A} = \frac{vdd}{2} + \frac{i_{IF}}{\kappa \frac{w}{l}(vdd - 2V_{th})}, \quad (1)$$

$$i_o = N \times \left( I_B + \frac{i_{IF}}{2} + \frac{{i_{IF}}^2}{16 I_B} \right), \quad (2)$$

$$I_B = \frac{1}{8} \kappa \frac{w}{l} (vdd - 2V_{th})^2 \quad (3)$$

where $w/l$ is the channel width to channel length ratio of the MOS devices, $\kappa = \mu_0 C_{ox}$ is the mobility $\mu_0$ times the oxide capacitance per unit area $C_{ox}$. The current $i_1$ is copied by the current-mirror amplifier formed by M1A and M3A and the aspect ratio of M3A is $N$ times that of M1A. From (2), the current-squaring function is realized. The transistor M4A acts as a current buffer and keeps the $V_{DS}$ of M3A the same as $V_{DS}$ of M1A to prevent from the channel length modulation, which would degrade the mirroring operation. Besides, the unwanted harmonic components inherently affected by the quadratic characteristic of MOS transistors, lead to leakages of IF at the outputs, which usually affect linearity of the mixer.

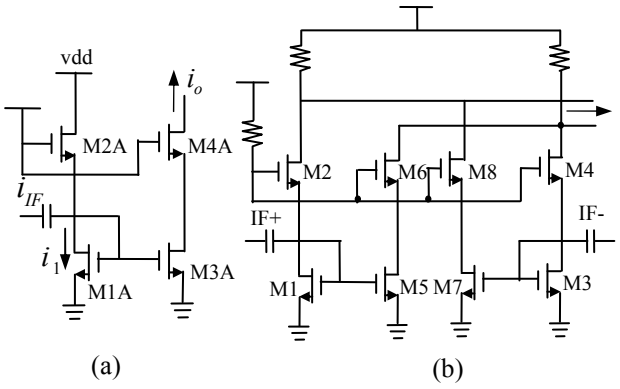


**Fig. 1.** The input stage of the proposed mixer. **(a)** The current-squaring circuit. **(b)** The proposed of class AB high-linear topology.

One way to improve linearity of the current-squaring circuit is by using the cross-coupled class AB topology [12] which is shown in Fig. 1(b). The circuit has the advantage that the current flowing trough M1 and M3 contributes to the output current, thanks to current mirrors Ml-M5 and M3-M7. This arrangement makes the circuit less sensitive to linearity degradation due to common-mode signals, since each output depends on both inputs.

## 2.2 Capacitive Cross-Coupling Output Technique

The technique we described is based on capacitive cross-coupling across the two sides of a differential output stage in up-conversion current-mode mixer. An obvious advantage of the capacitive cross-coupling is its inherently suitability for fully differential operation [13-15]. The capacitive cross-coupling technique has been used for gain enhancement and RF output matching in this paper.

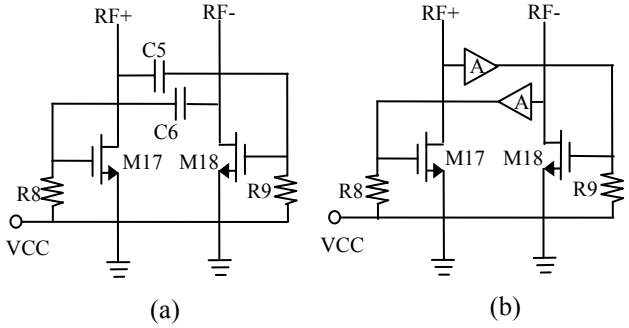


**Fig. 2.** The output stage of the proposed mixer. **(a)** The cross-coupled differential amplifier. **(b)** Two cross-coupled capacitors act as two buffer amplifiers.

It consists of two NMOS (M17, M18), two coupling capacitors (C5, C6) and two resistors (R8, R9). The capacitive cross-coupling pair (C5, C6) in Fig. 2(a) offers a feedback loop to each NMOS of the differential output to boost up the conversion gain in high frequency. It compensates the high-frequency gain decay of NMOS and then widens the working frequency of the RF output stage. Higher coupling capacitors give both higher amplifier-gain and lower corner of the working frequency. Theoretically two times of the transconductance of the NMOS can be reached if coupling capacitor is much larger than the gate-drain parasitic capacitor of each NMOS [14]. Besides, this technique reduces the Miller effect of the gate-drain capacitance of the main transistors, further improves the linearity of the mixer. Two coupling capacitors in Fig. 2(a) act as two buffer amplifiers. The equivalent circuit of Fig. 2(a) is shown in Fig. 2(b).

## 2.3 Circuit Design

The circuit diagram of the proposed CMOS up- conversion current-mode mixer including the biasing circuit is shown in Fig. 3. The input current-squaring circuit as the input stage, which is consist of M1-M8. The function is to transfer the received incoming IF signal from current to current that serves as the biased current of the four NMOS (M9-M12). M9-M12 act as switches to modulate the current provided by M1-M8, which is double balanced topology with the advantage of rejecting the strong LO signal and the even-order distortion products. To make M9-M12 as ideal switches, the transistors are biased in the saturation region that is close to the triode region. The output current-mirror (M13-M18) shares the output loading with the capa-

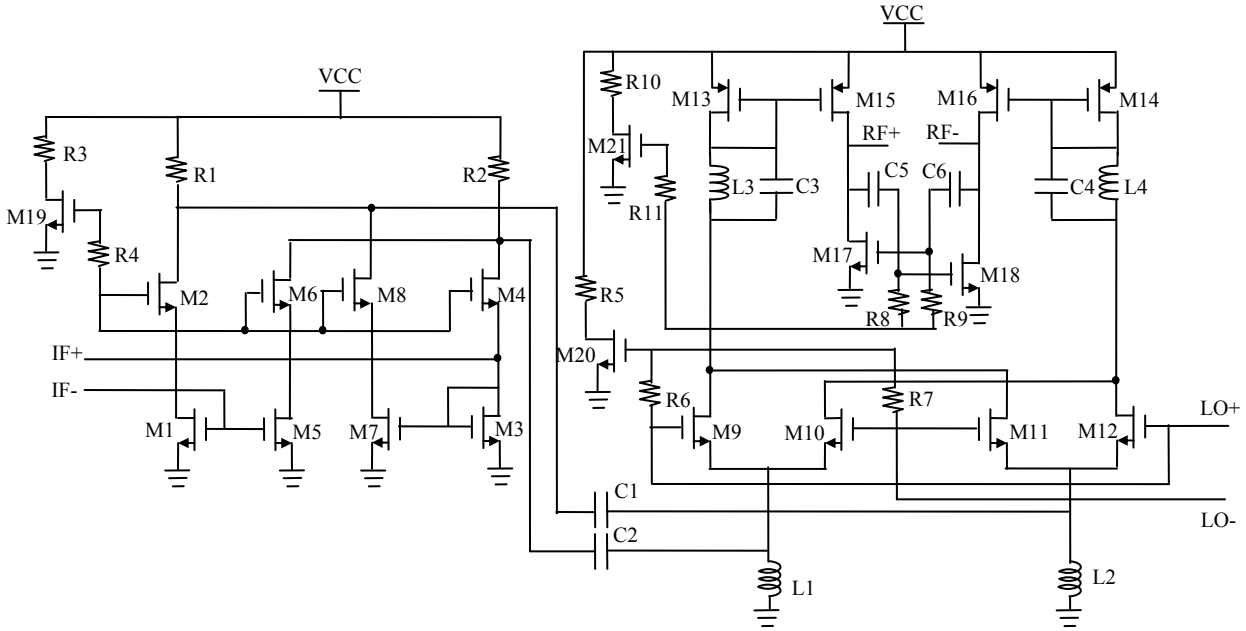


**Fig. 3.** Circuit diagram of the CMOS up-conversion current-mode mixer (with biasing circuit).

| Inst. | Para. | Inst. | Para. | Inst. | Para. |
|---|---|---|---|---|---|
| M1-M4 | $w/l$ =10/0.18 μm | C1,C2 | 10 pF | R3 | 1.27 kΩ |
| M5-M8 | $w/l$ =320/0.18 μm | C3,C4 | 2.6 pF | R4 | 19.8 kΩ |
| M9-M12 | $w/l$ =60/0.18 μm | C5,C6 | 1.4 pF | R5,R11 | 5 kΩ |
| M13,M14 | $w/l$ =80/0.18 μm | L1,L2 | 2.39 nH | R6,R7 | 10 kΩ |
| M15,M16 | $w/l$ =310/0.18 μm | L3,L4 | 1.43 nH | R8,R9 | 106 Ω |
| M17,M18 | $w/l$ =90/0.18 μm | R1,R2 | 1.25 kΩ | R10 | 1.58 kΩ |
| M19,M21 | $w/l$ =1/0.18 μm | | M20 | $w/l$ =45/0.18 μm | |

**Tab. 1.** Summary of instance parameters.

citive cross-coupling capacitors (C5, C6) that enhance the conversion gain. Degeneration inductors (L1, L2) are used in the mixer to improve linearity. C1 and C2 are applied to be the DC-blocking capacitors to isolate the IF port from the dc source.

The two parallel LC resonant tanks (L3, C3) and (L4, C4) at the circuit are used as the band-pass filter to reject the further products except the RF frequency at around 2.4 GHz. Nevertheless, the signal at the LO frequency plus the IF frequency, and the signal at the LO frequency minus the IF frequency, are both mixed to the RF frequency. Besides the desired signal, the image signal is also produced. A common way of avoiding this image problem in fully-integrated transmitter is the use of I/Q up-conversion mixer, the IF signal is multiplied by both the in-phase (I) LO signal and a quadrature (Q) LO signal. Using this technique in the transmitter, the image and desired signals remain distinct in the complex RF signal.

The circuit is biased by means of current mirrors. To minimize the power consumption, the width of M19 to M21 is set to smaller. The resistors R1 to R11 are added for signal choking, which must be selected so larger that their equivalent interference current signals can be ignored. The design parameters of most instances in Fig. 3 are summarized in Tab.1.

## 3. Post-Layout Simulation Results

The up-conversion current-mode mixer is simulated by version 6.1 of Cadence SpectreRF with chartered 0.18-μm RFCMOS process parameters. The layout has been drawn and the arrangement has been placed as symmetrical as possible to decrease mismatches. The parasitic effects have been extracted and taken into account in the post-layout simulations. Fig. 4 shows the simulation of S22, which is below –15 dB from 1.5 GHz to 5 GHz, indicating a good broadband RF output matching. Fig. 5 shows the conversion gain, the conversion gain is 6.5 dB when the

input LO power is 2 dBm. The linearity is checked when the RF output frequency at 2.4 GHz with 10 MHz and 10.1 MHz as two-tone input sources. Fig. 6 shows the input-referred third-order intercept point (IIP3) of the block is 15.3 dBm. Fig. 7 shows the transient simulation results with input IF signal at 10 MHz of which the signal level is -30 dBm and the LO signal at 2.39 GHz. The power dissipation is 6.8 mW from a 1.2V supply voltage. The layout diagram of the circuit is shown in Fig. 8, which takes a compact chip area of 0.7 mm×0.8 mm including testing pads.

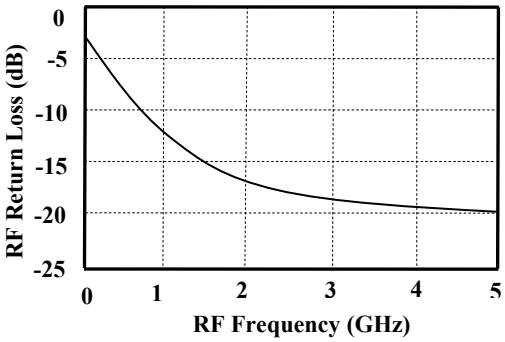


**Fig. 4.** Post-layout simulation of S22.

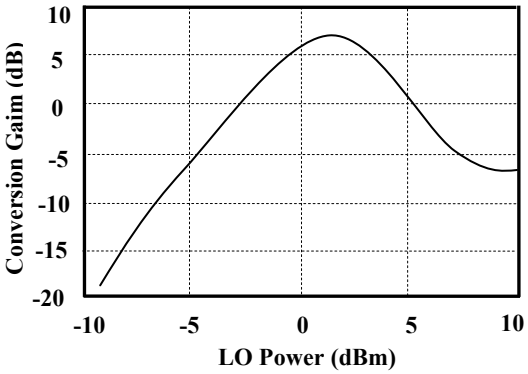


**Fig.5.** Post-layout simulation of Conversion Gain versus LO power with RF=2.4 GHz.

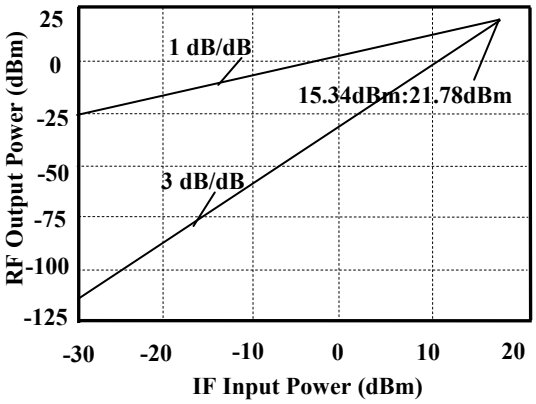


**Fig. 6.** IIP3 of the proposed current-mode mixer (LO power: 2 dBm).

Finally, the post-layout simulation performance of the up-conversion current-mode mixer is summarized in Tab. 2, where comparisons with other published CMOS mixers are also provided. From Tab. 2, the proposed up-conversion current-mode mixer can achieve high conversion gain and a higher linearity with low LO power while, at the same time, achieving a smaller chip area by adjusting the compact structure in the proposed mixer.

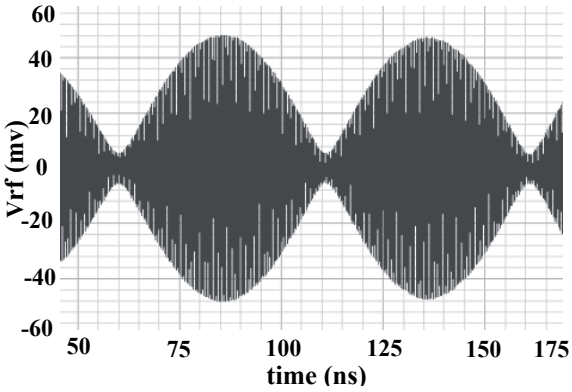


**Fig.7.** The transient analysis of the up-conversion current-mode mixer.

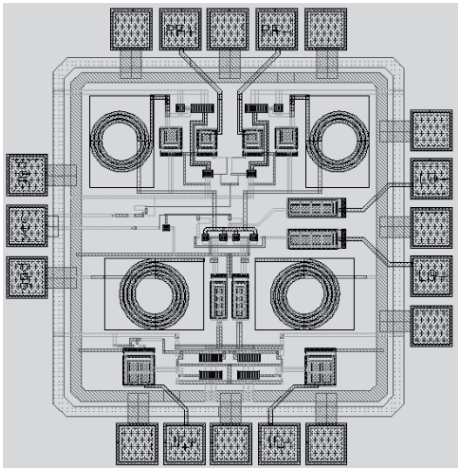

**Fig.8.** The layout diagram of the current-mode mixer (0.7mm×0.8mm).

# 4. Conclusion

This paper has proposed the analysis and simulation of a CMOS up-conversion current-mode mixer. The mixer is by using the input current-squaring circuit of cross-coupled class AB topology which significantly improves the linearity, and it shares the output loading with the capacitive cross-coupling technique that enhance the conversion gain. The post-layout simulation shows that the mixer only consumes 6.8 mW under low supply voltage of 1.2 V, the excellent simulation results have shown that the proposed current-mode mixer is suitable for the applications of low-voltage and low-power CMOS transmitters.

The experimental chip has been designed and under fabrication. Future research will be conducted to design a complete 2.4 GHz CMOS current-mode transmitter using the proposed I/Q mixer arrangement and integrating it with an on-chip power amplifier.

| Reference | [4] | [5] | [6] | [7] | [8] | This work |
|---|---|---|---|---|---|---|
| Technology | 0.18-μm | 0.18-μm | 0.18-μm | 0.13-μm | 0.6-μm | 0.18-μm |
| Topology | Voltage-mode | Voltage-mode | Voltage-mode | Current-mode | Current-mode | Current-mode |
| LO power | 0 dBm | 3 dBm | 0 dBm | 0 dBm | 6 dBm | 2 dBm |
| Conversion gain | 2.5 dB | 6.5 dB | 15 dB | 1 dB | -9 dB | 6.5 dB |
| IIP3 | 6.5dBm** | -9 dBm | -15 dBm | 12 dBm** | 10 dBm | 15.3dBm |
| Power dissipation | 39 mW | 15.3 mW | 15 mW | 3 mW | 3 mW | 6.8 mW |
| Area($mm^2$) | 1.4×1.3 | 0.9×0.7 | 1.1×1.0 | 1.4×1.0 | 0.4×0.4 | 0.7×0.8 |

** The result is estimated from its $P_{1dB}$.

**Tab.2.** Performance summaries of the proposed mixer and comparisons with other published mixers.

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