Dual Band High Efficiency Power Amplifier Based on CRLH Lines

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Abstract. *In this paper we propose the use of Composite Right/Left Hand (CRLH) and Extended Composite Right/Left Hand (ECRLH) transmission lines for the design of dual band high efficiency power amplifiers working in CE class. The harmonic termination can be synthesized using the meta-lines is particularly suitable for CE class amplifiers, which have a termination not as sensitive to the third harmonic as F class amplifier. This paper presents the design procedure and the design equations. The non-linear phase response of a CRLH and ECRLH transmission line has been utilized to design arbitrary dual-band amplifiers.*

Keywords

Power Amplifier, Meta-materials, CE class, CRLH, ECRLH, Diplexer, Statistical Sensitivity.

1. Introduction

The demand on wireless communication systems is forcing frequency spectrum to get higher. As frequency arises two problems appear: firstly, losses in transmission lines increase quite a lot and secondly, radio-frequency (RF) solid state devices are power limited. Due to the current demand on multi-frequency systems over several wireless communication bands, systems simultaneously working at some of the following bands (GSM, TETRA, DCS, PCS, IMT-2000, WLAN, or UWB) are currently being developed and are widely used in new portable wireless handsets.

In addition to the multi-frequency performance required, other critical problem is the great amount of RF power needed or the power consumption in portable devices (high power consumption results in large batteries and/or short battery lifetimes). For the first matter it could be thought of combining a lot of RF devices to reach the required RF power level. While, for the second matter, efficient electronics designs would maximize the device power performance. The circuit within such a device that typically consumes most power (sometimes as much as half of the DC power supplied) is the RF power amplifier, which converts the DC power from the battery into the RF signal that is transmitted through an antenna. Maximizing the efficiency of the power amplifier can allow reducing the battery size and/or increasing the battery life or the signal strength. Furthermore, efficient amplifiers also generate less heat, increasing the device lifetime and reliability.

Then, due to the high demand of wireless services at different frequencies, the availability of multi-frequency (or at least dual frequency) high efficiency amplifiers would be welcome. Some attempts have been undertaken in order to achieve that goal. In this way, the use of switches [1], varying lumped components [2] or diplexers [3] have been proposed as potential techniques for achieving dual-frequency high efficiency amplifiers.

During last years the appearance of CRLH lines [4] has opened new possibilities in the design of dual band amplifiers. Up to the authors' knowledge only one approach using CRLH lines to design to dual band high efficiency amplifiers has been proposed [5]. However, that amplifier lacks of the harmonic termination to achieve high efficiency. This paper pays attention to the harmonic terminations in high efficiency amplifiers at dual frequencies to achieve efficiency as high as possible. A second attempt to achieve dual frequency high efficiency amplifiers has been proposed in [6]. A dual frequency network tries to match the fundamental and the harmonic frequencies to aim at high efficiency amplifiers. However, the study presented in this paper shows that these networks are extremely sensitive to the components tolerance limiting the performance of the dual band amplifiers.

Recently, some generalizations on CRLH lines have appeared [7, 8] what could allow obtaining suitable phase conditions at three or four different frequencies. For instance, the extended E-CRLH lines [7] present load control at four frequencies allowing the design of a quad-band amplifier (with harmonic conditions not only to the second harmonic, but to third or fourth, or as it is shown later in this paper, dual amplifiers with load conditions to the second harmonic).

The load, bias conditions and the harmonics termination to overdrive the power level for single frequency RF power amplifiers (A, B, C, D, E, or F) have been summarized in [9] and [10]. The choice of a class implies a trade-off between various power amplifier figures of merit, which include gain, linearity, and efficiency. In this paper the authors have studied the realization and performance of dual frequency high efficiency amplifiers. Five possible solutions using meta-lines are proposed for this goal (the first two solutions are based in the same way as the one described by Dupuy et al. [11]). We will be mainly concerned on CE class power amplifiers since they provide larger efficiency and low bias supply and, what is more, the fact that it is the fundamental high efficiency amplifying class in bipolar transistor:

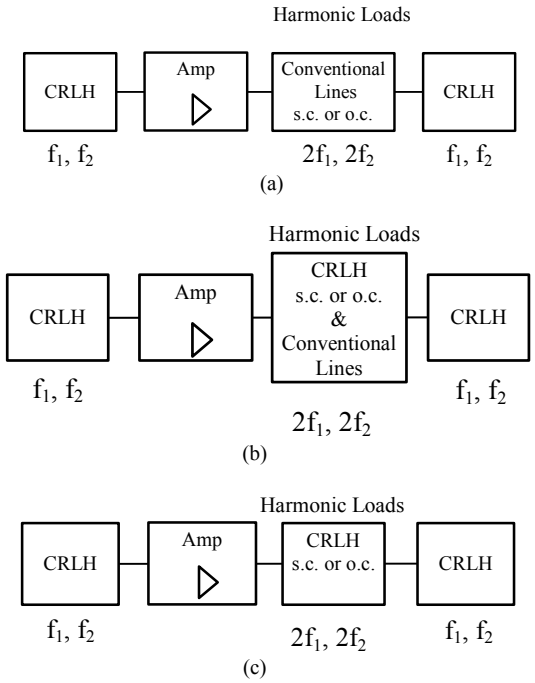
a) CRLH lines at the input and output to control two frequencies (f_1 and f_2), and conventional lines to control output harmonics ($2f_1$ and $2f_2$) (Fig. 1a).

b) CRLH lines at the input and output to control two frequencies (f_1 and f_2), and conventional lines mixed with CRLH lines to control output harmonics ($2f_1$ and $2f_2$) (Fig. 1b).

c) CRLH lines at the input and output to control two frequencies (f_1 and f_2), and CRLH lines to control output harmonics ($2f_1$ and $2f_2$) (Fig. 1c).

d) CRLH lines at the input to control two frequencies (f_1 and f_2), and E-CRLH lines to control output frequencies (f_1 and f_2) and their harmonics ($2f_1$ and $2f_2$) (Fig. 1d).

e) CRLH diplexer both at the input and output to control two frequencies (f_1 and f_2) and their harmonics (Fig. 1e).



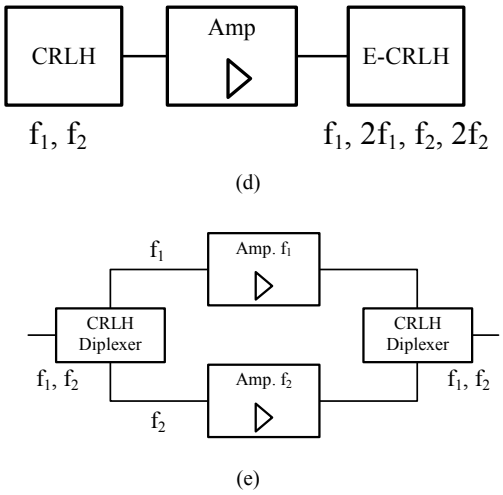


Fig. 1. Five solutions to implement dual band high efficiency amplifiers.

2. Composite Right/Left-Handed Transmission Line Metamaterials

The concept of composite right/left-handed (CRLH) transmission line meta-materials, introduced in [4] and extensively developed in successive papers, has been shown as a powerful tool for deep insight and efficient design of microwave devices. A CRLH meta-material is a practical transmission line meta-material structure which exhibits a left- handed (LH) band at lower frequencies and a right-handed (RH) band at higher frequencies, including a transition frequency where infinite-wavelength propagation occurs under a so-called balance condition.

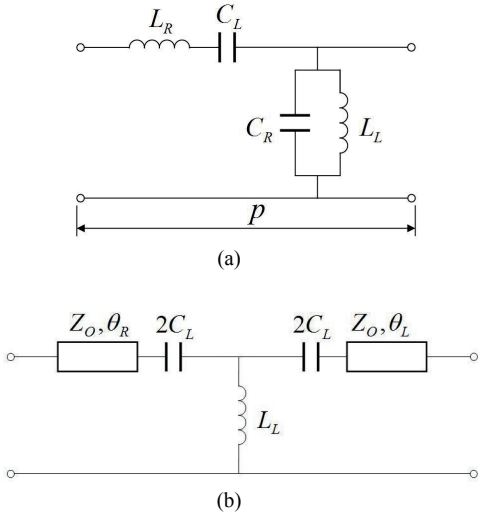


Fig. 2. CRLH structure: a) with lumped elements, b) with distributed and lumped elements.

Fig. 2 illustrates the equivalent circuit and its symmetrical model implemented with CRLH transmission lines. The calculus of the network components values are explained in detail in the reference [5]. A program to calculate the lumped element values for the design of the basic

CRLH transmission line structures in the high efficiency amplifiers has been developed. Recently the so called dual CRLH (D-CRLH) line has been developed as a tool that behaves as left-handed at higher frequencies and right-handed at lower frequencies. In this case the series-series configuration is changed by series-shunt configuration and the shunted shunt configuration by a shunted series one.

An Extended Composite Right/Left Handed transmission line (E-CRLH TL) is characterized by eight LC parameters (four C-CRLH - conventional CRLH- and four D-CRLH – dual-CRLH), which allow unprecedented diversity in the manipulation of the dispersion relation of the resulting TL structure. In particular, an E-CRLH TL meta-material, under an extended balance condition, exhibits two frequencies of infinite wavelength propagation. In addition, the E-CRLH is intrinsically a quad-band (arbitrary quadruplet of frequencies) structure, to provide the appropriate harmonic impedance to dual band high efficiency amplifiers. Fig. 3 illustrates the E-CRLH. The values of the components can be calculated by using other program developing to calculate these values according to the reference [7].

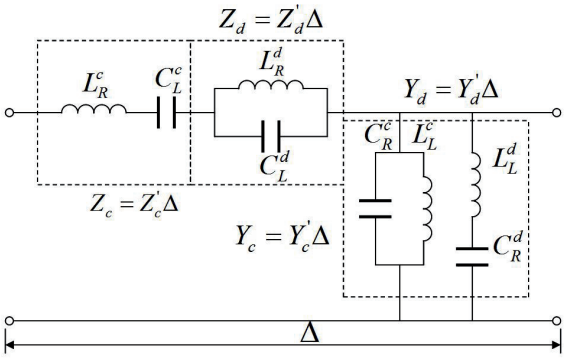


Fig. 3. E-CRLH structure according to the reference [7].

3. High Efficiency Power Amplifiers

One feasible solution to achieve dual frequency high efficiency amplifiers comes from [6], where a dual network to match the impedance at the fundamental and harmonics frequencies (mainly 2nd) has been used. If this termination were not implemented, the efficiency would decrease, while if more harmonic terminations were implemented, a higher efficiency could be obtained. The 3rd and 4th harmonic impedances have low effect on the efficiency and are omitted for most practical cases. (With the exception of the class F and F inverted where termination at third harmonic is very important).

Depending on the desired class for the high efficiency amplifier, different impedances associated to the corresponding harmonic frequency for that class will have to be matched. The most common classes are represented in Tab. 1, which describes the theoretical maximum efficiency that can be achieved, and the impedances to be presented at the fundamental frequency and second harmonic (and 3rd at class F and F inverted).

Class	Max. Output Efficiency η_{out}	Fundamental Impedance Z_{fo}	2nd Harmonic Impedance $Z_{\text{second harmonic}}$
A saturated	63.5%	Real	S.C.
A saturated and overexcited	80%	Real	S.C.
B	78.5%	Real	S.C.
C	100%	Real	S.C.
C saturated	100%	Real	S.C.
C_E	> 90%	Complex	O.C.
D	100%	Real	S.C.
E	100%	Complex	O.C.
F	88%	Real	S.C. (O.C. 3rd)
F-1	88%	Real	O.C. (S.C. 3rd)

Tab. 1. Classes of high efficiency power amplifiers (S.C = Short Circuit, O.C. = Open Circuit).

Due to the physical characteristics of bipolar transistors C class amplifiers are not suitable at microwave frequencies. Similar amplifying characteristics can be achieved with CE class amplifiers. This amplifying mode has its maximum efficiency when the load impedance (at fundamental frequency) is the one given (approximately) by the equation (1) and the impedance at 2nd harmonic is an open circuit.

$$R_p = 0.625 \cdot \frac{(V_{cc} - V_{sat})^2}{2 \cdot P_{out}}; \quad X_p = -\frac{1}{\omega \cdot C_{ob}} \tag{1}$$

where R_p and X_p are the equivalent parallel impedance of load.

In any case, it should be noted that this is an approach that have to be adjusted with a load-pull analysis, (to include the most significant parasitic of transistor output network and effect of overdrive). The input impedance will be the one that allows the maximum power transfer under the corresponding load conditions. The shapes of the currents and voltages have been carefully described in [12]. If the quotient between previous magnitudes is calculated the

load at the different harmonic frequencies is obtained. In this case it corresponds to open circuits at the harmonic frequency of the fundamental one.

$$Z(f_o) = \frac{1}{1/R_p + j/X_p}; \quad Z(n \cdot f_0 = \infty(o.c.) \tag{2}$$

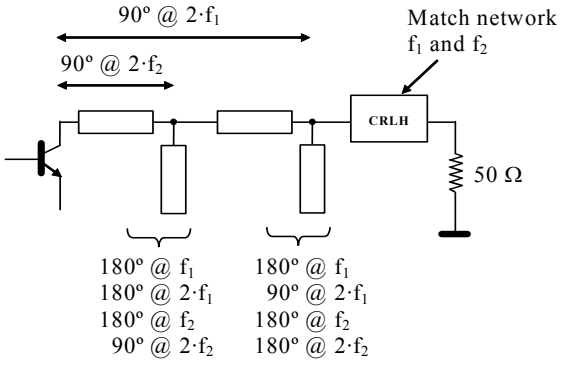
4. Dual Band Class CE Power Amplifier: Solutions Description

This section will provide the descriptions to implement a dual amplifier with meta-lines as presented previously. Then:

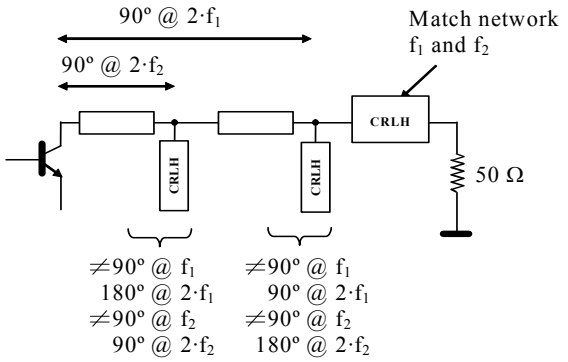
- Conventional lines are used with the architecture shown in Fig. 1a to implement the harmonic control. Traps (made with open or short circuited stubs) are implemented at $2f_1$ and $2f_2$ by means of conventional lines. This circuit can be implemented for a short circuit condition instead of an open circuit one.

  CRLH lines are used to implement the control harmonic in Fig. 1b. These two variants are shown in Fig. 4a and 4b. Traps are implemented at $2f_1$ and $2f_2$ by means of conventional lines and E-CRLH. In this way the output presents infinite impedance at these frequencies, working in CE class. Fig. 4 shows the schemes with open circuit. As in the previous case, depending on the configuration chosen, so will be the size of the resulting circuit.

  Optimal implementation is shown in Fig. 4a; however, this solution is difficult to perform because the o.c. traps must provide four performances at four frequencies (first and second harmonic of f_1 and f_2). For this reason a suitable solution is represented in Fig. 4b. For this solution, two among the four previous conditions are fulfilled while the other two only need to achieve a phase difference larger than 90º. This solution is easily implemented using CRLH lines.



(a)



(b)

Fig. 4. Proposed structure with conventional lines and CRLH lines for dual band CE amplifier.

- Fig. 1c replaces conventional lines with CRLH lines which can present arbitrary phase conditions at two frequencies. This solution is more compact, as it is shown in Fig. 5.

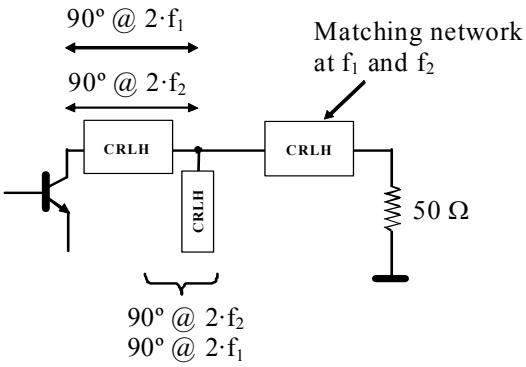


Fig. 5. Proposed structure with CRLH lines for dual band CE amplifier.

- The solution proposed in Fig. 1d is implemented with E-CRLH lines to satisfy four different output impedance conditions. In this solution the input network is a CRLH structure. The input impedance at the optimum desired frequencies are given by:

$$\begin{aligned} Z_{in}(f_1) &= R_{in1} + jX_{in1}, \theta_{ins1}, \theta_{inp1} \\ Z_{in}(f_2) &= R_{in2} + jX_{in2}, \theta_{ins2}, \theta_{inp2} \end{aligned} \tag{3}$$

where θ_{insx} and θ_{inpx} are the electrical lenghts of the equivalent transmission line, in series or parallel, to synthesize the input impedance at the corresponding x frequency (1 at f_1 and 2 at f_2 in Fig. 5).

The output network in the structure shown in Fig. 6 is based on an E-CRLH structure, establishing four impedance conditions

$$\begin{aligned} &Z(f_1) = R_{p1} + jX_{p1}, \theta_{s1}, \theta_{p1} \\ &Z(2 \cdot f_1) = \infty(o.c.), \theta_s = 90º, \theta_p = 90º \\ &Z(f_2) = R_{p2} + jX_{p2}, \theta_{s2}, \theta_{p2} \\ &Z(2 \cdot f_2) = \infty(o.c.), \theta s = 90º, \theta_p = 90º \end{aligned} \tag{4}$$

where θ_{sx} and θ_{px} are the electrical lengths of the equivalent transmission line in series or parallel to synthesize the output impedance at the corresponding x frequency (1 at f_1 and 2 at f_2 in Fig. 6). As discussed above, an E-CRLH line is able to meet four frequency conditions simultaneously. Therefore, with a single network the output impedance in class CE can be implemented.

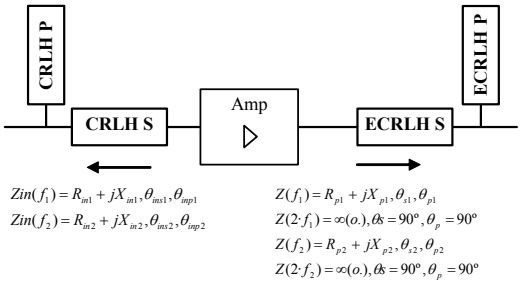
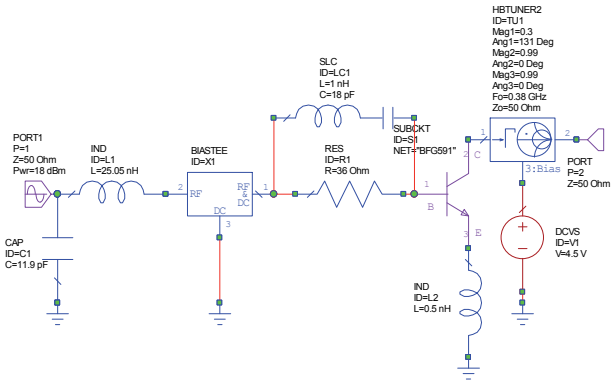


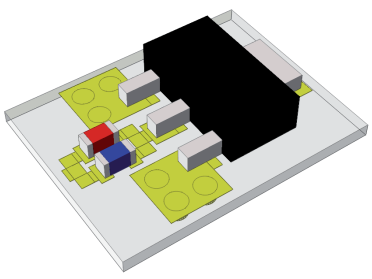
Fig. 6. Proposed structure with CRLH and E-CRLH lines for dual band CE amplifier.

- The solution presented in Fig. 1e solves the dual amplifier with two diplexers at the input and output. Each of the diplexers divides the signal towards the corresponding amplifier depending on the frequency. Both diplexers are implemented with CRLH lines [13], offering an optimal performance and a more compact design.

5. Practical Design and Simulations



(a)



(b)

Fig. 7. BFG591 transistor. a) Simulated electrical circuit with padding. b) Transistor padding detail view 3D.

For practical designs and simulations the TETRA (380 MHz) and GSM (960 MHz) bandwidths have been chosen. These frequencies are widely used in portable wireless handsets and are a good application example. The chosen transistor must satisfy the following criteria:

1. Single supply operation and low bias (<5V).
2. 26 dBm output capability at 1 GHz
3. Efficient operation (PAE>60%)
4. Availability of a large signal model
5. Available as discrete packaged device

The choice of the BFG591 transistor allows an easy modeling with the Microwave Office (AWR 2007). An input resistive padding (with frequency equalization) has been used to stabilize it at low frequencies (see Fig. 7). The separation between frequencies allows that the order of the CRLH networks would not be very high.

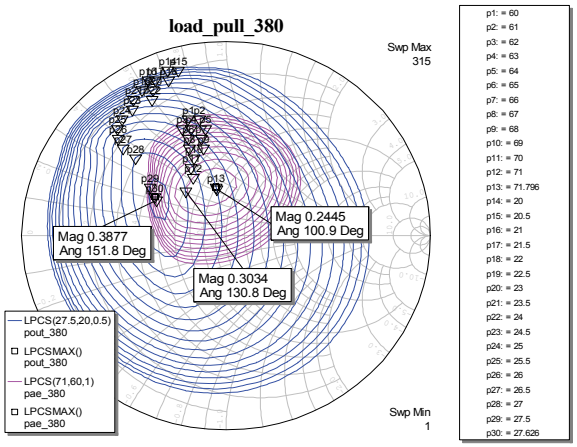


Fig. 8. 380 MHz Load Pull Simulation. PAE and P_{out} contours to determine the optimal load impedance.

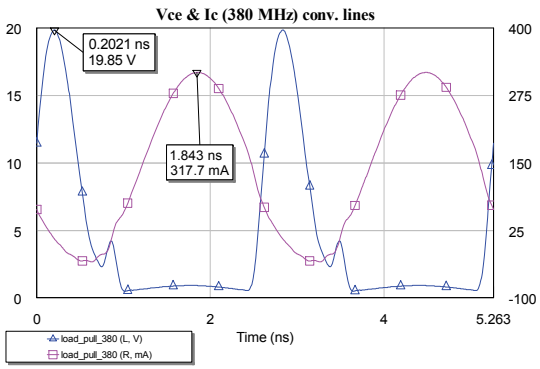


Fig. 9. Voltage V_{ce} and current I_c waveforms (380 MHz).

A load-pull analysis has been undertaken in order to select the necessary input and output impedance device. For this case it is usual to take a compromise between efficiency and output power. Figs 8 to 10 show the efficiency and power contours obtained for the device stabilized at design frequencies, 380 and 960 MHz. The signals waveforms V_{CE} and I_C of the implemented circuit with

these impedances, clearly demonstrate a typical behavior of the CE class at both frequencies (see Fig. 9 and 11).

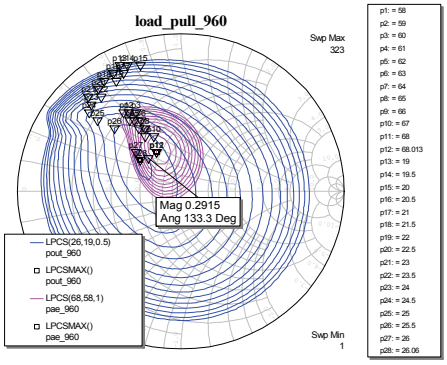


Fig. 10. 960 MHz Load Pull Simulation. PAE and P_{out} contours to determine optimal load impedance.

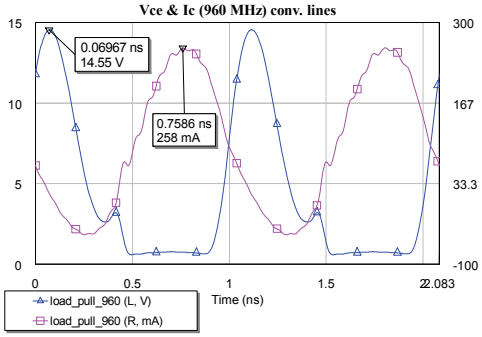


Fig. 11. Voltage Vce and current Ic waveforms (960 MHz).

After an optimization procedure the needed conjugate impedances at the working frequency with an open circuit at the second harmonics are presented in Tab. 2.

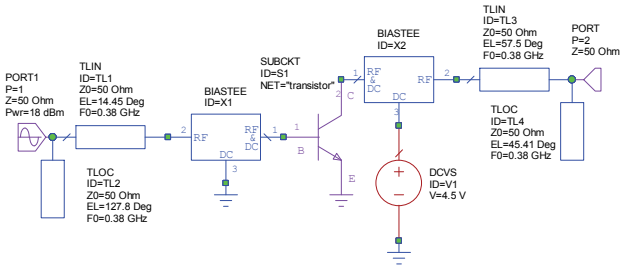
f_1=380 MHz		
PAE= 70.95%	DCRF=81.18%	P_{out}=27dBm
Vce=4.41·Vcc	Z_{in}=16.56-36.27j	Z_{out}=30.67-15.26j
f_2=960 MHz		
PAE= 66.64%	DCRF=92.77%	P_{out}=26dBm
Vce=3.23·Vcc	Z_{in}=13.01-4.12j	Z_{out}=30.95-14.33j

Tab. 2. Transistor values summary.

MHz / Line	f_1=380	$2f_1$=720	f_2=960	$2f_2$=1920
Input				
Series Line	14.45º	N.D.	27.75º	N.D.
Shunt Line	127.6º	N.D.	54.31º	N.D.
Output				
Series Line	57.5º	±90º	54.82º	±90º
Shunt Line	45.41º	±90º	39.3º	±90º

Tab. 3. Conventional lines values summary.

The simulated results with a transistor model including the actual components of resistors and capacitors show small differences respect to the presented results due to the corresponding package tolerances. Tab. 3 shows the values of the results obtained by conventional lines calculation.



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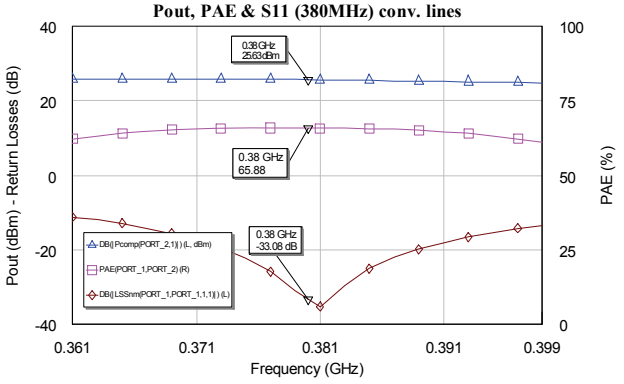

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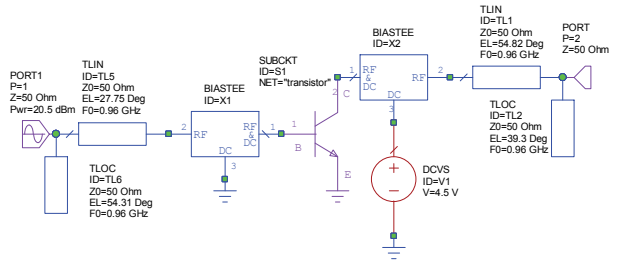
Fig. 12. Conventional Lines amplifier: Output power, PAE and return loss (380 MHz).



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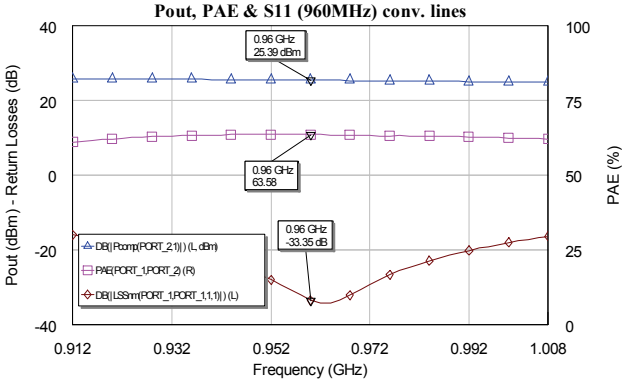


(b)

Fig. 13. Conventional Lines amplifier: Output power, PAE and return loss (960MHz).

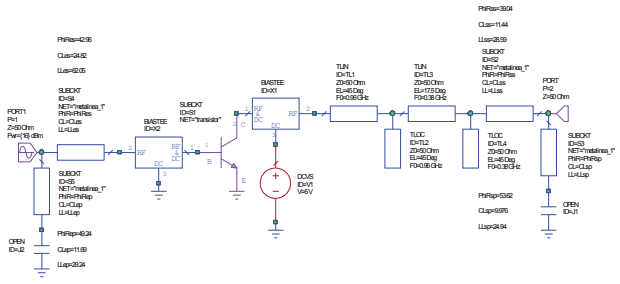
5.1 Design with CRLH Meta-Lines and Conventional Lines

In this case the input networks (with lumped and distributed components) are synthesized with CRLH transmission lines (only two phase conditions are needed). The obtained values, according to Fig. 2b, are shown in Tab. 4 (capacities in pF, inductances in nH, and lengths referred to electrical degrees at f_1=380 MHz).

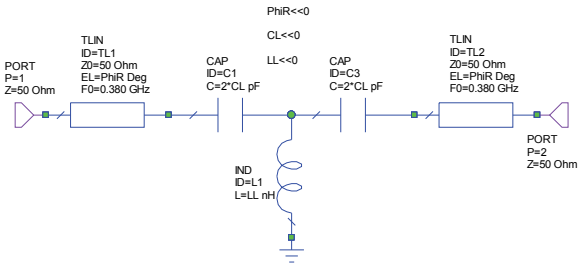
	C_L	L_L	Length
CRLH S	8.46	21.16	41.26º
CRLH P	13.5	33.69	53.26º

Tab. 4. Input CRLH line. Values summary Conventional Lines amplifier: Output power, PAE and return loss (960 MHz).

Simulated circuit is shown in Fig. 14. This circuit shall provide a dual frequency performance so that at each of the two working frequencies, the transistor input and output impedances will be the typical of a CE class.



(a)



(b)

Fig. 14. CRLH & Conventional Lines dual amplifier: Circuit (a) and CRLH line detail (b).

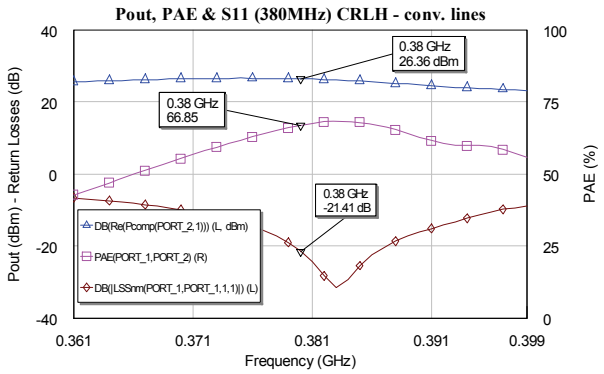


Fig. 15. CRLH & Conventional Lines dual amplifier: Output power, PAE and return loss (380 MHz).

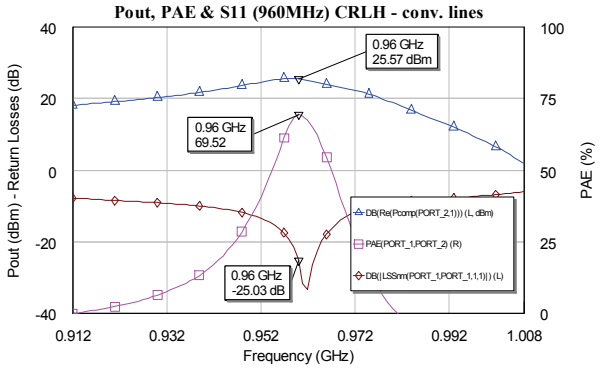


Fig. 16. CRLH & Conventional Lines dual amplifier: Output power, PAE and return loss (960MHz).

The results at both frequencies are shown in Fig. 15 and 16. Two problems arise with this circuit: its narrow bandwidth, especially at the higher frequency and its sensitivity with the tolerance component.

5.2 Design with CRLH and E-CRLH Meta-Lines

In this case the output networks are synthesized with E-CRLH lines (where four phase conditions are necessary at both-fundamental and its respective harmonics), so the joint amplifier-network performance corresponds to a CE class at both operating frequencies. In particular, a metamaterial E-CRLH transmission line, under a widespread equilibrium condition, has two spread frequencies of infinite wavelength. In addition, the E-CRLH structure is inherently a four-band (where the four frequencies are arbitrarily chosen).

To determine the values of all components, four equations with four unknown variables (frequencies) must be solved by using the equation (5).

$$\Phi_c = \frac{(\omega^2 - \omega_{1e}^2)\cdot(\omega^2 - \omega_{2e}^2)}{\omega\cdot\omega_R^c(\omega^2 - \omega_o^2)}. \tag{5}$$

Frequencies ω_{1e} and ω_{2e} are two balanced transition frequencies that satisfy equations (6) and (7).

$$\sqrt{\omega_{1e}\cdot\omega_{2e}} = \omega_o \tag{6}$$

$$\omega_R^c = \frac{1}{\sqrt{L_R^c\cdot C_R^c}} \tag{7}$$

The frequencies of the system have been numerically obtained and the results are used to calculate the components values. The order (number of stages of the CRLH transmission line) in both structures must be as low as possible in order to minimize the losses.

In other words, these lines allow determining four desired electric lengths at four selected frequencies. The input network values (capacity in pF, inductances in nH and lengths referred to electrical degrees at f_1=380 MHz) are

the same as in the previous case (Tab. 4), whereas the values in Tab. 5 correspond to the output E-CRLH lines (according to Fig. 3).

E-CRLH S	C_R^C=1.34	L_R^C=3.35	C_L^C=10.25
	C_R^D=15.9	L_R^D=39.7	C_L^D=0.864
E-CRLH P	C_R^C=1.38	L_R^C=3.45	C_L^C=9.924
	C_R^D=0.99	L_R^D=2.48	C_L^D=13.78

Tab. 5. Values for the output E-CRLH line.

The resulting circuit is implemented by blocks to look for the optimal order value. An example of block and the corresponding E-CRLH line is shown in Fig. 17.

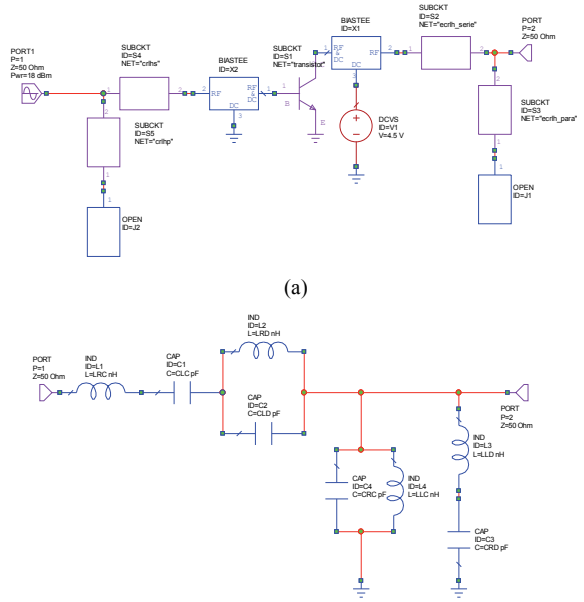


Fig. 17. E-CRLH dual amplifier: Circuit (a) and E-CRLH line detail (b).

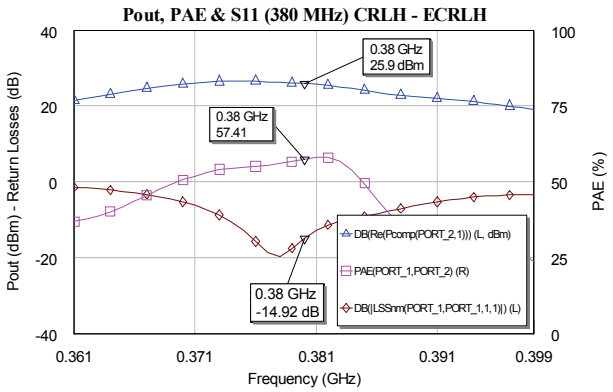


Fig. 18. E-CRLH dual amplifier: Output power, PAE and return loss (380 MHz).

Fig. 18 and 19 show the output power, the power added efficiency (PAE) and the return losses at the two working frequencies. The PAE is close to 60 % at the two working frequencies but with a very narrow band at 960 MHz. The sensitivity problems still maintains, especially when compared with the results of Fig. 13b. The same problems can be seen for the 380 MHz band when compared with Fig. 12b.

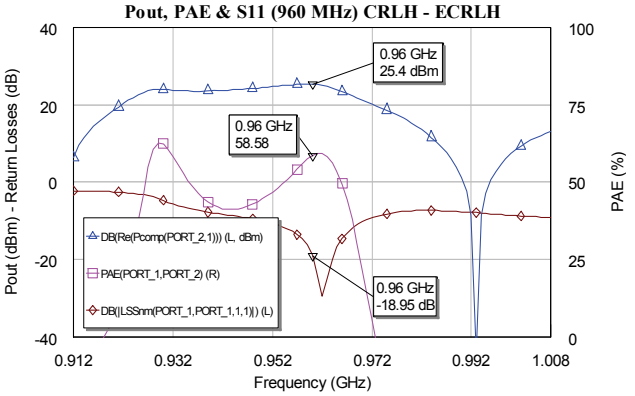


Fig. 19. E-CRLH dual amplifier: Output power, PAE and return loss (960 MHz).

Fig. 20 and 21 show the waveforms resulting from simulation for current and voltage in the amplifier, working at 380 and 960 MHz, respectively. Both waveforms correspond to the response of a CE class amplifier being the voltage working cycle very lower than 50%.

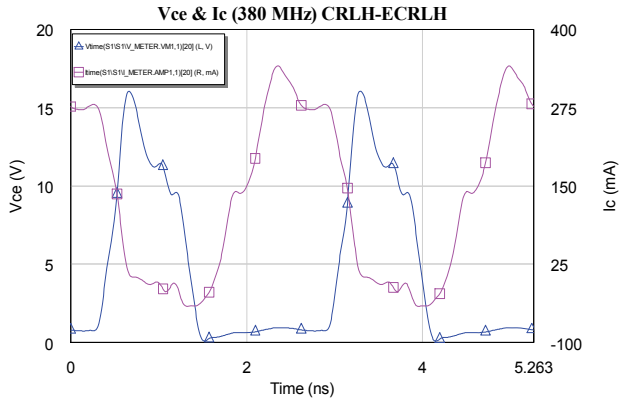


Fig. 20. E-CRLH dual amplifier: voltage Vce and current Ic waveforms (380 MHz).

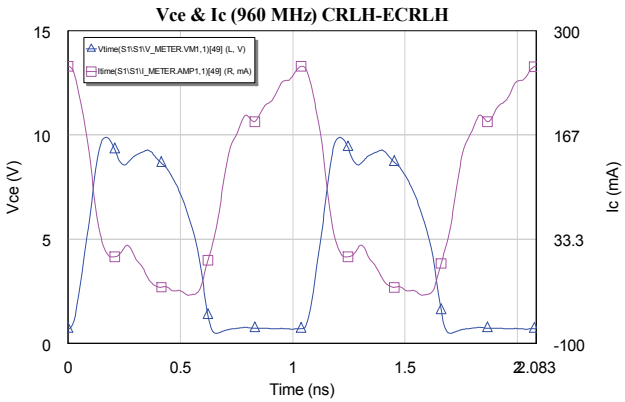


Fig. 21. E-CRLH dual amplifier: voltage Vce and current Ic waveforms (960 MHz).

5.3 Design with CRLH Diplexers

For the realization of this design authors have designed a CRLH diplexer [13]. Fig. 22 shows the operation of the CRLH diplexer with ideal components. A behavior according to the results of design is seen in Fig. 22. Port 2 works at 380 MHz while port 3 works at 960 MHz.

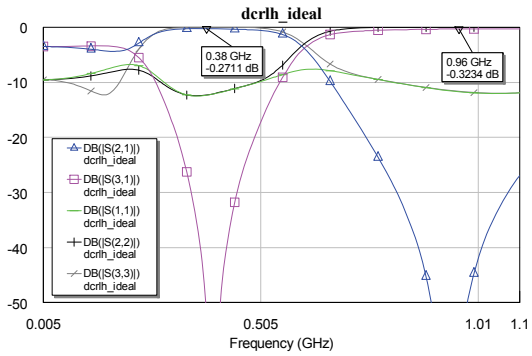
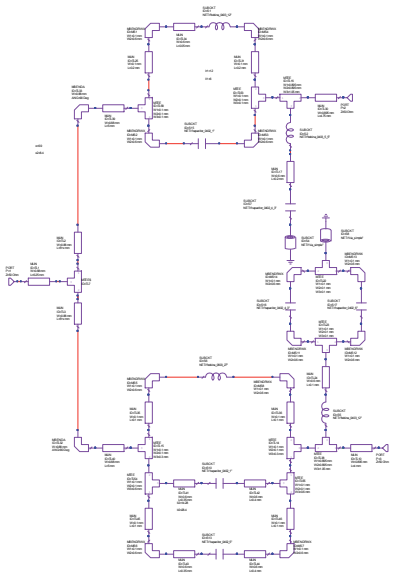
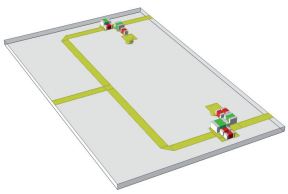


Fig. 22. Diplexer. Return loss and transmission loss in dB.

If the ideal elements are replaced by complex models (see Fig. 23), an acceptable behavior is observed (see Fig. 24). The difference with previous ones is very slightly.



a)



b)

Fig. 23. Physical simulated Diplexer. Schematic a) and 3D view b).

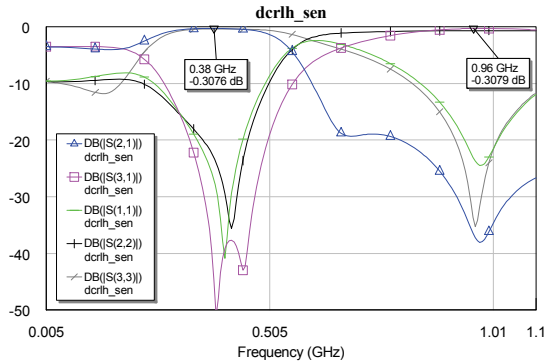
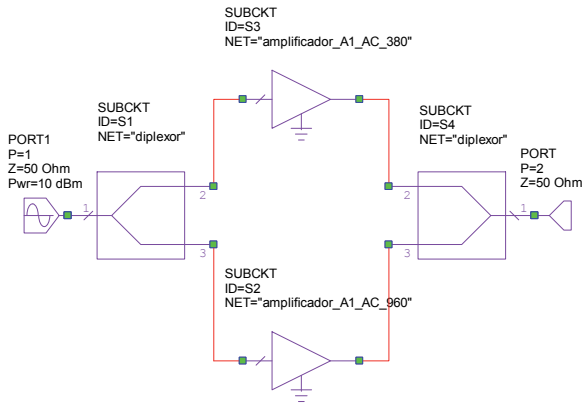


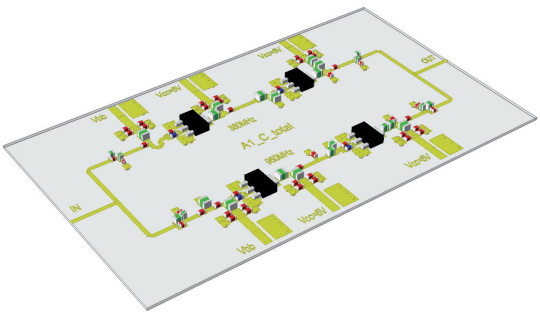
Fig. 24. Physical simulated Diplexer. Return loss and transmission loss in dB.

The diplexer is very robust against the tolerance components. A complete dual amplifier (see Fig. 25) where each amplifier branch is composed of a driver and a power amplifier has been realized.

In the amplifier simulations, at each frequency (Fig. 26 and 27) the PAE represented takes into account the power consumed by the quiescent branch (20 mA in the 960 MHz branch, and 10 mA in the 380 MHz branch). Thus, this PAE value is actually higher, as it is evidenced in the individual simulations (Fig. 28 and 29). The PAE improves up to near 9% at 380 MHz and 5% at 960 MHz.



(a)



(b)

Fig. 25. Physical simulated Dual-Amplifier circuit. Schematic (a) and 3D view (b).

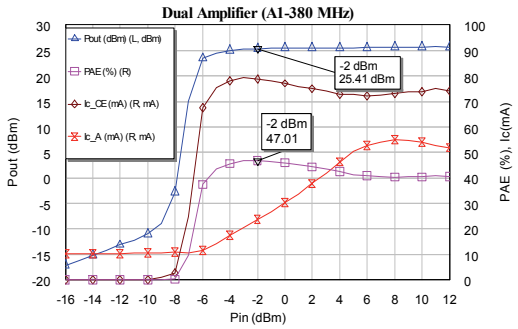


Fig. 26. Dual amplifier (A1 with diplexer): Simulated output power, PAE, driver current (Ic_A) and stage output current (Ic_CE) at 380 MHz.

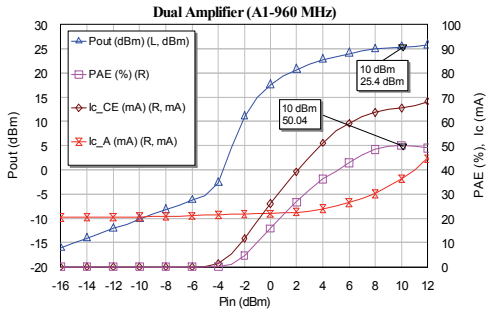


Fig. 27. Dual amplifier (A1 with diplexer): Simulated output power, PAE, driver current (Ic_A) and stage output current (Ic_CE) at 960 MHz.

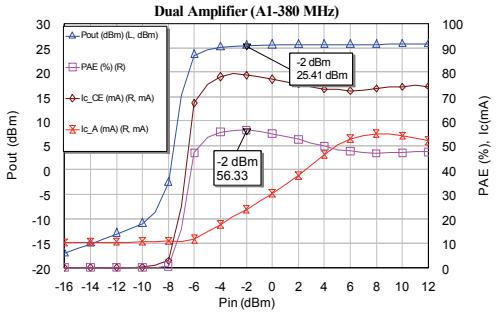


Fig. 28. Amplifier (A1 with diplexer): Simulated output power, PAE (without quiescent branch consumption), driver current (Ic_A) and stage output current (Ic_CE) at 380 MHz.

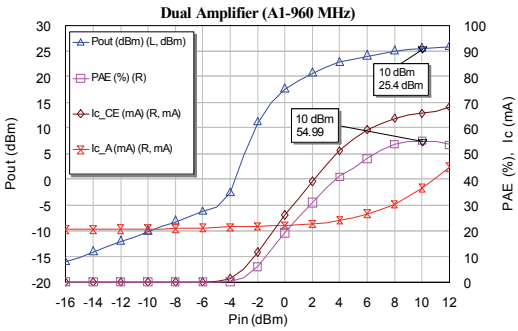


Fig. 29. Amplifier (A1 with diplexer): Simulated output power, PAE (without quiescent branch consumption), driver current (Ic_A) and stage output current (Ic_CE) at 960 MHz.

The driver has been optimized by using a load as a final stage, instead of a classic output impedance of 50 Ohms. This improves the overall efficiency (the optimized circuit is called A2 in Fig. 30 and 31). In the figures the PAE shown corresponds to the set of the amplifier and includes the driver consumption. The quiescent branch consumption has not been considered, while the represented collector efficiency is only referred to the output power amplifier of the active branch: neither the driver nor the quiescent branch consumptions are included. The PAE is increased in more than 10 % vs. the A1 amplifier at 380 MHz. The collector efficiency obtained at 960 MHz is near to 90%.

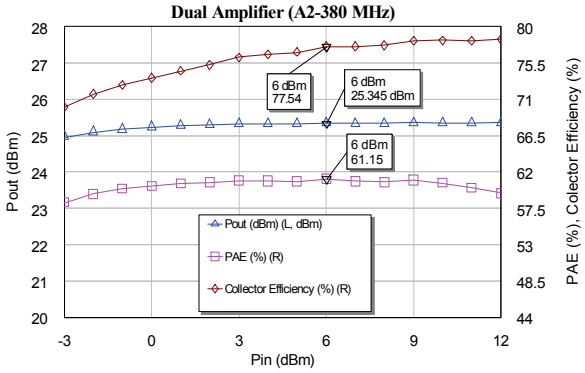


Fig. 30. Amplifier (A2 with diplexer): Simulated output power, PAE and Collector Efficiency (380 MHz).

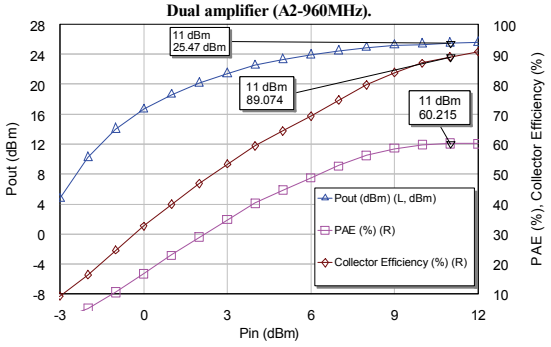


Fig. 31. Amplifier (A2 with diplexer): Simulated output power, PAE and Collector Efficiency (960 MHz).

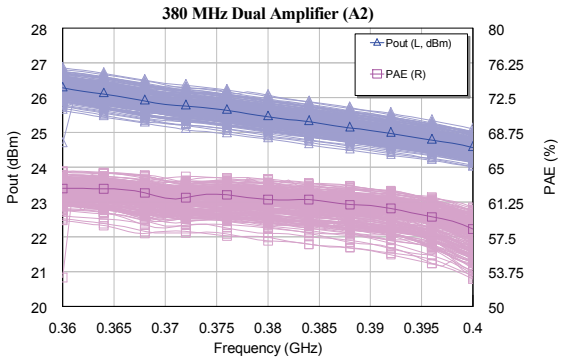


Fig. 32. Dual amplifier (A2 with diplexer): Statistical sensitivity study of the output power and PAE (380 MHz).

Finally Fig. 32 and 33 show the study of the statistical sensitivity at both frequencies after 200 iterations with uniform statistical distribution [14], ±5% tolerance for capacitors, inductors and transistors, and ±1% for substrate. The tolerance performance is good, especially for the interesting input power, where the transistor output is already saturated.

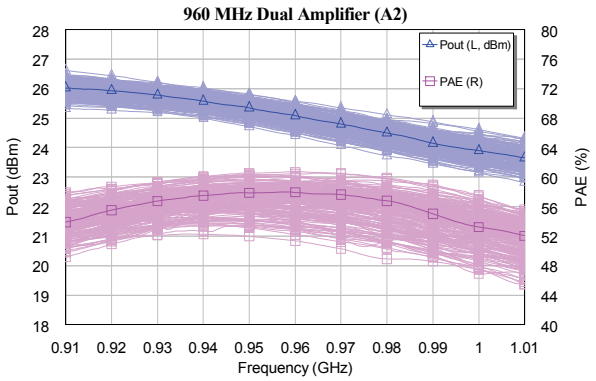


Fig. 33. Dual amplifier (A2 with diplexer): Statistical sensitivity study of the output power and PAE (960 MHz).

Fig. 32 and 33 also show the kindness of the design, presenting a great robustness performance with regard to other CRLH topologies. The other structures are more sensitive so their studies are not presented.

Tab. 6 shows a summary between the different simulated circuits, where one can see that all the alternatives offer high efficiency. The choice of one or the other depends on the requirements for each use and, mainly, from the sensitivity to the tolerance of the components.

	380 MHz		960 MHz	
	PAE (%)	$\eta_{out(\%)}$	PAE (%)	η_{out} (%)
Individual Amp. conv. lines	65.9	79.5	63.6	91
CRLH+ conv. Lines	66.9	73.6	69.5	87.6
CRLH+ECRLH	57.4	68	58.6	86
CRLH Diplexers	62	80	60	89

Tab. 6. Approximate PAE and efficiency collector values of simulated amplifiers.

The circuit with CRLH and conventional lines presents a higher PAE, but the design becomes more complex and very sensitive to the components tolerance. The circuit with E-CRLH is more compact and easier to implement but, also, very sensitive to the components tolerance. Finally, the amplifier with diplexers has the great advantage of its easiest design and individual control of frequencies and its better statistical sensitivity at a price of a less compact design. For that reason, this last topology has been manufactured. Fig. 34 shows a photo of the proposed high efficiency amplifier based on a diplexer topology.

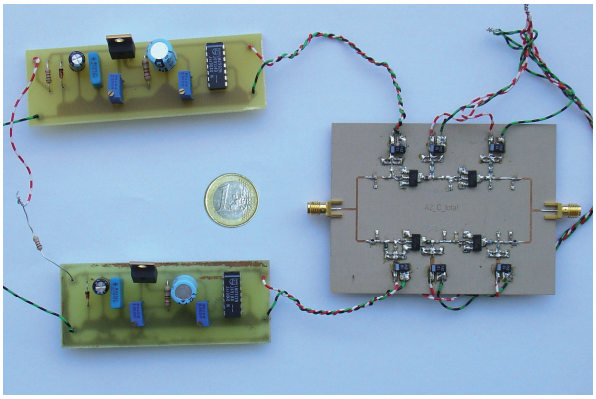


Fig. 34. Photo of the manufactured high efficiency amplifier based on a D-CRLH line diplexer.

Tab. 7 shows the experimental results obtained for this architecture. The efficiency results show good agreement with the simulations.

	380 MHz		960 MHz	
	PAE (%)	$\eta_{out(\%)}$	PAE (%)	η_{out} (%)
CRLH Diplexers (simulation)	62	80	60	89
CRLH Diplexers (experimental)	64.5	71.2	61.2	91.2

Tab. 7. Approximate PAE and efficiency collector values of the diplexer D-CRLH high efficiency amplifier.

6. Conclusions

In this paper the authors have presented several methods for designing dual band high efficiency power amplifiers. A comparison with the results for individual amplifiers has been realized demonstrating the viability of these circuits, since they can provide high efficiency and compact design by means of using CRLH lines.

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