Feedback Compensation Algorithm for BPSK/QPSK Carrier Synchronization

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Abstract. *This paper deals with carrier synchronization problem in coherent communication system, such as BPSK and QPSK. First, this paper surveys and analyzes currently existing carrier synchronization algorithms and relevant receiver structures. After an analysis of those methods, a novel algorithm called feedback compensation is proposed, including the receiver structures based on this new synchronization algorithm. This new algorithm can not only simplify the signal processing stage but also decouple the demodulator and carrier synchronization module. At last, FPGA implementation results are presented and discussed.*

Keywords

Carrier synchronization, feedback compensation, receiver structure, FPGA based implementation.

1. Introduction

In coherent digital communication systems, carrier synchronization is an essential part in the implementation of receiver structure. With carrier synchronization, the carrier frequency can be recovered in the receiver and the carrier phase can also be tracked. For BPSK and QPSK scheme, several carrier synchronization techniques are available. These techniques can be classified to two kinds. In the feedback technologies, a Phase Lock Loop (PLL) scheme is utilized and the carrier phase is tracked automatically by the loop. And for the feed-forward technologies, estimation theory is used to estimate the phase error. However, in the existing receiver structures, carrier synchronization module and demodulator module are coupled together, or the signal processing is too complex. This paper intends to develop a new feedback compensation carrier synchronization technique which can simplify the signal processing stage and decouple the demodulator and carrier synchronization module.

This feedback compensation algorithm can be easily implemented on a digital IF or an analog IF platform. For convenience, the formulas are in the form of analog signal.

2. Existing Synchronization Algorithms

2.1 Feedback Control Algorithm

Costas Loop is discussed in [1], [2], [3] and [4]. It is a classical BPSK carrier synchronization algorithm, as shown in Fig. 1, which indicates that Costas Loop is a special case of PLL (Phase Lock Loop). The specialized phase detector, which is used to eliminate the information component in the modulated signal, makes it different from the classical PLL that simply employs a multiplier as a phase detector. Ignoring the noise, the BPSK error signal $e(t)$ is given in (1)

$$e(t) = \frac{1}{8} A^2 \sin(2\theta) . \tag{1}$$

This error signal $e(t)$ is filtered by the loop filter, whose control output is applied to VCO (Voltage Control Oscillator). Control voltage changes the VCO frequency in a direction that reduces the phase error between the input signal and VCO output.

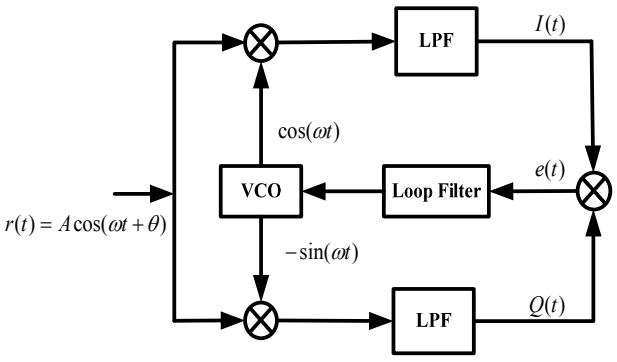

Fig. 1. Costas Loop for BPSK.

For QPSK carrier synchronization, feedback control Loop can be reconstructed as shown in Fig. 2. As the complexity of signal constellation increases, more complex phase detector is employed to eliminate the information component. Refer to [4] for detail of the loop in Fig. 2.

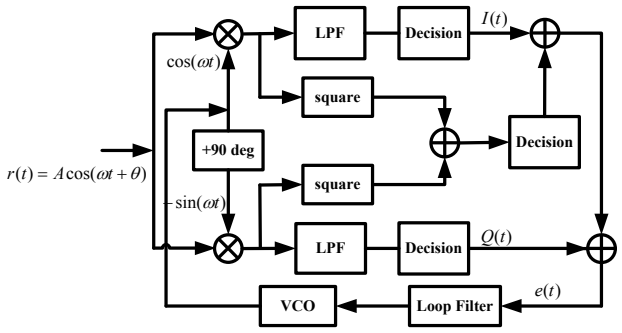

Fig. 2. Costas Loop for QPSK.

Ignoring the noise, the QPSK error signal is given in (2)

$$e(t) = \mathrm{sgn}(\sin 4\theta). \tag{2}$$

Another kind of coherent receiver is the M-power receiver, discussed in [5]. For BPSK, M-power loop can be simplified as a square loop, as in Fig. 3.

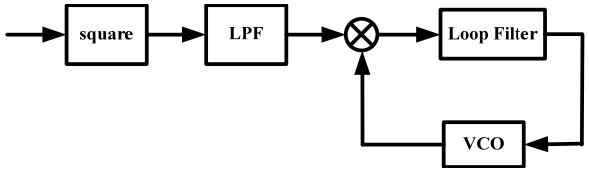

Fig. 3. Square loop for BPSK.

The M-power loop can also be used in coherent demodulation for M-array signal receiver. A MPSK M-power loop is shown in Fig. 4.

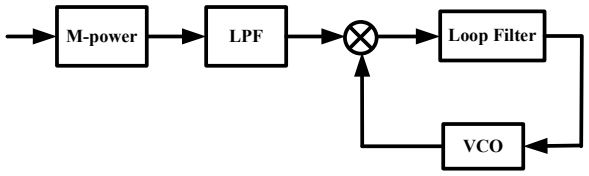

Fig. 4. M-power loop for MPSK.

We can draw a conclusion from the review of several feedback carrier synchronization algorithms: Both the Costas and M-power loop utilize the PLL scheme to implement carrier synchronization. A VCO is used to generate a coherent carrier output. For this reason, these algorithms can be classified as feedback control algorithms. The feedback control algorithms need an error signal to control LO (Local Oscillator), thus mix the carrier synchronization and demodulator module together. This mixture not only confuses the conceptions of demodulation and synchronization, but also increases the complexity of the receiver implementation. For example, modern receivers not only include a carrier phase synchronization module, but usually also a carrier frequency synchronization module. Under this case, two error signals are used to control the VCO. Apparently, these error signals make the design more complex and hard to analyze.

Another problem in implementation of the feedback control algorithms is the position of ADC (Analog to Digital Converter). It's better to directly sample IF signal rather than base-band signal. Because if base-band signal sampled, an extra DAC (Digital to Analog Converter) is needed to convert the digital error signal to analog error signal, which will be used to control the analog VCO. This obviously increases the complexity of the receiver.

Although having the weak points, the feedback control algorithms also have an excellent advantage: The computing process of error signal is easy. It doesn't need complex functions such as sin( ) or cos( ). The feedback loop can acquire and track the phase of the received signal automatically.

2.2 Feed-Forward Compensation Algorithm

In [6], [7], [8] and [9], the conception of feed-forward compensation method is introduced. And in [10], the feed-forward compensation algorithm is discussed in detail. The receivers using feed-forward compensation algorithm can be constructed as in Fig. 5.

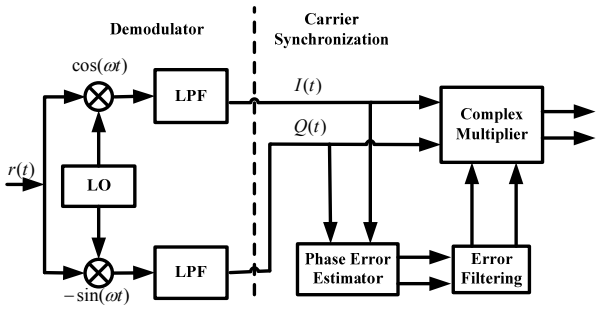

Fig. 5. Feed-forward compensation loop.

The feed-forward loop utilizes the phase error estimator to estimate the phase error directly. After filtering, phase error signal is used to compensate the distorted $I(t)$ and $Q(t)$. Those signal processing stages construct a feed-forward loop. Thus, it can be classified as a feed-forward compensation algorithm.

Apparently, the structure in Fig. 5 has divided the receiver into two separated modules. One is demodulator and the other is carrier synchronization. Furthermore, the designer doesn't need pay much attention to whether sampling the IF signal or sampling the zero-IF signal, because neither of these two solutions will increase more complexity.

However, unlike feedback control loop utilizing PLL scheme, feed-forward loop should estimate the phase error precisely. Thus, phase error estimator will introduce very complex function such as sin( ), cos( ) and so on, which greatly increase the complexity of the receiver.

3. Feedback Compensation Algorithm

This paper intends to develop a new feedback compensation algorithm, which can take advantages of

both feedback control loop and feed-forward compensation loop.

The feedback compensation algorithm for BPSK is shown in Fig. 6. This receiver structure has obviously two modules for carrier synchronization. Demodulator is used to downconvert the IF signal into base-band signal, and carrier synchronization is used to compensate the phase error.

For DSP implementation, the ADC converter may directly sample the received IF signal $r(t)$ to construct a digital-IF receiver or it may sample the zero-IF signals $I(t)$ and $Q(t)$ to construct an analog-IF receiver. Like the feed-forward loop, neither of these solutions will increase more complexity.

In the following description, we can find this feedback compensation also employs PLL scheme. This scheme enables the loop lock on the phase of the received signal automatically without complex signal processing.

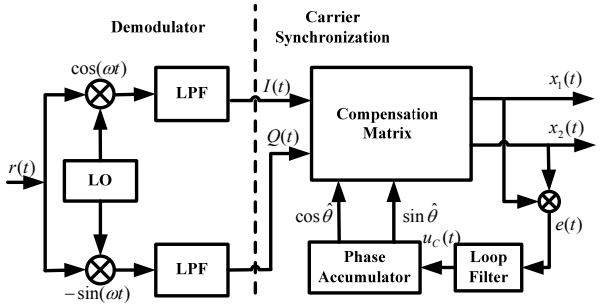

Fig. 6. Feedback compensation algorithm blocks for BPSK.

Let $r(t)$ indicate the received signal, ignoring the noise

$$r(t) = A\cos(\omega t + \theta) \tag{3}$$

where $A \in \{-1,+1\}$ for BPSK.

Signals from the mixer are fed to the LPF, obtaining $I(t)$ and $Q(t)$.

$$I(t) = A\cos(\omega t + \theta)\cos(\omega t) = \frac{1}{2}A[\cos(2\omega t + \theta) + \cos\theta] \tag{4}$$

$$Q(t) = -A\cos(\omega t + \theta)\sin(\omega t) = \frac{1}{2}A[-\sin(2\omega t + \theta) + \sin\theta] \tag{5}$$

After low pass filtering, $I(t)$ and $Q(t)$ can be rewritten as

$$I(t) = \frac{1}{2}A\cos\theta, \tag{6}$$

$$Q(t) = \frac{1}{2}A\sin\theta. \tag{7}$$

Error detection matrix uses $I(t)$ and $Q(t)$ as input to generate error signal,

$$x_1(t) = I(t)\cos\hat{\theta} + Q(t)\sin\hat{\theta}, \tag{8}$$

$$x_2(t) = Q(t)\cos\hat{\theta} - I(t)\sin\hat{\theta}. \tag{9}$$

Rewrite (8) and (9) in matrix form,

$$\begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} = \begin{pmatrix} I(t) & Q(t) \\ Q(t) & -I(t) \end{pmatrix} \begin{pmatrix} \cos\hat{\theta} \\ \sin\hat{\theta} \end{pmatrix}. \tag{10}$$

For BSPK, the compensation matrix is

$$\begin{pmatrix} I(t) & Q(t) \\ Q(t) & -I(t) \end{pmatrix}.$$

Thus,

$$e(t) = \frac{1}{8}A^2\sin[2(\theta - \hat{\theta})] = \frac{1}{8}\sin 2\theta_e. \tag{11}$$

Equation (11) is not only suitable for constant phase error, but can also be used in slowly changed phase error signal. For a slowly changed phase error signal, equation (11) can be rewritten as,

$$e(t) = \frac{1}{8}\sin 2\theta_e(t). \tag{12}$$

The mathematical model of phase accumulator is described in (13) and (14),

$$\hat{\theta}(t) = \int_0^t K_C u_C(x)dx, \tag{13}$$

$$u_C(t) = \frac{d\hat{\theta}(t)}{dt}. \tag{14}$$

$u_C(t)$ can also be considered as a filtering result of $e(t)$, as described in (15)

$$u_C(t) = F(p)e(t) = \frac{1}{8}\sin 2\theta_e(t)F(p). \tag{15}$$

p denotes $\frac{d}{dt}$, and $F(p)$ the system function for loop filter.

Then we can obtain the loop equation in (16),

$$\frac{1}{8}\sin 2\theta_e(t)F(p) = p\hat{\theta}(t). \tag{16}$$

From (16), we can find this feedback compensation loop has an identical mathematical model with the classical PLL. So, the performance analysis for classical PLL is also valid for this feedback compensation loop. There is also a difference: classical PLL employs a VCO to implement the phase accumulator. The physical character of VCO makes the frequency, not the phase, become the controlled variable. Phase accumulator is only a mathematical model of VCO in the system transfer function. While in the feedback compensation loop a real phase accumulator is in use. The error signal can directly affect the change of the phase. This difference makes the feedback compensation

loop is especially suitable for DSP implementation in digital domain, not available in analog domain.

With the same compensation matrix for QPSK, the receiver structure in Fig. 6 can be easily applied in QPSK coherent receiving.

In QPSK mode, $r(t)$ should be rewritten in (17)

$$r(t) = A_I \cos(\omega t + \theta) - A_Q \sin(\omega t + \theta) \tag{17}$$

where $A_I, A_Q \in \{-1,+1\}$.

After low pass filtering,

$$I(t) = \frac{1}{2} A_I \cos\theta - \frac{1}{2} A_Q \sin\theta, \tag{18}$$

$$Q(t) = \frac{1}{2} A_I \sin\theta + \frac{1}{2} A_Q \cos\theta. \tag{19}$$

With the same compensation matrix,

$$x_1(t) = \frac{1}{2} A_I \cos(\theta - \hat{\theta}) - \frac{1}{2} A_Q \sin(\theta - \hat{\theta}), \tag{20}$$

$$x_2(t) = \frac{1}{2} A_I \sin(\theta - \hat{\theta}) + \frac{1}{2} A_Q \cos(\theta - \hat{\theta}). \tag{21}$$

Matrix output is further processed as

$$x_1^2(t) = \frac{1}{4} - \frac{1}{4} A_I A_Q \sin[2(\theta - \hat{\theta})], \tag{22}$$

$$x_2^2(t) = \frac{1}{4} + \frac{1}{4} A_I A_Q \sin[2(\theta - \hat{\theta})], \tag{23}$$

$$x_1(t) x_2(t) = \frac{1}{4} A_I A_Q \cos[2(\theta - \hat{\theta})]. \tag{25}$$

Then, we can obtain the error signal in (26),

$$[x_2^2(t) - x_1^2(t)] x_1(t) x_2(t) = \frac{1}{16} \sin[4(\theta - \hat{\theta})]. \tag{26}$$

According to (26), QPSK compensation loop can be constructed as in Fig. 7.

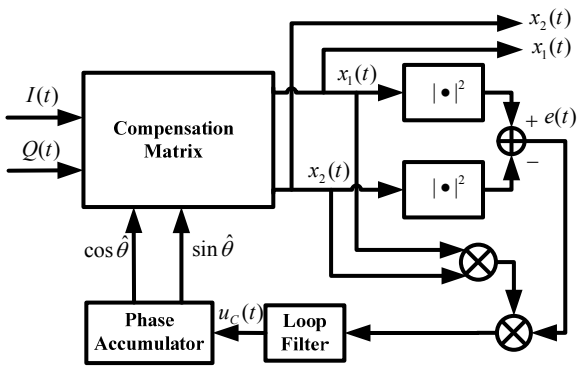

Fig. 7. Compensation loop for QPSK.

4. FPGA Based Implementation

A BPSK feedback compensation loop is implemented on an Altera Stratix II EP2S180 FPGA. The function block of feedback compensation loop is shown in Fig. 8 and Fig. 9. Fig. 8 is the implementation of demodulator and Fig. 9 is the carrier synchronization block.

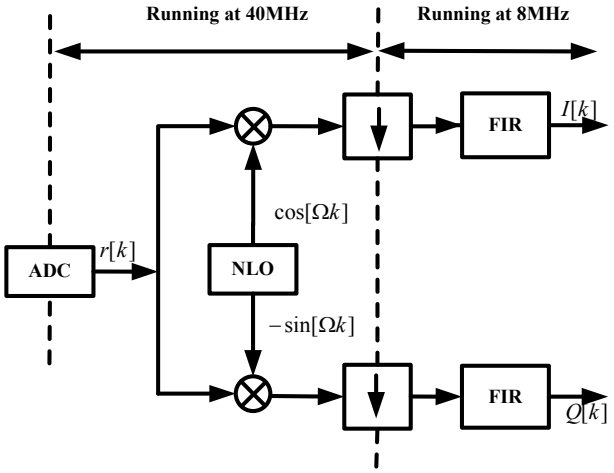

Fig.8. FPGA implementation of demodulator.

Input signal has a carrier frequency of 10 MHz, and symbol rate is 2M symbols per second. ADC is running at 40 MHz. Sampled digital signal is mixed with Numeric Local Oscillator (NLO). Before filtering, a down sample converter is needed to slow down the running frequency for following stages. Furthermore, this down sample converter changes the sampling frequency from 20 samples per symbol to 4 samples per symbol, which decreases the FIR order remarkably.

Fig. 9 shows the FPGA implementation of the carrier synchronization block.

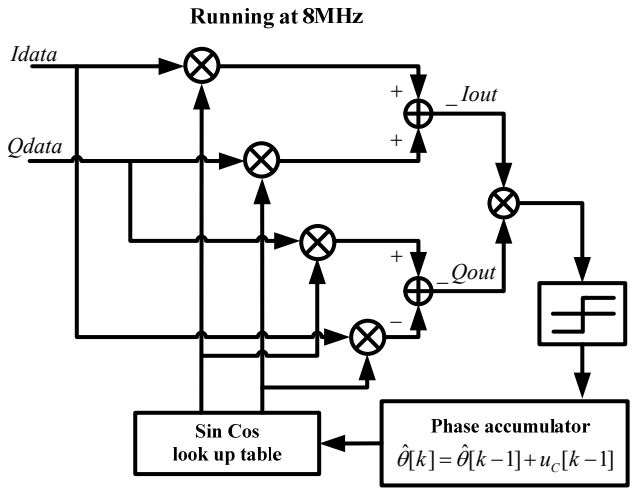

Fig. 9. FPGA implementation of BPSK carrier synchronization.

The whole carrier synchronization block is running at 8 MHz. For convenience of implementation, the loop filter is omitted, and then the transfer function of loop filter is $F(p) = 1$. And instead of sine phase detector, a rectangular phase detector is employed, which can greatly decrease the implementation complexity.

For FPGA based multirate signal processing, clock distribution is a crucial problem for the entire design. In this carrier synchronization design, the clock distribution strategy is shown in Fig. 10.

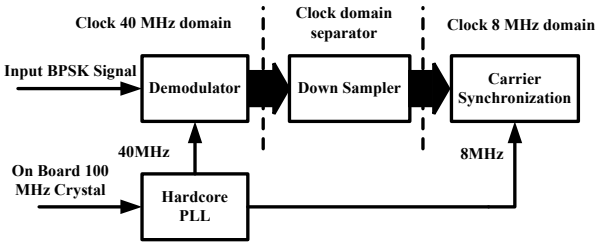

Fig. 10. Clock distribution strategy.

On-chip Hardcore PLL is used as a frequency synthesizer. PLL synthesizes a 40MHz clock to drive the demodulator and ADC, and an 8MHz clock to drive the carrier synchronization block. The two clock domains are separated by a clock domain separator. This clock domain separator is actually a DPRAM (Dual Port RAM).

Usually, the synchronization result can be watched on an oscilloscope. For convenience, a SigTap II Logic Analyzer tool integrated in the Quartus II IDE is used to watch the synchronization result.

Fig. 11 is the waveform of the BPSK signal.

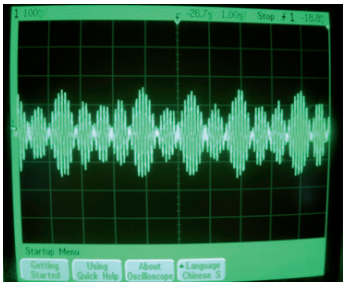

Fig. 11. Input modulated signal.

The synchronization result from SigTap II Logic Analyzer is shown in Fig. 12.

Idata and Qdata are directly demodulated signal without any compensation. The nonzero phase error θ_e makes $I(t) = A\cos\ \theta_e$ and $Q(t) = -A\sin\ \theta_e$. _Iout and _Qout are base-band signals after feedback compensation. In theory for BPSK scheme, a zero phase error makes $I(t) = A$ and $Q(t) = 0$. It can be seen from Fig. 11 that after compensation, _Iout swings much greater than _Qout, while before compensation, both Idata and Qdata swing with an envelop of the same level. So, we can assert that the carrier synchronization has been achieved.

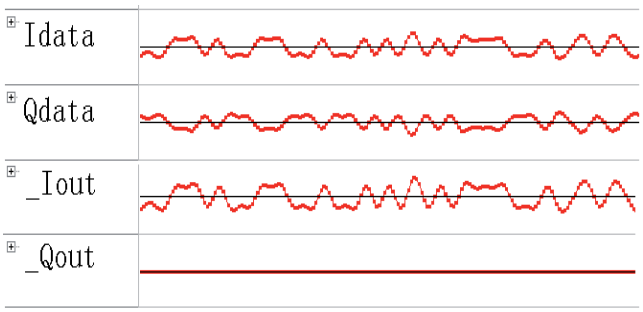

Fig. 12. BPSK synchronization result.

5. Conclusion

In this paper, a feedback compensation algorithm and relevant receiver structure are proposed. This receiver structure takes advantages of both feedback control loop and feed-forward compensation loop. It may separate the demodulator and carrier synchronization block. This separation can not only clarify the receiver structure in the aspect of function, but also be helpful to modular design. Also, because of the introduced feedback scheme, the phase of input signal can be automatically tracked without complex computation. Further more, based on this new structure, the system designer may care little about the position of ADC, because neither the digital-IF form nor the analog-IF form will increase more complexity. This advantage lets the designer may pay more attention to other system problems.

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