Systematic Design of Fully Balanced Differential Current-Mode Multiple-Loop Feedback Filters Using CFBCCII

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Abstract. *In this paper, a systematic design method producing balanced current-mode filters is proposed, using current controlled fully balanced second-generation current conveyor circuit (CFBCCII). In this method, many kind of all-pole multiple loop feedback (MF) current mode balanced filters can be obtained, all the produced filters have fully balance structures. Moreover, the frequency of the filters can be electronically adjustable. The produced nth-order filters are constructed by n CFBCCIIs and 2n grounded capacitors, no resistors are needed. The sensitivities of the filters and influences of CFBCCII parasitic elements on filters are analyzed.*

Keywords

Fully balanced, current mode, filter, current conveyor**,** multiple-loop feedback formatting.

1. Introduction

Active filters stand very important positions in many areas such as high-speed computer communication transceiver chips, retrieval and storage systems, radio and TV receivers, and analog interface systems in general, numerous second-order [1-3] and high-order filters have been reported [4-9]. There are basically three approaches to the design of active filters with a high order: the cascade of biquadratic sections; simulation based on passive LC ladder prototypes; the multiple loop feedback (MF). Compared with cascade structures which have high sensitivity and ladder topologies that can implement only imaginary axis zero, MF active filters have both low sensitivity and arbitrary transmission zeros. In addition, MF filters have simple structure, so the multiple loop feedback is a very important approach to design *n*th-order filters [4].

Systematic designs of filters are very important, it can produce multiple structures. Till now some kinds of systematic designs of MF *n*th-order filters have been proposed. For example, papers [5-8] proposed systematic designs of *n*th-order MF filters based on OTA (Operational Transconductance Amplifier). However, they belong to voltage mode filters, and have relative complex structures. In addition, all these circuits but the one in paper [5] have not fully balanced structure. Paper [9] proposed current mode *n*th-order MF filters based on OTA, but it has not fully balanced structure, too.

Current-mode circuits have obvious advantage by comparison with voltage-mode circuits, current-mode circuits have low impedance, they have high speed and large bandwidth, lower nonlinear distortion and wider dynamic range, and the power consumption is low.

A fully balanced filter can suppress even order distortion and common-mode interference effectively. It has an important application in communication systems. In literature [5], systematic designs of fully balanced filters were proposed. However, it belongs to voltage mode circuit, too, 2*n* OTA and 2*n* capacitors are required to implement *n*th order filter. Moreover, the system is implemented by OTA that has narrow dynamic range and worse linearity compared with second generation current conveyor (CCII).

CCII, as a basic building block in the current-mode signal processing, is widely used in filter design, either single-ended [10-15] or differential [16]. Compared with single-ended circuits, differential current mode circuits have the ability of reducing even harmonics as well as common-mode interference, thus they play an important part in telecommunications. In a previous work, Chiu et al. proposed a differential difference current conveyor (DDCC) and a second-order filter which can realize low-pass and band-pass filtering function [17]. In 1997, Elwan et al. proposed two new differential voltage current conveyors (DVCC) [18], and realized a continuous-time current mode MOSFET-C filter. A fully differential current conveyor (FDCCII) [19] was presented by EI-Adawy. The circuit employs fully differential structure and suppresses undesirable common mode signals. A new realization of FDCCII was proposed by Soliman [20], and the terminals X, Y and Z of this circuit are all differential.

In modern VLSI applications, balanced-mode structures are increasingly used. In a balanced circuit, output common-mode signal is kept constant, and it is entirely independent of the input signal. Therefore, performance of a fully balanced structure (such as dynamic range, noise suppression, and harmonic distortion) can be largely improved. A fully balanced current conveyor [21] provides a pair of differential Y terminals and a pair of differential X terminals. The circuit introduces a common-mode feedback

circuit and an RC compensation circuit which keeps the common mode signal constant, while increasing the dynamic range of differential mode signals. In 2004, Alzaher introduced a CMOS fully differential current conveyor [22]. However, in all of these previously reported elements, there exists a relatively significant voltage tracking error from terminal Y to terminal X. The parasitic resistor in terminal X leads to transfer function error in their application circuits. Moreover, these elements lack electronic programmability, which has become a key feature in recent application.

In this paper, by introducing a new element, current controlled fully balanced second-generation current conveyor circuit (CFBCCII), a systematic design method producing all-pole MF current-mode filter is proposed. The CFBCCII with fully balanced structure can suppress common-mode signals, and its port relation has electronic programmability. The produced filters from systematic method have fully balanced structure which can reduce even order distortion and common-mode interference effectively. Moreover, the frequency of the filters is electronically adjustable. The sensitivity of the filter is less than 1. In addition, the structure of the circuit is simple, all the *n*th-order filters are constructed by *n* CFBCCII, 2*n* capacitors and no resistors. All capacitors are grounded, so the circuit is convenient for integration.

2. CFBCCII Circuit and Realization

The circuit symbol of CFBCCII is shown in Fig. 1, where I_B denotes the bias current of CFBCCII. Here, Y_+, Y_- are differential voltage input terminals, X_+ and X_- behave as differential voltage tracking terminals, Z_{1+}, Z_{2+} and Z_{1-}, Z_{2-} are the current output terminals. The number of current output terminals Z can be extended if necessary. Its ideal port characteristics can be expressed as:

$$\begin{cases} I_{Y+} = I_{Y-} = 0 \\ V_{X+} - V_{X-} = (V_{Y+} - V_{Y-}) + (I_{X+} - I_{X-})R_X \\ I_{Z1+} - I_{Z1-} = I_{Z2+} - I_{Z2-} = I_{X+} - I_{X-} \end{cases} \quad (1)$$

where R_x represents the parasitic resistance of terminal X.

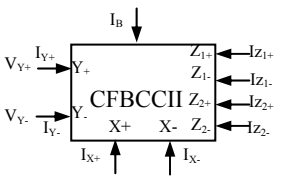


Fig. 1. Symbol of CFBCCII.

The circuit frame diagram of CFBCCII is given in Fig. 2. The circuit is made up of four blocks: the differential voltage input stage, the second-generation current controlled current conveyor (CCCII), voltage-sampling circuit, and the common mode feedback circuit (CMFB).The basic principle of the circuit is analyzed as follows: There are two signal-feed paths in the circuit, the feedforward and the feedback path. The feedforward path consists of a differential input stage and two CCCIIs. Differential voltage signals are added to the differential input stage, and the voltages would be transferred to the points A and B. The current controlled current conveyors (CCCII) are employed to transfer V_A and V_B to the output terminals. The feedback path consists of voltage sampling circuit and CMFB circuit. The voltages of the points A and B will be sampled in the voltage sampling block, where the common-mode (CM) voltage V_{CM} is generated. The CMFB circuit is employed to suppress the CM signals, by comparing V_{CM} and V_{RCM}, V_{CM} is forced to follow $V_{CM}= V_{RCM}$, in this way, the CM signal can be effectively suppressed.

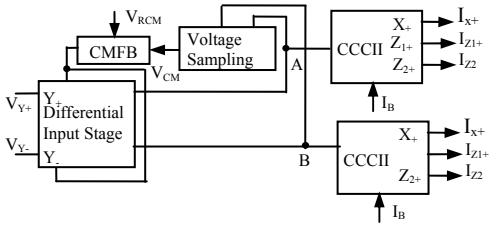


Fig. 2. Frame diagram of CFBCCII.

The realization of the CFBCCII circuit is illustrated in Fig. 3, M_1~M_4 constitute two pairs of differential inputs, the parameters of the transistors are symmetric. The circuit has high input impedance as the input voltages are applied to the circuit by the gates of MOS transistors, so $I_{Y+}= I_{Y-}= 0$. Assuming that all transistors operate in their saturation region, and channel-length modulation effects are not taken into consideration, we get:

$$I_M = (KW/L)(V_{GS} - V_T)^2 , \quad (2)$$

$$K = \mu c_{ox} \frac{W}{L}, \mu = K_\mu T^{-1.5} \quad (3)$$

where K is the transconductance parameter, W and L are the width and length of the drain channel respectively, V_T is the threshold voltage.

The two pairs of differential transistors are loaded by M_{10}~M_{11} which carry equal bias currents (I_B). M_{20}~M_{22} compose current mirrors. So:

$$I_{M1} + I_{M3} = I_{M2} + I_{M4} = I_B , \quad (4)$$

$$I_{M1} + I_{M4} = I_{M2} + I_{M3} \quad (5)$$

where I_{Mi}(i=1-4) respectively denotes the drain current of the transistor M_i. From (4), (5), we get:

$$I_{M1} = I_{M2}, I_{M3} = I_{M4} . \quad (6)$$

If channel dimensions of M_1~M_4 are: $W_1/L_1=W_2/4L_2$, $W_3/L_3=W_4/4L_4$, we get:

$$\begin{aligned} (V_{Y1} - V_A + V_T)/2 &= V_D - V_B = V_{Y4} - V_C \\ (V_{Y2} - V_A + V_T)/2 &= V_{Y3} - V_B = V_G - V_C \end{aligned} \quad (7)$$

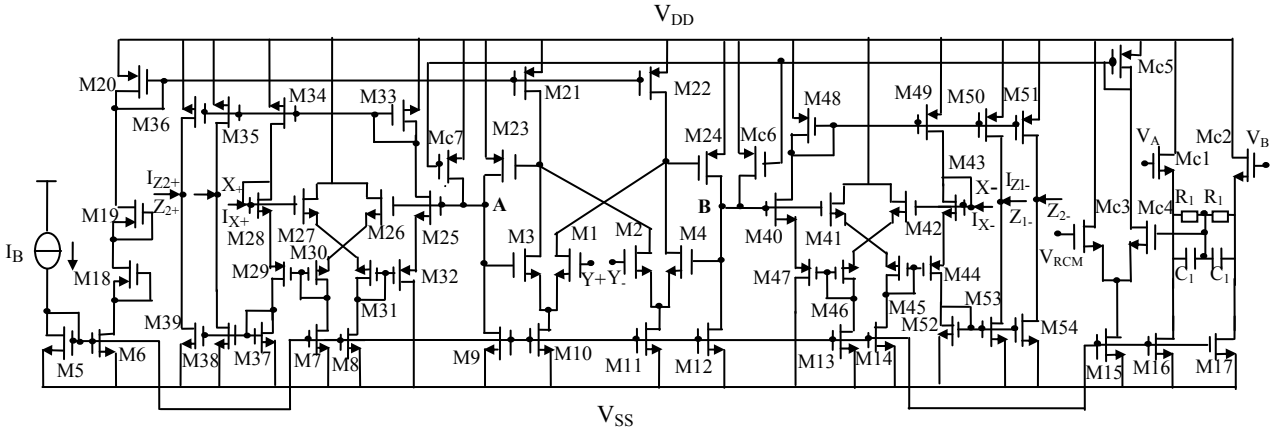


Fig. 3. Circuit realization of CFBCCII.

Then the expressions for V_A and V_B become:

$$V_A = V_B = \frac{1}{2}(V_{Y+} - V_{Y-}). \tag{8}$$

M_{25}~M_{32}, M_{40}~M_{44} constitute two CMOS translinear loops, M_{25}~M_{32} transfer the voltage from point A to X+, and M_{40}~M_{44} transfer the voltage from point B to X-. Now consider the translinear loop of M_{25}~M_{32}: M_{25} and M_{32}, M_{26} and M_{30}, M_{27} and M_{31}, M_{28} and M_{29} constitute four compound transistors respectively. If the channel aspect ratios *W/L* of NMOS transistors in the four compound transistors are identical, and the ratios *W/L* of PMOS transistors are alike (all transistors operate in saturation region), we can get [23]:

$$\begin{aligned} R_X &= (2\sqrt{2K_{eff}}\sqrt{I_B})^{-1} \\ K_{eff} &= K_n K_p / (\sqrt{K_n} + \sqrt{K_p})^2 \end{aligned} \tag{9}$$

where K_n and K_p are the transconductance coefficient of the PMOS and NMOS transistor, so R_x can be adjusted by I_B. From (3) and (9), R_x is increased while temperature increases.

In Fig. 3, M_{34}~M_{36}, M_{37}~M_{39}, M_{49}~M_{51}, M_{52}~M_{54} are four current mirrors respectively, then $I_{Z1+} = I_{Z2+} = I_{X+}$, $I_{Z1-} = I_{Z2-} = I_{X-}$, so:

$$I_{Z+} - I_{Z-} = I_{X+} - I_{X-}. \tag{10}$$

It is clear that the proposed CFBCCII satisfies the characteristics shown in (1). In Fig. 3, the common mode feedback circuit consists of M_{C1}-M_{C8} in addition to two resistors (R) and two capacitors (C). The operation of the CMFB is explained in [2] in detail. The CMFB circuit suppresses the common-mode and increases the input dynamic range to a great extent, and it can suppress common-mode interference effectively.

CFBCCII is simulated in SPICE using 0.35μm CMOS process parameters for transistors shown in Tab. 1. The dimensions of MOS transistors are listed in Tab. 2. Supply voltages are ± 1.65 V.

```
.model  SEANMOS nmos (level=3 UO=460.5 TOX=1.0E-8
TPG=1 VTO=.62 JS=1.8E-6 +XJ=.15E-6 RS=417 RSH=2.73
LD=0.04E-6 ETA=0 VMAX=130E3 NSUB=1.71E17 PB=0.761
+PHI=0.905 THETA=0.129 GAMMA=0.69 KAPPA=0.1 AF=1
WD=0.11E-6 CJ=76.4E-5 +MJ=0.357 CJSW=5.68E-10
MJSW=0.302 CGSO=1.38E-10 CGDO=1.38E-10
+CGBO=3.45E-10 KF=3.07E-28 DELTA=.42 NFS=1.2E11)

.model  SEAPMOS pmos (level=3 UO=100 TOX=1.0E-8
TPG=1 VTO=-0.58 JS=0.38E-6 +XJ=0.1E-6 RS=886 RSH=1.81
LD=0.03E-6 ETA=0 VMAX=113E3 NSUB=2.08E17 PB=0.911
+PHI=0.905 THETA=0.120 GAMMA=0.76 KAPPA=2 AF=1
WD=0.14E-6 CJ=85E-5 +MJ=0.429 CJSW=4.67E-10
MJSW=0.631 CGSO=1.38E-10 CGDO=1.38E-10
+CGBO=3.45E-10 KF=1.08E-29 DELTA=.81 NFS=0.52E11)
```

Tab. 1. 0.35μm CMOS process parameters for transistors.

MOS Transistors	W/L (μm)	M0S Transistos	W/L(μm)
M_1,M_3	2/0.35	M_5-M_{14}	16/0.35
M_2,M_4	8/0.35	M_{16}-M_{17}	10/0.35
M_{15}	80/0.35	M_{18}-M_{19}	
M_{20}-M_{22}	14/0.35	M_{23}, M_{24}	20/0.35
M_{25}-M_{28} M_{40}-M_{43}	10/0.35	M_{29}-M_{32}, M_{44}-M_{47}	40/0.35
M_{33}-M_{36} M_{48}-M_{51}	80/0.35	M_{37}-M_{39}, M_{52}-M_{54}	4/0.35
M_{c1}-M_{c4}	1/0.35	M_{c5}-M_{c7}	2/0.35

Tab. 2. Dimensions of MOS transistors in CFBCCII.

The theoretical result and the simulated result of relationship between R_x and I_B are given in Fig. 4.

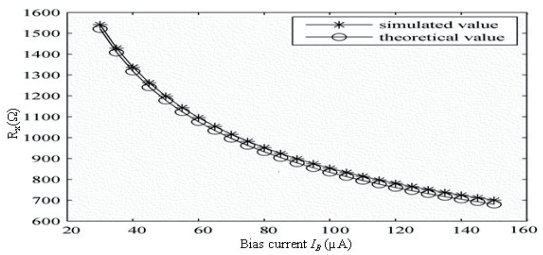


Fig. 4. Simulated relationship between R_x and I_B.

The relation of R_x and temperature has been given in Fig. 5. From Fig. 5, it can be seen that the influence of temperature on R_x is very small.

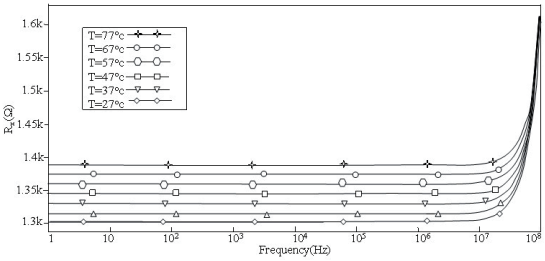


Fig. 5. The influence of temperature on R_x of CFBCCII.

The transconductance common-mode gain (A_{CM}) is $(I_{z+}+I_{z-})/(V_{y+}+V_{y-})$. The simulation result of A_{CM} of CFBCCII is given in Fig. 6. It can be seen from Fig. 6 that A_{CM} it is equal to 2.7×10^{-6} which is very small.

The input and output impedance of CFBCCII can be seen in Fig. 7 and Fig. 8 while bias currents are equal to 40, 50, 65 μA respectively. It is clear that input impedance is independent of bias currents, but output impedance is influenced by bias currents. From Fig. 7, it is known that the input impedance is larger than 46 MΩ and 4.5 MΩ when frequency is less than 1 MHz and 10 MHz respectively. From Fig. 8, it is known that output impedance is equal to 1 MΩ approximately when frequency is less than 1 MHz.

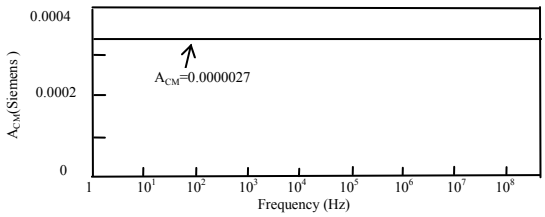


Fig. 6. Common-mode gain of CFBCCII.

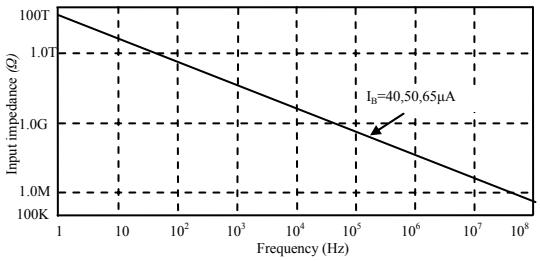


Fig. 7. Input impedance of Y terminal of CFBCCII.

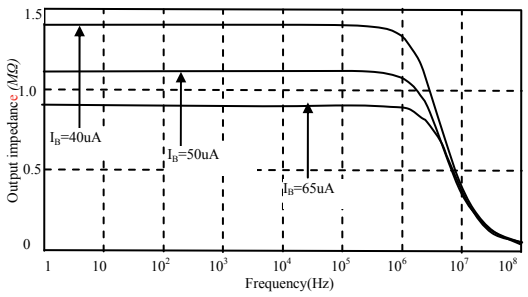


Fig. 8. Output impedance of CFBCCII.

The stability of CFBCCII is analyzed. From Fig. 3, it is clear that the stability of CFBCCII is determined by the circuit between X and Y where the feedback circuit exist in. According to [27], the stability criteria are as follows: at the frequency (f_{cl}) with transfer gain = 0 dB, if $-180^o <$ phase $< 180^o$ and phase margin (phase shift distance from ±180°) > 45°, the system is stable. The gain and phase of differential terminal X and Y transfer function $(V_{x+}-V_{x-})/(V_{y+}-V_{y-})$ with three bias currents are shown in Fig. 9. It can be seen that at about $f_{cl} = 0.8$ GHz, gain is 0 dB and phase margin > 45°. So the system satisfies stability criteria and is stable.

The differential currents of terminal Z and X with three bias currents: 30 μA, 65 μA and 100 μA are given in Fig. 10.

Fig. 11 shows the simulated DC characteristic of differential voltages between terminal X and Y, the voltage of X terminals is undistorted when the input voltage of Y terminals is ±1.5 V. So the input dynamic range is ±1.5 V.

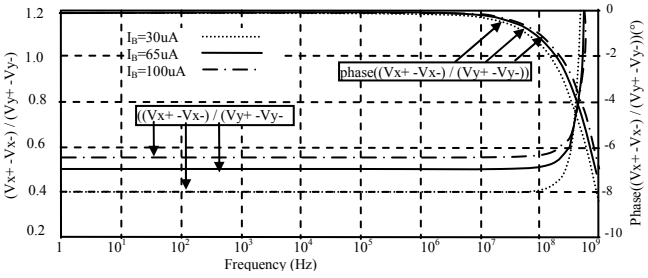


Fig. 9. The gain and phase response of differential voltage transfer between X and Y in CFBCCII.

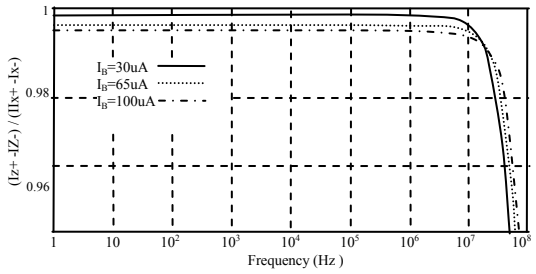


Fig. 10. Simulated frequency response of Z-X current.

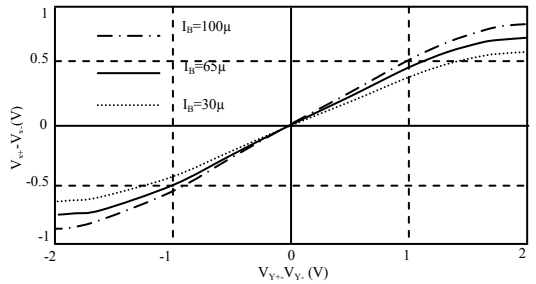
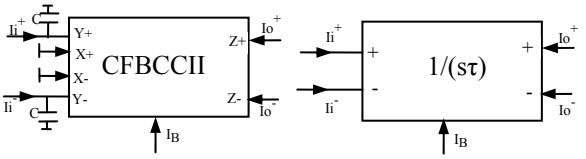


Fig. 11. Simulated Y-X DC characteristics.

From above analysis, it is clear that the CFBCCII with fully balanced structure can suppress common-mode signals, and its port relation has electronic programmability compared with classical fully differential operational amplifiers [17-20].

3. Systematic Design Method of Fully Balanced Current Mode Filter

3.1 CFBCCII Based Integrator



(a) Structure (b) Symbol

Fig. 12. Structure and symbol of CFBCCII integrator.

The structure of CFBCCII integrator is shown in Fig. 12. (a). Routine analysis based on (1), we can get:

$$\begin{aligned} i_o^+ - i_o^- &= i_X^+ - i_X^- \\ 0 &= (i_i^+ - i_i^-)\frac{1}{sC} + (i_X^+ - i_X^-)R_X \end{aligned} \quad . \tag{11}$$

The symbol of CFBCCII integrator is show in Fig. 12. (b), form (11) we can get:

$$H(s) = \frac{i_o^+ - i_o^-}{i_i^+ - i_i^-} = -\frac{1}{sR_XC} = -\frac{1}{s\tau} \quad . \tag{12}$$

3.2 Model and Relations of the MF Balanced Current Mode Filter

The model circuit of MF balanced current mode filter based on CFBCCII is shown in Fig. 13. The circuit is constructed by two parts: The feed-forward circuit consisting of *n* CFBCCII integrators and the feed-back network constructed symmetrically by links connecting I_{fi}^-, I_{fi}^+, I_{oj}^+ and I_{oj}^-. From Fig. 13, the feedback equations can be obtained as follows:

$$I_f^+ = -FI_o^-, I_f^- = -FI_o^+ \tag{13}$$

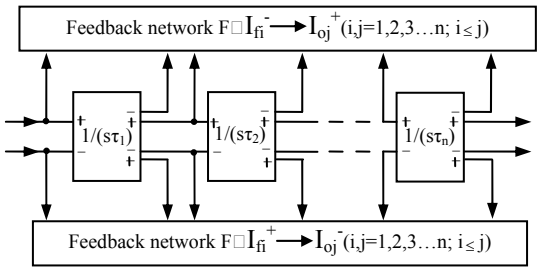


Fig. 13. Model circuit of differential MF filters

where $I_o^+ = [I_{o1}^+, I_{o2}^+ \ldots I_{on}^+]^T$, $I_o^- = [I_{o1}^-, I_{o2}^- \ldots I_{on}^-]^T$ is the output vector, and $I_f^+ = [I_{f1}^+, I_{f2}^+ \ldots I_{fn}^+]^T$, $I_f^- = [I_{f1}^-, I_{f2}^- \ldots I_{fn}^-]^T$ is the feedback vector. $F = [f_{ij}]_{n\times n}$ is the feedback matrix, when $i<j$, $f_{ij}=0$, so F is an upper triangular matrix, namely:

$$F = \begin{pmatrix} f_{11} & f_{12} & f_{13} & \cdots & f_{1n} \\ 0 & f_{22} & f_{23} & \cdots & f_{2n} \\ 0 & 0 & f_{33} & \cdots & f_{3n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & f_{nn} \end{pmatrix} \tag{14}$$

Based on the model circuit in Fig. 13 and (1), the equations can be derived:

$$I_{in}^+ - I_{in}^- - (I_f^+ - I_f^-) = M(I_o^+ - I_o^-) \tag{15}$$

where $I_{in}^+ - I_{in}^- = \left(I_i^+ - I_i^-, 0, 0, \cdots 0\right)^T$, and

$$M = \begin{pmatrix} s\tau_1 & 0 & 0 & \cdots & 0 \\ -1 & s\tau_2 & 0 & \cdots & 0 \\ 0 & -1 & s\tau_3 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & s\tau_n \end{pmatrix}.$$

From (13) and (15), the transfer function of systematic model circuit in Fig. 13 can be shown as following:

$$H(s) = \frac{I_o^+ - I_o^-}{I_{in}^+ - I_{in}^-} = \frac{1}{F+M} = \frac{1}{|A(s)|} \tag{16}$$

where $|A(s)|$ represents the determinant of A(s).

3.3 Filter Production and Synthesis

To illustrate the general design theory above, we take the design of fourth-order filter as an example. The system matrix $A(s)$ of the filter is:

$$A(s) = \begin{pmatrix} s\tau_1 + f_{11} & f_{12} & f_{13} & f_{14} \\ -1 & s\tau_2 + f_{22} & f_{23} & f_{24} \\ 0 & -1 & s\tau_3 + f_{33} & f_{34} \\ 0 & 0 & -1 & s\tau_4 + f_{44} \end{pmatrix}. \tag{17}$$

From (16) and (17), the transfer function of the four-order filter system can be derived:

$$\begin{aligned} H(s) = 1/\{&(\tau_1\tau_2\tau_3\tau_4)s^4 + (\tau_1\tau_2\tau_3 f_{44} + \tau_1\tau_2\tau_4 f_{33} \\ &+ \tau_1\tau_3\tau_4 f_{22} + \tau_2\tau_3\tau_4 f_{11})s^3 + [\tau_1\tau_2(f_{33}f_{44} + f_{34}) + \\ &\tau_1\tau_3 f_{22}f_{44} + \tau_1\tau_4(f_{22}f_{33} + f_{23}) + \tau_2\tau_3 f_{11}f_{44} + \\ &\tau_2\tau_4 f_{11}f_{33} + \tau_3\tau_4(f_{11}f_{22} + f_{12})]s^2 + [\tau_1(f_{22}f_{33}f_{44} \\ &+ f_{22}f_{34} + f_{23}f_{44} + f_{24}) + \tau_2(f_{11}f_{33}f_{44} + f_{11}f_{34}) + \\ &\tau_3(f_{11}f_{22}f_{44} + f_{12}f_{44}) + \tau_4(f_{11}f_{22}f_{33} + f_{11}f_{23} + \\ &f_{12}f_{33} + f_{13})]S + (f_{11}f_{22}f_{33}f_{44} + f_{11}f_{22}f_{34} + \\ &f_{11}f_{23}f_{44} + f_{12}f_{33}f_{44} + f_{11}f_{24} + f_{13}f_{44} + f_{12}f_{34} + f_{14})\} \end{aligned} \tag{18}$$

We can obtain a variety of fourth-order filters by selecting different f_{ij}, and we will show four kinds of them arbitrarily.

Structure 1: if $f_{11}=f_{12}=f_{13}=f_{14}=1$, the corresponding filter circuit is shown in Fig. 14. (a). Its transfer function is:

$$H(s)=1\Big/\{(\tau_1\tau_2\tau_3\tau_4)s^4+\tau_2\tau_3\tau_4 s^3+\tau_3\tau_4 s^2+\tau_4 s+1\}. \quad (19)$$

Structure 2: if $f_{11}=f_{12}=f_{23}=f_{24}=1$, the corresponding filter circuit is shown in Fig. 14. (b). Its transfer function is:

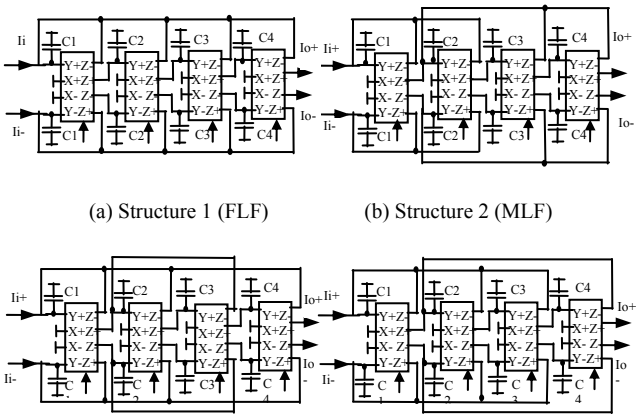
$$H(s)=1\Big/\{(\tau_1\tau_2\tau_3\tau_4)s^4+\tau_2\tau_3\tau_4 s^3+(\tau_3\tau_4+\tau_1\tau_4)s^2+(\tau_1+\tau_4)s+1\}. \quad (20)$$

Structure 3: if $f_{11}=f_{12}=f_{23}=f_{14}=1$, the corresponding filter circuit is shown in Fig. 14. (c). Its transfer function is:

$$H(s)=1\Big/\{(\tau_1\tau_2\tau_3\tau_4)s^4+\tau_2\tau_3\tau_4 s^3+(\tau_3\tau_4+\tau_1\tau_4)s^2+\tau_4 s+1\}. \quad (21)$$

Structure 4: if $f_{11}=f_{12}=f_{13}=f_{24}=1$ the corresponding filter circuit is shown in Fig. 14. (d). Its transfer function is:

$$H(s)=1\Big/\{(\tau_1\tau_2\tau_3\tau_4)s^4+\tau_2\tau_3\tau_4 s^3+\tau_3\tau_4 s^2+(\tau_1+\tau_4)s+1\}. \quad (22)$$



(a) Structure 1 (FLF) (b) Structure 2 (MLF)

(c) Structure 3 (IFLF) (d) Structure 4 (MSF)

Fig. 14. Four kinds of MF filters based on CFBCCII.

The four structures belong to follow-the-leader-feedback (FLF), modified-leap-frog (MLF), inverse FLF (IFLF) and the minimum-sensitivity-feedback (MSF) structure respectively. The structure of FLF is simple; MLF provides the freedom to optimize the filter to meet some requirements; IFLF can maximize dynamic range; MSF has low sensitivity [26].

It can be seen from Fig. 14 that the fourth-order filter is constructed by 4 CFBCCIIs and 8 capacitors, and we can get the *n*th-order filter that is constructed by *n* CFBCCIIs and 2*n* capacitors.

3.4 Design Examples

As an example, we design a fourth-order Butterworth filter. The normalized transfer function of fourth-order Butterworth filter is:

$$H(s)=1\Big/\begin{matrix}(s^4+2.61313\,s^3+3.4142\,s^2\\+2.61313\,s+1)\end{matrix}. \quad (23)$$

The structure 1 in Fig. 14. (a) is used to realize the filter. From (19) and (23), we can get: τ_1=0.3827, τ_2=0.7654, τ_3=1.3066, τ_4=2.61313, and $\tau_i=R_x\overline{C_i}$ (i=1~4), $\overline{C_i}$ is the normalized capacitor. Setting R_x=1 kΩ, then we get I_B=65 μA, $\overline{C_1}=3.827\cdot10^{-4}$F, $\overline{C_2}=7.654\cdot10^{-4}$F, $\overline{C_3}=13.066\cdot10^{-4}$F, $\overline{C_4}=26.131\cdot10^{-4}$F. If cut-off frequency (f_c) is equal to 1 MHz, according (24), we can get: C_1=60.90 pF, C_2=121.80 pF, C_3=207.93 pF, C_4=415.85 pF.

$$C_i=\overline{C_i}\Big/2\pi f_C(i=1,2,3,4). \quad (24)$$

The simulation results are given in Fig. 15. The curve"□" responds to I_B=65 μA, and f_c = 1 MHz.

The f_c of the proposed MF filters can be tuned by I_B of CFBCCIIs. In order to keep form of fourth-order Butterworth filter shown in (23), τ must be invariant. According to $\tau_i=R_x\overline{C_i}$ (i=1~4) , if R_x is decreased, $\overline{C_i}$ would be increased. According to (24), if C_i keeps invariant, f_c will be increased.

According to above tune principle, when choosing I_B= 30 μA, the R_x is equal to 1.41 kΩ, it can be obtained f_c= 0.82 MHz; when choosing I_B= 100 μA, R_x= 0.77 kΩ and f_c= 0.82 MHz. The simulation results are shown as "□" and "○" respectively in Fig. 15.

Similarly, the stability of the filter can be analyzed. Fig. 15 and Fig. 16 are gain and phase characteristics of differential current transfer function $(I_{o+}-I_{o-})/(I_{i+}-I_i)$ in structure 1. It can be seen that in Fig. 15, at f_{c1}= 1 MHz corresponding Gain = 0 dB, phase = 31° which is more than -180° and less than 180°, and phase margin = 128° which is more than 45°. The stability criteria [27] are satisfied to the filter, and it is stable.

The time-domain response and the linearity of the filter can be seen in Fig. 17 and 18, when setting I_B= 65 μA and the C_i are kept invariant. From Fig. 18, it is known that the input linear range of the filter is larger than 2 mA.

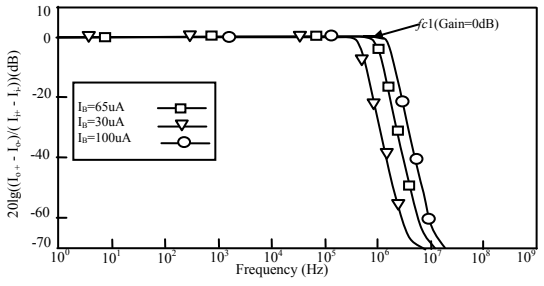


Fig. 15. Frequency response of the filter of structure 1.

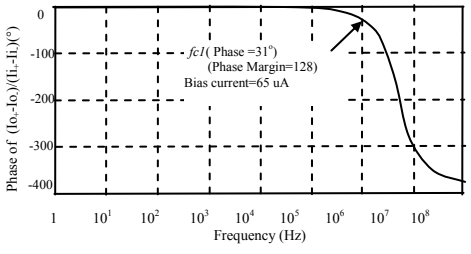


Fig. 16. Phase response of filter of structure 1.

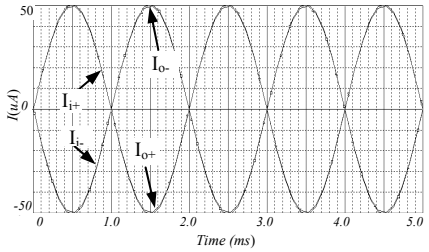


Fig. 17. Time-domain response of the filter of structure 1.

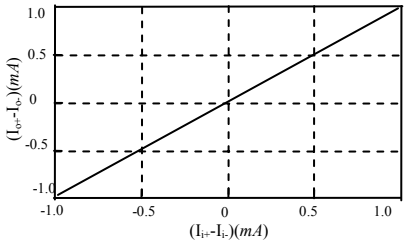


Fig. 18. Linearity of the filter of structure 1.

Harmonic	Frequency(Hz)	Fourier component
No. 1	100K	8.618×10^{-3}
No. 2	200K	8.611×10^{-9}
No. 3	300K	1.694×10^{-7}
No. 4	400K	6.937×10^{-9}
No. 5	500K	1.189×10^{-7}
No. 6	600K	2.636×10^{-9}
No. 7	700K	7.340×10^{-8}
No. 8	800K	6.875×10^{-10}
No. 9	900K	2.975×10^{-8}

Tab. 3. The even order distortion of filter.

The produced filters from systematic method have fully balanced structure which can reduce even order distortion and common-mode interference effectively. The even order distortion analysis with base frequency 100 kHz is given in Tab. 3 where Fourier components of the first~9th harmonics are given. It is noted that even harmonics are restrained largely. So the filter can reduce even order distortion.

3.5 Sensitivity Analysis

To study the sensitivity in the proposed filter, τ_j are important parameters. The definition of sensitivity is:

$$S_{\tau_j}^{H(s)} = \frac{\tau_j}{H(s)} \frac{\partial H(s)}{\partial \tau_j}. \tag{25}$$

According to [24], it is known that:

$$\begin{aligned} S_{\tau_j}^{H(s)} &= -s\tau_j \frac{|A_{jn}(s)A_{1j}(s)|}{|A(s)|} \\ &= -s\tau_j H(s)|A_{jn}(s)A_{1j}(s)| \end{aligned}. \tag{26}$$

The structure 1 in Fig. 14. (a) is analyzed, and the others are similar to it. From (26) and (19), we can get:

$$S_{\tau_1}^{H(s)} = \frac{\tau_1\tau_2\tau_3\tau_4 s^4}{\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + \tau_3\tau_4 s^2 + \tau_4 s + 1}, \tag{27}$$

$$S_{\tau_2}^{H(s)} = \frac{\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3}{\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + \tau_3\tau_4 s^2 + \tau_4 s + 1}, \tag{28}$$

$$S_{\tau_3}^{H(s)} = \frac{\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + \tau_3\tau_4 s^2}{\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + \tau_3\tau_4 s^2 + \tau_4 s + 1}, \tag{29}$$

$$S_{\tau_4}^{H(s)} = \frac{\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + \tau_3\tau_4 s^2 + \tau_4 s}{\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + \tau_3\tau_4 s^2 + \tau_4 s + 1} \tag{30}$$

where $s=j\omega$. It can be seen in Fig. 19 the sensitivities of τ_1, τ_2, τ_3, τ_4 are very close to each other, and are less than 1.

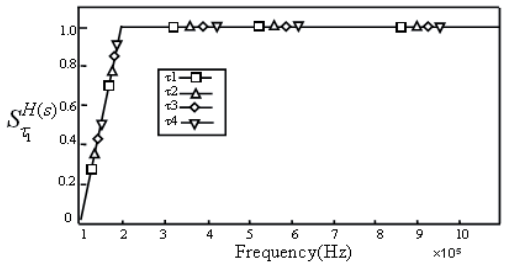


Fig. 19. Sensitivity of the filter of structure 1.

3.6 Influence of CFBCCII Parasitic Elements

The nonideal CCII model [25] is shown in Fig. 20. The real CCII has parasitic resistors and capacitors from the Y and Z terminals to the ground, and a serial resistor at the input terminal x. $\alpha(s)$ and $\beta(s)$ are used to represent the followers of the CCII, respectively, and they are considered as 1 here.

As a nonideal CFBCCII, parasitic resistors and capacitors of Y (including Y+, Y-) terminals and Z (including Z+, Z-) terminals are almost the same with Y terminal and Z terminal of CCII respectively, and it is assumed that they all equal to R_y, C_y and R_z, C_z respectively.

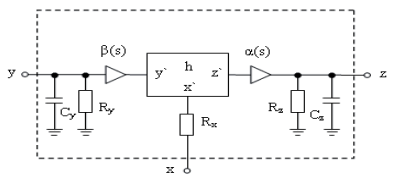


Fig. 20. Non-ideal CCII with its parasitic resistors and capacitors.

To study the influence of parasitic elements in CFBCCII, the structure 1 shown in Fig. 14. (a) is considered, and it can be transformed to Fig. 21. Other structures can be analyzed in this way. We define G_{z1}, G_{z2}, G_{z3}, G_{z4}, C_{z1}, C_{z2}, C_{z3}, and C_{z4} as the parasitic elements of the z terminals of CFBCCII in Fig. 21, and G_{y1}, G_{y2}, G_{y3}, G_{y4}, C_{y1}, C_{y2}, C_{y3}, C_{y4} as the parasitic elements of the Y terminals of CFBCCII respectively. The serial resistance of the x terminals of CFBCCII is considered as R_x.

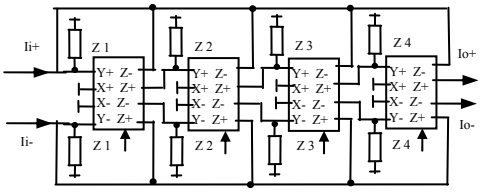


Fig. 21. Proposed filter of structure 1 including the parasitic elements of the CFBCCII.

Analyzing Fig. 22 yields following equations:

$$\begin{aligned} Y_1(j) &= j\omega\left(C_1 + C_{y1} + C_{z1} + C_{z2} + C_{z3} + C_{z4}\right) \\ &\quad + G_{yz1} + G_{yz2} + G_{yz3} + G_{yz4} \\ &= j\omega\left(C_1 + C_y + 4C_z\right) + 4G_{yz} \end{aligned}, \tag{31}$$

$$\begin{aligned} Y_2(j) &= j\omega\left(C_2 + C_{y2} + C_{z1}\right) + G_{yz1} \\ &= j\omega\left(C_2 + C_y + C_z\right) + G_{yz} \end{aligned}. \tag{32}$$

Similarly, we can get Y_3, Y_4.

$$Y_i(j) = j\omega\left(C_i + C_y + C_z\right) + G_{yz} \tag{33}$$

where $Y_i = 1/Z_i$, $C_y = C_{yi}$, $C_z = C_{zi}$, $G_{yz} = G_{yzi} = G_{yi} + G_{zi}$ (i=1~ 4).

It is considered that C_y and C_z are smaller than 10 pF , G_{yz} is smaller than 10^{-6} S, and the frequency f_c is more than 1 MHz. Therefore, Y_1, Y_2, Y_3, and Y_4 can be approximated by:

$$\begin{aligned} Y_1(j) &= j\omega\left(C_1 + C_y + 4C_z\right) + 4G_{yz} \\ &= j\omega\left(C_1 + C_y + 4C_z\right)\left[1 + \frac{4G_{yz}}{j\omega\left(C_1 + C_y + 4C_z\right)}\right], \\ &\approx j\omega\left(C_1 + C_y + 4C_z\right) \end{aligned} \tag{34}$$

$$\begin{aligned} Y_i(j) &= j\omega\left(C_i + C_y + C_z\right) + G_{yz} \\ &= j\omega\left(C_i + C_y + C_z\right)\left[1 + \frac{G_{yz}}{j\omega\left(C_i + C_y + C_z\right)}\right]. \\ &\approx j\omega\left(C_i + C_y + C_z\right)(i = 2,3,4) \end{aligned} \tag{35}$$

From (31) - (35), it is observed that the parasitic capacitors are the main influence factor, we define that c_i' (i=1~4) as the capacitors including the parasitic elements of the CFBCCIIs. Because of C_y and C_z are smaller than 10 pF, the parasitic capacitors can be negligible by comparison if $C_i >> (C_y + C_z)$ (i=1~4), and the CFBCCII can be seen as ideal one.

From (24), (34), (35), we get:

$$\Delta f_c = f_c' - f_c = f_c\left(\frac{c_i' - c_i}{c_i'}\right)(i = 1,2,3,4) \tag{36}$$

where f_c' is the cut-off frequency of the filter including the parasitic elements of the CFBCCIIs .

To verify the analysis, we keep I_B = 65 μA invariant, change the capacitors, the simulated results and theoretical ones (from (23)) are given in Fig. 22. It can be seen that the simulated curves are in accordance with theoretical ones when frequency is less than 10 MHz. When frequency is larger than 10 MHz, the capacitors C_i (i=1~4) are comparable with parasitic capacitors, and non-ideal characteristic of CFBCCII needs to be considered, the frequency modified formula shown in (36) can be used.

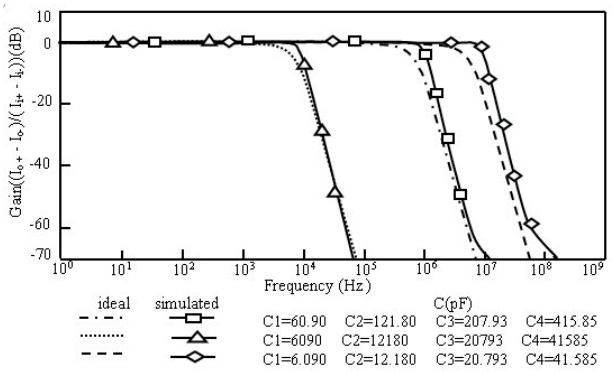


Fig. 22. Simulation results of the influence of parasitic elements to the proposed filter.

From above analysis, it can be known that compared with other circuit [5-9], the filter suppresses even order distortion, has wide dynamic range and good linearity, low sensitivity.

4. Conclusion

This paper proposed a method of designing nth-order multi-loop feedback filter based on CFBCCII. The method has following advantages: The various current mode balanced structures of the low-pass filters can be generated by changing the form of the feedback; fully balanced structure of the filter can reduce even harmonics and common-mode signals effectively; the cut-off frequency of the filter can be controlled by the bias current of CFBCCII. The produced nth-order filters are constructed by n CFBCCIIs and 2n RC passive elements; all passive components are grounded, so the filters can be integrated conveniently; the filters are not affected by non-ideal characteristic of CFBCCII when frequency is less than 10 MHz.

Acknowledgements

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