New Grounded and Floating Simulated Inductance Circuits using Current Differencing Transconductance Amplifiers

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Abstract. *Current differencing transconductance amplifier (CDTA) is receiving considerable attention as a building block for current-mode (CM) analog signal processing / signal generation. In this paper, new CDTA based lossless grounded and floating inductance simulation circuits have been proposed. The proposed grounded simulated inductance circuit employs two CDTAs and a single grounded capacitor whereas the floating simulated inductance circuit employs three CDTAs and a grounded capacitor. The circuit for grounded inductance does not require any realization conditions whereas in case of floating inductance only equality of two transconductances is needed (which can be easily maintained in practice by ensuring equal dc bias currents in the two trans-conductance amplifiers). Some sample results demonstrating the applications of the new simulated inductors using CMOS CDTAs have been given to confirm the workability of the new circuits.*

Keywords

CDTA, inductance simulation, filters.

1. Introduction

Recently, CDTAs have been extensively used as building blocks in a number of CM and voltage-mode (VM) signal processing and signal generation applications. Although the filter applications of CDTA have been reported in the literature such as a Tow-Thomas equivalent biquad using CDTAs presented in [1], a design of high order filters using CDTAs (cascadable filter, CDTA-based ladder structure and cascadable CM filter) were published in the literature [2], [3], [8], VM and CM KHN equivalents using CDTAs were published in [4], [5], and [7], allpass (AP) VM and CM filters using CDTAs appeared in [6] and [11], a MISO-type CM filter using CDTA was published in [9], and single CDTA biquads in VM and CM have been presented in [12], [13], and [14]. There are several non filtering applications of CDTA such as quadrature oscillator in [15], [16], [19], [20] and multi-phase sinusoidal oscillator in [17], and single resistance controlled oscillator in [18]. It is interesting to note that although grounded and floating inductor using Current Differencing Buffered Amplifier (CDBA) (which can be considered to be a 'sister' of CDTA) have been reported earlier in [21] and [22], very few inductance simulation circuits using CDTAs have been reported in the literature so far. In fact, only the floating inductance circuit of [23] can be cited in this context. The purpose of this paper is, therefore, to propose a new lossless grounded inductance and an alternative lossless floating inductance simulation circuit using CDTAs.

2. The Proposed New Configurations

The proposed configurations are shown in Fig. 1 and in Fig. 2.

Assuming an ideal CDTA is characterized by $V_p = V_n = 0$, $I_z = I_p - I_n$, $I_x^+ = g_m V_z$, $I_x^- = -g_m V_z$, where $V_z = I_z.Z_z$ and Z_z is the external impedance connected to the z-terminal of the CDTA.

For selected currents and node voltages, well-known equations can be obtained for Fig. 1 as:

$$I_{in} = -I_{Z_1} = 2g_{m_2} V_{Z_2} = 2g_{m_2}\left(\frac{I_{Z_2}}{sC}\right) = \frac{4g_{m_1}g_{m_2}}{sC} V_{in},$$
$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)}, \tag{1}$$
$$Z_{in}(s) = s\left(\frac{C}{4g_{m_1}g_{m_2}}\right).$$

The circuit, thus, simulates a grounded inductance with resulting value given by

$$L_{eq} = \frac{C}{4g_{m_1}g_{m_2}} \tag{2}$$

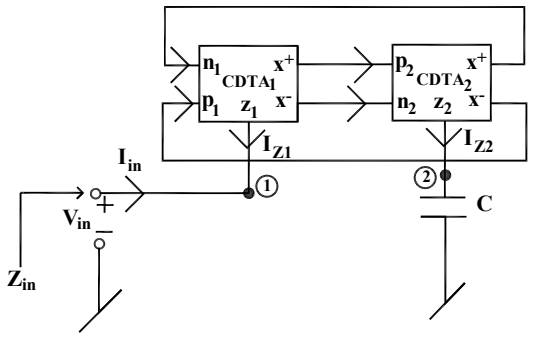

Fig. 1. Proposed grounded inductance simulation configuration.

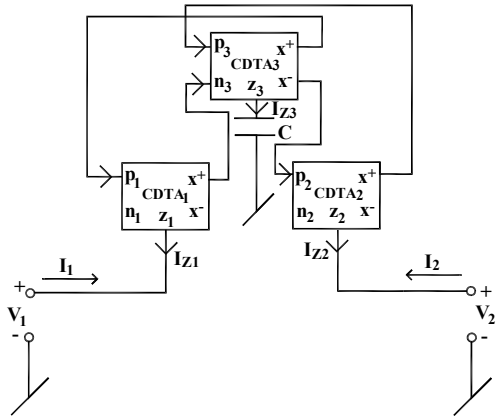

Fig. 2. Proposed floating inductance simulation configuration.

where g_{m1} and g_{m2} are the transconductances of CDTA1 and CDTA2, respectively.

Similarly, an analysis of the circuit shown in Fig. 2 yields

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{g_{m_3} g_m}{sC} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{3}$$

with $g_{m1} = g_{m2} = g_m$ which proves that the circuit simulates a floating lossless inductance with the resulting inductance value given by

$$L_{eq} = \frac{C}{g_{m_3} g_m}. \tag{4}$$

Note that ensuring $g_{m1} = g_{m2} = g_m$ requires only the equality of the two DC bias currents of the CDTAs which can be easily implemented in practice by ensuring equal dc bias currents in the two transconductance amplifiers.

3. Non-Ideal Analysis and Sensitivity Performance

Let R_p and R_n denote the input resistances of the p and n terminals of the CDTA respectively, C_Z and C_X denote the parasitic capacitances and R_Z and R_X denote the parasitic resistances of the Z and X terminals of the CDTA, respectively.

Assuming the external capacitance C to be much large than parasitic capacitances C_X and C_Z, considering R_Z to be much greater than g_{mi}; i=1,2, and, therefore, taking into account only the dominant non-ideal parasitic resistances R_p, R_n and R_X of the CDTA, the input impedance for the circuit shown in Fig. 1 is

$$Z_{in}(s) = \frac{V_{in}}{I_{in}} \cong \frac{sC}{g_{m_1} g_{m_2} \left\{ \frac{1}{\frac{R_p}{R_X}+1} + \frac{1}{\frac{R_n}{R_X}+1} \right\}^2} \tag{5}$$

which yields

$$L_{eq} = \frac{C}{g_{m_1} g_{m_2} \left\{ \frac{1}{\frac{R_p}{R_X}+1} + \frac{1}{\frac{R_n}{R_X}+1} \right\}^2}. \tag{6}$$

The sensitivities of L_{eq} with respect to active and passive elements are:

$$\begin{aligned} &S_C^{L_{eq}} = 1, \quad S_{g_{m_1}}^{L_{eq}} = -1, \quad S_{g_{m_2}}^{L_{eq}} = -1, \\ &S_{R_p}^{L_{eq}} = \frac{2R_p}{R_X \left\{ \frac{R_p}{R_X}+1 \right\}^2 \left\{ \frac{1}{\frac{R_p}{R_X}+1} + \frac{1}{\frac{R_n}{R_X}+1} \right\}}, \\ &S_{R_n}^{L_{eq}} = \frac{2R_n}{R_X \left\{ \frac{R_n}{R_X}+1 \right\}^2 \left\{ \frac{1}{\frac{R_p}{R_X}+1} + \frac{1}{\frac{R_n}{R_X}+1} \right\}}, \\ &S_{R_X}^{L_{eq}} = -\frac{2}{R_X \left\{ \frac{1}{\frac{R_p}{R_X}+1} + \frac{1}{\frac{R_n}{R_X}+1} \right\}} * \left\{ \frac{R_p}{\left\{ \frac{R_p}{R_X}+1 \right\}^2} + \frac{R_n}{\left\{ \frac{R_n}{R_X}+1 \right\}^2} \right\} \end{aligned} \tag{7}$$

Taking into account the non-idealities of the CDTA, namely

$$I_Z = (\alpha_p I_p - \beta_n I_n), \; V_p = V_n = 0,$$

$$I_X{}^+ = g_m V_Z \;\text{ and }\; I_X{}^- = -g_m V_Z$$

where

$$\alpha_p = (1 - \varepsilon_p); \quad \varepsilon_p << 1, \quad \beta_n = (1 - \varepsilon_n); \quad \varepsilon_n << 1$$

denote the current tracking errors.

For the circuit shown in Fig. 2, the non-ideal y-matrix is found to be

$$\begin{aligned} &\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{g_{m_3} g_m}{sC} \begin{bmatrix} \alpha_1\beta_3 & -\alpha_1\alpha_3 \\ -\alpha_2\beta_3 & \alpha_2\alpha_3 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \\ &\text{with} \quad g_{m_1} = g_{m_2} = g_m, \\ &\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{g_{m_3} g_m \alpha^2}{sC} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \\ &\text{with} \quad \alpha_1 = \alpha_2 = \alpha_3 = \beta_3 = \alpha \end{aligned} \tag{8}$$

yields

$$L_{eq} = \frac{C}{g_{m_3} g_m \alpha^2}. \quad (9)$$

The sensitivities of L_{eq} with respect to active and passive elements are:

$$S_{\alpha}^{L_{eq}} = -2, \quad S_{g_m}^{L_{eq}} = -1, \quad S_{g_{m3}}^{L_{eq}} = -1, \quad S_C^{L_{eq}} = 1. \quad (10)$$

From the above expressions, it is seen that all passive and active sensitivities of both the proposed circuits are low.

4. Verification of the Workability of the New Proposed Grounded / Floating Inductance Configurations

The workability of the proposed simulated inductors has been verified by realizing a band pass filter.

Fig. 3 shows the schematics for the realization of the band pass filter, using the new simulated grounded inductor.

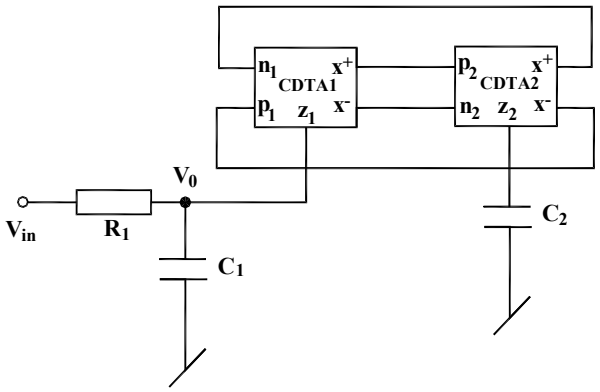

Fig. 3. Band pass filter realized by the new grounded simulated inductor.

The transfer function realized by this configuration is given by

$$\frac{V_0}{V_{in}} = \frac{\dfrac{s}{R_1 C_1}}{s^2 + \dfrac{s}{R_1 C_1} + \dfrac{4 g_{m_1} g_{m_2}}{C_1 C_2}} \quad (11)$$

Fig. 4 shows the schematics for the realization of the band pass filter, using the proposed floating inductor circuit.

The transfer function realized by this configuration is given by

$$\frac{V_0}{V_{in}} = \frac{s \dfrac{R_2 g_m g_{m_3}}{C_1}}{s^2 + s \dfrac{(R_1 + R_2) g_m g_{m_3}}{C_1} + \dfrac{g_m g_{m_3}}{C_1 C_2}}. \quad (12)$$

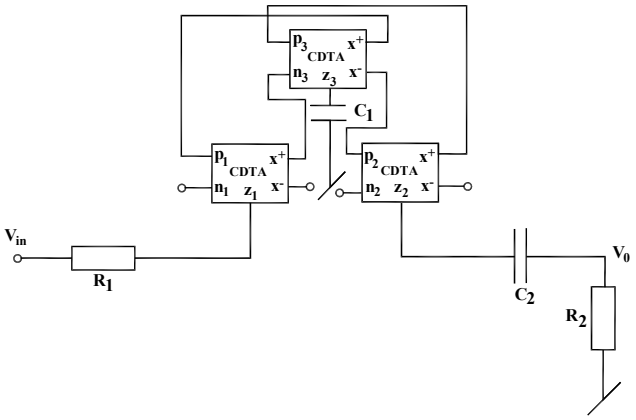

Fig. 4. Band pass filter realized by the new floating simulated inductor.

The performance of the new simulated inductors was evaluated by PSPICE (version 9.1) simulations. A CMOS implementation of the CDTA [13] was used to determine the frequency response of the grounded and floating simulated inductors. The following values were used for grounded inductor C = 0.3 nF, $g_{m1} = g_{m2}$ = 281.418 μA/V, for floating inductor C = 0.1 nF, $g_m = g_{m3}$ = 281.418 μA/V. From the frequency response of the simulated grounded inductor (Fig. 5) it has been observed that the inductance value remains constant up to 1 MHz (0.960 mH). From the frequency response of the simulated floating inductor (Fig. 6) it has been observed that the inductance value remains constant up to 1 MHz (1.284 mH).

To verify the theoretical analysis, the application circuits shown in Fig. 3 and Fig. 4 have been simulated using CMOS-based CDTA given in [13].The component values used for Fig. 3 C_1 = 1.577 nF, C_2 = 1 nF, R_1 = 1 kΩ, and for Fig. 4 C_1 = 0.04 μF, C_2 = 0.1 nF, R_1 = 1 kΩ, R_2 = 100 kΩ, the CDTA was biased with ± 2.5 volts DC power supplies with $I_{B1} = I_{B2}$ = 54 μA and I_{B3} = 32 μA. I_{B1} and I_{B2} are the biasing currents for the devices to perform the current differencing operation, while CDTA transconductance is controlled by I_{B3}. Fig. 7 and Fig. 8 show the simulated filter responses of the BP filters. Fig. 9 shows the unit step response of the filter of Fig. 3 which confirms the stability of the implemented filter. These results, thus, confirm the validity of the application of the proposed grounded / floating simulated inductance circuits.

5. Concluding Remarks

Among various modern active building blocks, CDTA is emerging as quite flexible and versatile for analog circuit design and has been used earlier for a variety of functions. However, the use of CDTA in the realization of grounded inductor had not been known earlier. This paper has filled this void by introducing a new CDTA-based grounded inductor and an alternative floating inductor (in addition to a CDTA-based floating inductor reported earlier in [23]) configurations. This paper, thus,

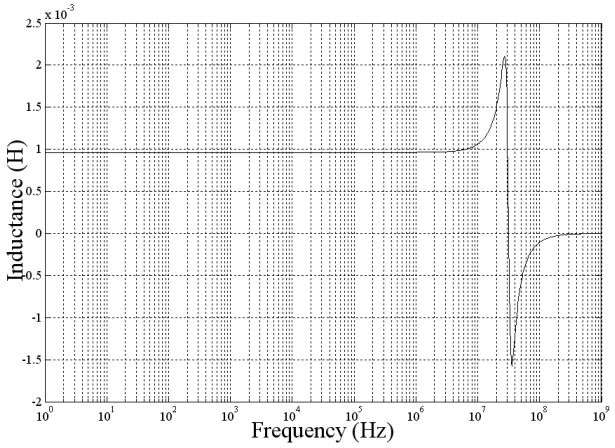

Fig. 5. Frequency response of simulated grounded inductor.

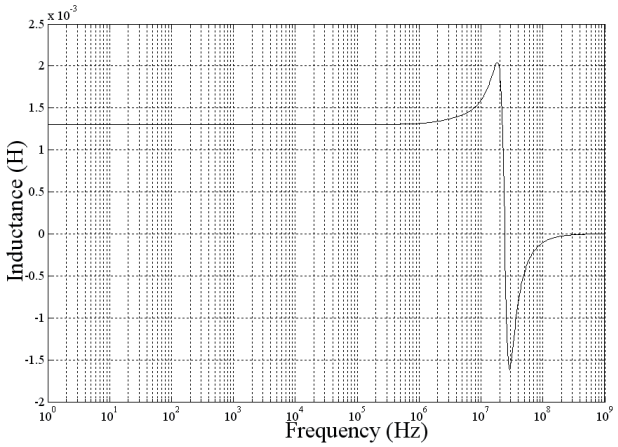

Fig. 6. Frequency response of simulated floating inductor.

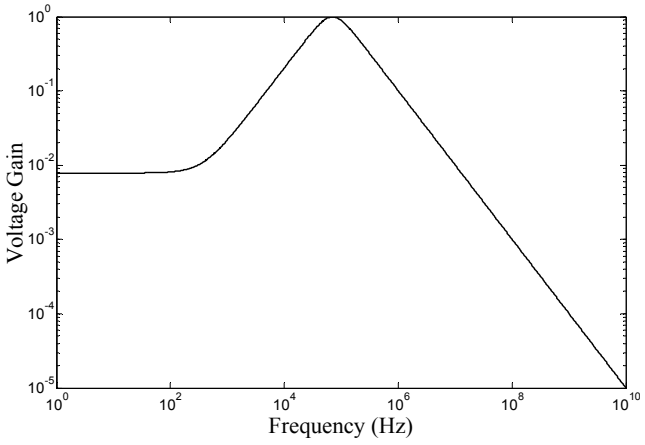

Fig. 7. Frequency response of BPF using simulated grounded inductor.

has added two new circuits to the existing repertoire of CDTA-based application circuits. SPICE simulations have established the workability of the proposed formulations.

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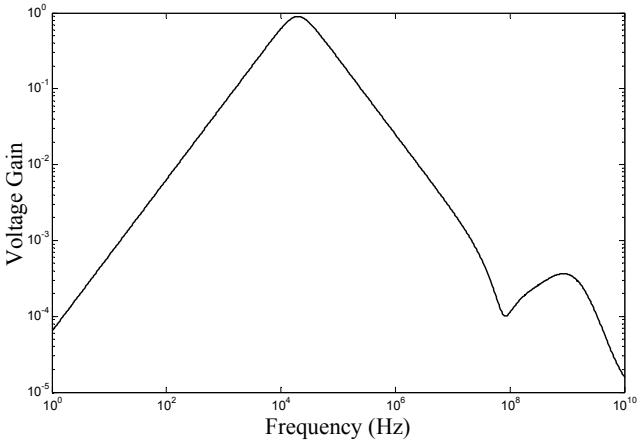

Fig. 8. Frequency response of BPF using simulated floating inductor.

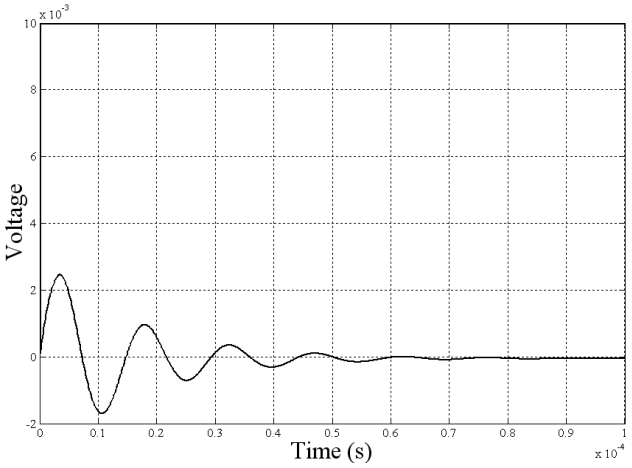

Fig. 9. Unit step response of Fig. 3.

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