A Novel Current-Mode Full-Wave Rectifier Based on One CDTA and Two Diodes

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Abstract. *Precision rectifiers are important building blocks for analog signal processing. The traditional approach based on diodes and operational amplifiers (OpAmps) exhibits undesirable effects caused by limited OpAmp slew rate and diode commutations. In the paper, a full-wave rectifier based on one CDTA and two Schottky diodes is presented. The PSpice simulation results are included.*

Keywords

Current–mode rectifier, CDTA.

1. Introduction

The current-mode approach offers a promising way of revising traditional circuits towards different and more elegant solutions [1]. The current–mode operation has proved its usefulness in a lot of application areas, not only in linear circuits such as active filters but also in non–linear blocks such as triggers, relaxation oscillators or precision rectifiers [2–21]. The potential advantages of the current–mode circuits are wide dynamic range, good linearity over the full operational range, low temperature sensitivity, and low power supply voltages.

Precise circuits for the rectification of low–level signals play an important role in analog signal processing. Conventional rectifiers based on voltage–feedback operational amplifiers (OpAmps) and diodes produce the well–known distortion due to the combination of OpAmp finite slew rate and effects caused by diode commutation. This distortion increases for lower levels and higher frequencies of the signals being processed. As a result, the rectifier operates well in the frequency range deep below the gain–bandwidth product of the OpAmp used.

Many current–mode full–wave rectifiers have been reported in the literature [22–32]. They provide rectification with the aim of maximizing the operation frequency of low–level input signals. However, the reported rectifiers usually employ at least two current–mode active elements, four diodes, and additional subcircuits. The well–known principle of precise current–conveyor rectification, first reported in [22, 23], uses two CCII+ and four diodes. To eliminate the delay introduced by diodes when switching between the ON and OFF states, several types of auxiliary biasing or bias cancellation circuits have been proposed [25–27], which make the circuit concept more complicated. A simplification of the two–CCII version of rectification is described in [32], utilizing one CDTA (Current Differencing Transconductance Amplifier) element [33–36] and four diodes.

A novel current–mode full–wave rectifier based on one CDTA and two diodes is introduced in this paper. To verify its functionality, PSpice simulations are performed, utilizing the respective model of the CDTA. Several recent works propose transistor–level CDTA structures in the CMOS [34], [37–39] and also in bipolar [40–41] technologies. In [42], a SPICE model that truly describes the behavior of the CDTA chip, fabricated in the 0.7um CMOS technology [43], is mentioned. However, all the above CDTA implementations have a drawback consisting in the non–linear current–to–voltage DC characteristics of the OTA stage and also in the rather low levels of output currents. This can be in conflict with the demand for the precision rectification of signals with amplitudes varying over a high dynamic range.

As a consequence of the above facts, the CDTA used in this paper is built up from commercial diamond transistors [44]. Utilizing the technique of degeneration resistors, they provide linear regime of operation up to currents of several milliampers. The rectification is verified via PSpice simulation.

2. CDTA

Current differencing transconductance amplifier (CDTA) with its schematic symbol in Fig. 1 is an active circuit element introduced in [33]. Its parasitic input capacitances have a negligible effect due to low impedance levels. The CDTA operates in a wide frequency range due to its current–mode operation.

The input stage is driven by two input currents, I_p and I_n. Their difference is transferred as a current I_z to the high–

impedance *z* terminal. Here it is converted to a voltage via external impedance. This *z*–terminal voltage is then converted to output currents I_x via a multiple–output transconductance stage with a transconductance g_m.

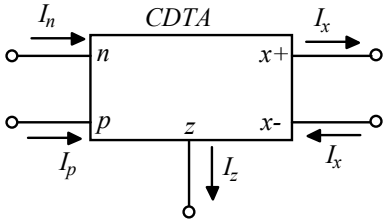


Fig. 1. The CDTA schematic symbol.

The idealized CDTA is characterized by the following equations:

$$V_p = V_n = 0\,, \tag{1}$$

$$I_z = \alpha_p I_p - \alpha_n I_n\,, \tag{2}$$

$$I_x = g_m V_z \tag{3}$$

where the current gains α_p and α_n are equal to 1 in the ideal case. Fig. 2 shows possible implementations of the CDTA using commercially available circuits, namely OPA860, containing the so–called diamond transistors (DTs) and diamond buffers (DBs) [44]. The diamond transistor with B (base), C (collector) and E (emitter) terminals behaves like a current conveyor CCII with the corresponding *Y*, *Z*, and *X* terminals. When properly biased, the transconductance g_m of the diamond transistor is about 100 mA/V, ensuring a low input resistance of about 10 Ω of the *n* and *p* terminals in Fig. 2. The input current I_n is conveyed to the collector of DT_1, and here it is subtracted from the input current I_p. The difference current I_p–I_n is conveyed to the collector of DT_2, which is connected directly to the *z* terminal of the CDTA.

Figs 2 (a), (b), and (c) show three methods of OTA implementation via DT_3 and DT_4. The transistors are complemented with degeneration resistors $R_g >> 1/g_m$ in order to increase the OTA linearity and decrease the offset value [45]. The OTA transconductance (g_m) is then approximately given by the reciprocal value of R_g. The OTAs in Figs 2 (a) and (b) have bipolar outputs, which corresponds to the notation "CDTA+–". In Fig. 2 (c), the "CDTA++" contains an OTA with unipolar outputs as its terminal stage.

From the point of view of large–signal DC responses, all the CDTA versions in Fig. 2 have similar characteristics shown in Fig. 3. These results were obtained under the following conditions: OPA860 is biased by supply voltages ±5V, with R_{set} = 330 Ω (for details, see [44]). The values of degeneration resistors R_g are set to 1 kΩ, and the corresponding transconductance of the CDTA is approximately 1 mS. The *z* terminal is grounded via a 1 kΩ resistor throughout the test.

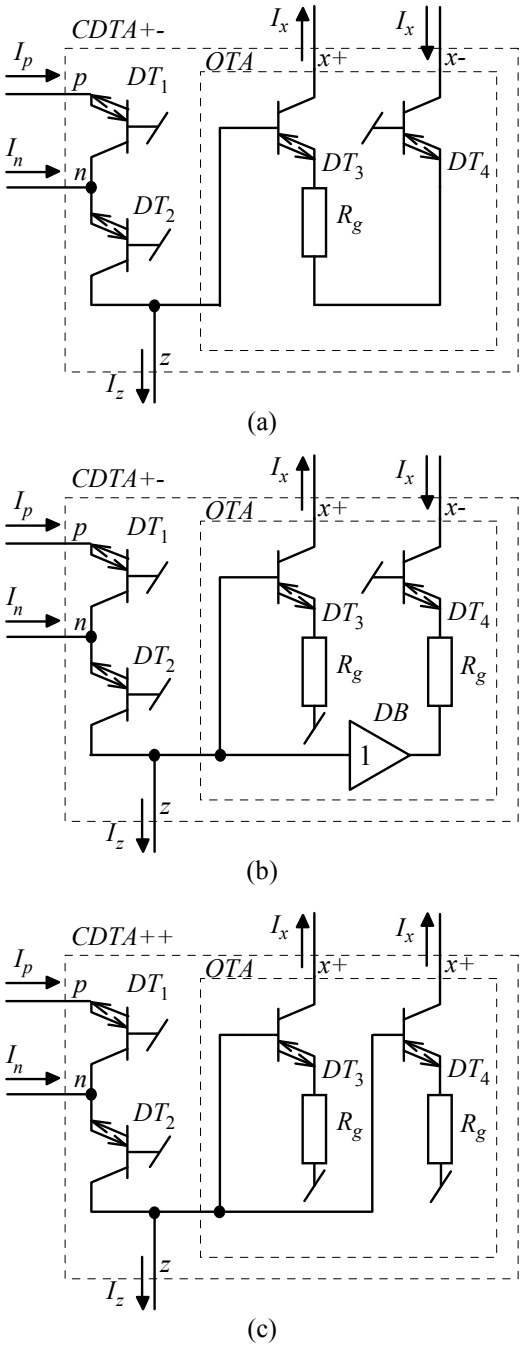
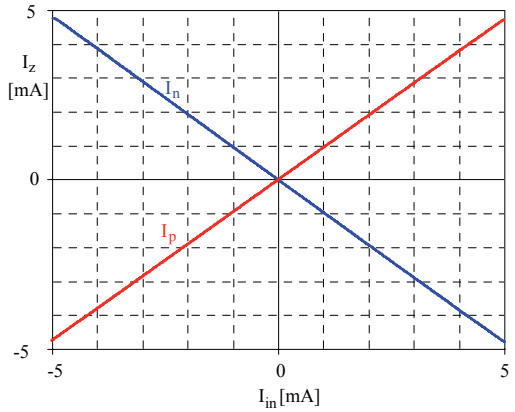


Fig. 2. Possible implementations of the CDTA with three types of OTA stage.

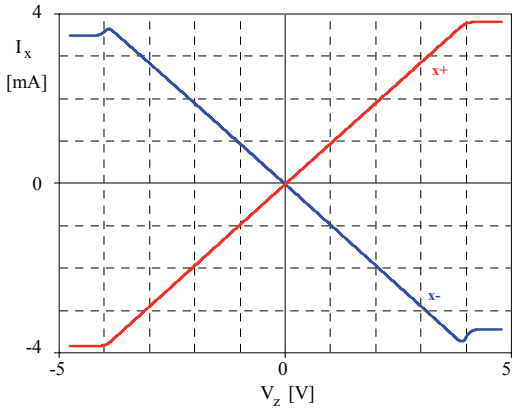
A detailed SPICE analysis of the above characteristics reveals that the CDTA++ in Fig. 2 (c) has the best parameters among all three CDTA implementations from the point of view of low current offset (2.2 μA *x*–terminal offset). Since the offset of the output current is an important feature of current–mode rectifiers, the following analysis will be confined to the CDTA++ in Fig. 2 (c). The small–signal parameters of this CDTA version are as follows:

$$\alpha_p \approx 0.951,\ \alpha_n \approx 0.965,\ g_m \approx 0.969\ \text{mA/V}\,. \tag{4}$$

AC analysis reveals the flat frequency responses of the above parameters with a –3 dB cutoff frequency of about 40 MHz.



(a)



(b)

Fig. 3. Results of DC analysis of CDTAs in Fig. 2, with z terminal grounded via 1 kΩ resistor, (a) I_z versus I_p and I_n, (b) I_{x+} versus V_z (all CDTAs in Fig. 2), I_{x-} versus V_z (CDTAs (a) and (b) in Fig. 2).

3. Full-Wave CDTA–Based Rectifier

To achieve full–wave precision rectification, the CDTA is connected to two diodes as shown in Fig. 4. Note that with the z–terminal open, the CDTA behaves like a True Current Operational Amplifier (TCOA), i.e. a current source controlled by the difference of input currents, with very high current gain [7]. Since I_z = 0, the following condition is fulfilled:

$$I_p = I_n . \tag{5}$$

For a positive input current I_{in}, D_1 (D_2) is in ON (OFF) state, and this current flows through D_1 to the p terminal of the CDTA. According to (5), identical currents must flow from the upper x+ terminal to the n terminal, and also from the lower x+ terminal to the ground through a load R_L. If the polarity of the input current changes, D_1 (D_2) is in OFF (ON) state. Then $I_p = 0$ and thus $I_n = 0$, and I_{in} flows through D_2 from the upper x+ terminal. An identical current must flow from the lower x+ terminal through the load to the ground. In other words, this circuit behaves like a full–wave rectifier.

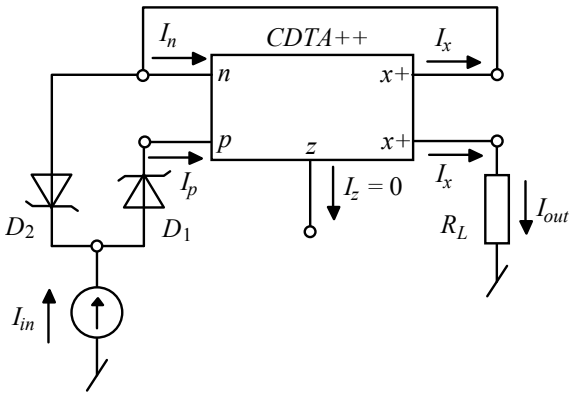


Fig. 4. Full–wave rectifier based on CDTA and two diodes.

Spice simulations confirm the basic functionality of this circuitry. The CDTA was modeled according to Fig. 2 (c), with the SPICE model of OPA 860 from [46]. The transconductance g_m was set via R_g = 1 kΩ to an approximate value of 1 mA/V. Fast Schottky diodes 1PS79SB63 were used [47]. The load resistance R_L was set to 1 Ω.

Fig. 5 shows the DC transfer characteristic, which confirms precise rectification over a wide range of input currents [-3 mA, 3 mA]. As can be seen from the detail in Fig. 5, the offset of the output current is approximately 1.72 μA, and the large–signal positive and negative slopes of the characteristic are 0.961 and 0.978, respectively. These imperfections will be discussed in more details in Section 4.

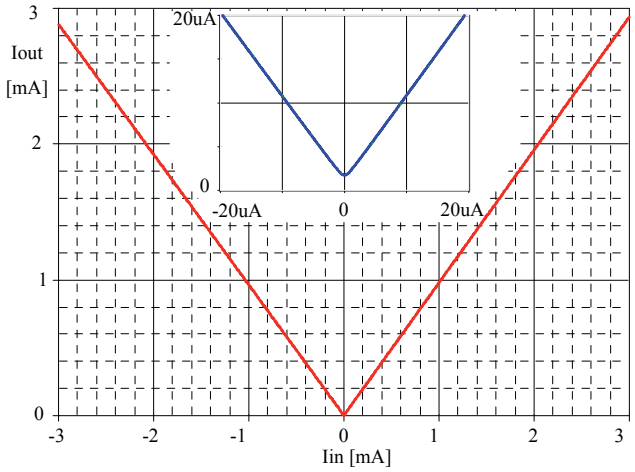


Fig. 5. Simulated DC output/input characteristic of current–mode rectifier, temperature = 27°C.

The rectifier was then excited by a current source with a magnitude of 50 μA and a frequency of 5 MHz. The load resistance R_L was set to 1 Ω. The rectified waveform of the output current is shown in Fig. 6 together with the input signal.

In order to analyze the performance of the proposed rectifier more rigorously, an analysis of real influences is given in the next Section.

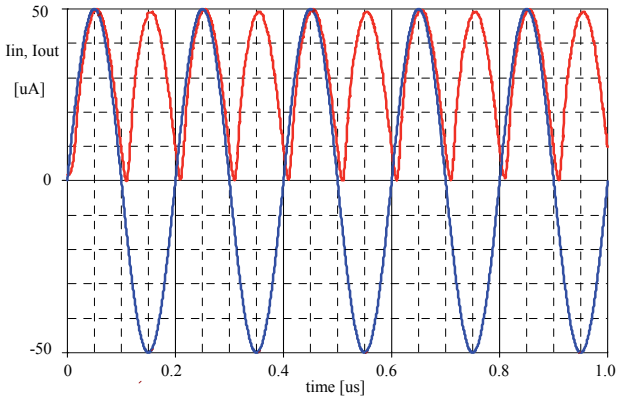


Fig. 6. Simulated waveforms of the input and output currents.

4. Non–Ideal Analysis

As shown in Fig. 5, the DC precision of the rectifier can be evaluated via the values of the current offset and the slopes of the DC characteristic, which should be +1 and –1 in the ideal case. In addition, the above DC analysis was performed on the assumption of the rectifier being excited by an ideal current source, without considering the influence of the internal impedance of this source. One can expect that the high–impedance input node can be a source of potential problems. All these factors should be examined carefully.

The transient analysis in Fig. 6 is done only for fixed values of the frequency and the amplitude of the input signal. It is useful to evaluate the quality of the rectification for larger range of the above signal parameters.

4.1 Low–Frequency Behavior

Fig. 7 shows the effect of the finite input resistance of current source I_{in} on the DC characteristic of the rectifier. Note that this resistance does not affect the current offset but it can decrease significantly the slopes discussed above. To eliminate this phenomenon, one should choose the source I_{in} with sufficiently high resistance (preferably more than 500 kΩ).

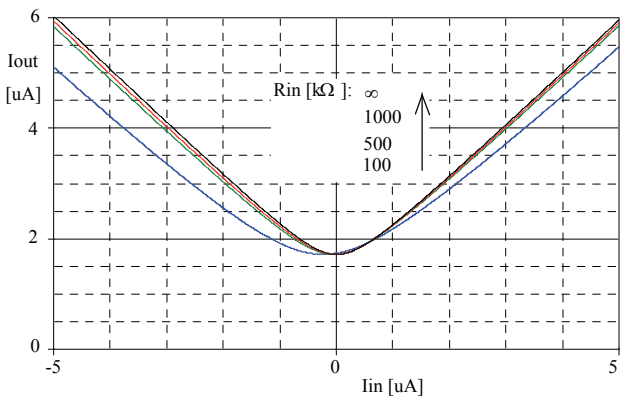


Fig. 7. DC characteristic of the rectifier for different values of the resistance of input current source.

Since the diodes D_1 and D_2 are current–controlled, the current offset of the rectifier is determined by the offset properties of the diamond transistors, which are the building components of the CDTA.

A simple analysis of the offset properties of diamond transistors is given in [45]. A more general analysis is needed for evaluating the DC inaccuracy of the rectifier proposed in Fig. 4. The DC characteristics of transistor No. i, i = 1, 2, 3, and 4 of the CDTA in Fig. 2 (c) can be approximated in the vicinity of the origin of the coordinates by linear dependences

$$I_{ei} = g_{mi}(V_{bei} + \Delta V_i)\,, \tag{6}$$

$$I_{ci} = \alpha_{ci} I_{ei} + \Delta I_{ci}\,. \tag{7}$$

Here, I_{ei}, I_{ci}, and V_{bei} are emitter and collector currents and voltages between the base and emitter of transistor No. i. The symbols ΔV_i and ΔI_{ci} denote the voltage and current offsets of transistor No. i, with their typical values of 3 mV and 18 μA. The tracking coefficients α_{ci}, which are equal to 1 in the ideal case, are typically about 0.98. The transconductance g_{mi} depends on the DC biasing. It is adjusted to ca 100 mA/V for our purposes, as also mentioned in Section 3.

Fig. 8 is built up from Figs 2 (c) and 4 with the aim to reveal the key sources of DC inaccuracies of the rectifier. The input resistance of the current source is not taken into account here, because its value is sufficiently high (see Fig. 7).

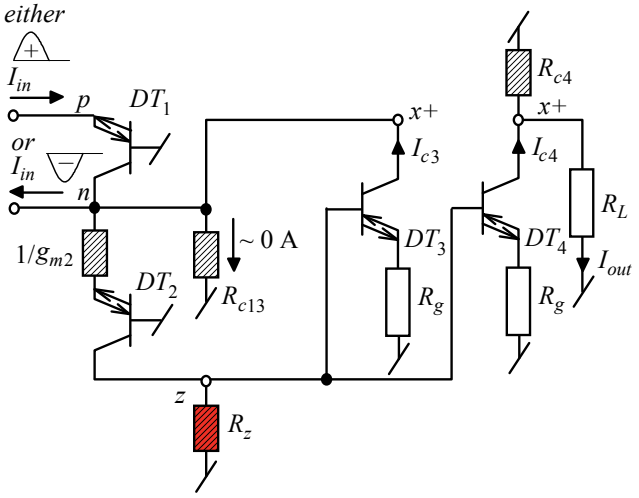


Fig. 8. Auxiliary schematic for the error analysis of DC behavior of the rectifier in Fig. 2 (c).

If positive, the input current flows into the p terminal, otherwise it flows out of the n terminal. Since the emitter current of DT_1 is not affected by the transconductance of this transistor, g_{m1} is not denoted in Fig. 8 as an error parameter. R_{c13} models the parasitic resistance which is formed by the collector resistances of DT_1 and DT_3 (54 kΩ is a typical value of each, thus $R_{c13} \approx 27$ kΩ). R_z is a parasitic resistance formed by the collector resistance of DT_2

and base resistances of DT_3 and DT_4. Since the base resistances are high (typically 455 kΩ each), then $R_z \approx 54$ kΩ.

Since $R_{c13} >> 1/g_{m2}$, the current flowing through R_{c13} can be neglected. That is why R_{c13} and $1/g_{m2}$ are not key elements, which would generate the DC error. Also, the influence of parasitic resistance R_{c4} can be neglected because it is damped by $R_L << R_{c4}$. In the following, the error analysis will be performed with respect to the influence of *DT* inaccuracies described by (6), (7) and the parasitic resistance R_z. The aim of the analysis is to find a mathematical model of the current I_{out}.

After modeling each *DT* in Fig. 8 via (6) and (7), and also taking the inequality $1/g_{m3} << R_g$ into account, the analysis of the circuit in Fig. 8 leads to the following results:

for $I_{in} > 0$:

$$I_{c3} = \alpha_{3+} I_{in} + \Delta I_3 , \tag{8}$$

for $I_{in} < 0$:

$$I_{c3} = \alpha_{3-} I_{in} + \Delta I_3 , \tag{9}$$

where

$$\alpha_{3+} = \frac{R_z}{R_g} \frac{\alpha_{c1}\alpha_{c2}\alpha_{c3}}{1 + \alpha_{c2}\alpha_{c3}\dfrac{R_z}{R_g}},\ \alpha_{3-} = -\frac{R_z}{R_g} \frac{\alpha_{c2}\alpha_{c3}}{1 + \alpha_{c2}\alpha_{c3}\dfrac{R_z}{R_g}},$$
$$\Delta I_3 = \frac{\dfrac{R_z}{R_g}\alpha_{c3}(\Delta I_{c2} - \alpha_{c2}\Delta I_{c1}) + \alpha_{c3}\dfrac{\Delta V_3}{R_g} + \Delta I_{c3}}{1 + \alpha_{c2}\alpha_{c3}\dfrac{R_z}{R_g}}, \tag{10}$$

and

for $I_{in} > 0$:

$$I_{out} = \alpha_{out+} I_{in} + \Delta I_{out} , \tag{11}$$

for $I_{in} < 0$:

$$I_{out} = \alpha_{out-} I_{in} + \Delta I_{out} , \tag{12}$$

where

$$\alpha_{out+} = \frac{R_z}{R_g} \frac{\alpha_{c1}\alpha_{c2}\alpha_{c4}}{1 + \alpha_{c2}\alpha_{c3}\dfrac{R_z}{R_g}},\ \alpha_{out-} = -\frac{R_z}{R_g} \frac{\alpha_{c2}\alpha_{c4}}{1 + \alpha_{c2}\alpha_{c3}\dfrac{R_z}{R_g}},$$
$$\Delta I_{out} = \alpha_{c4}\frac{R_z}{R_g}\frac{\Delta I_{c2} - \alpha_{c2}(\Delta I_{c1} + \alpha_{c3}\dfrac{\Delta V_3}{R_g} + \Delta I_{c3})}{1 + \alpha_{c2}\alpha_{c3}\dfrac{R_z}{R_g}} + \alpha_{c4}\frac{\Delta V_4}{R_g} + \Delta I_{c4} . \tag{13}$$

Equations (8) to (13) offer a comparison of the rectifier accuracy in terms of rectified currents I_{c3} and $I_{c4} \approx I_{out}$.

Recall that DT_3 and DT_4 form a double–output OTA. For identical and ideal transistors DT_3 and DT_4, the currents I_{c3} and I_{c4} should be equal. Let us show that in a real case, the accuracy of the rectification is higher for the current I_{c3} than for I_{c4}.

Note that equations (11) and (12) or (8) and (9) represent a simple mathematical model of the DC characteristic of the rectifier in Fig. 5.

The positive and negative slopes of the characteristics are not equal in their absolute values when the tracking coefficient of DT_1 is not equal to one. Also note that the voltage offsets of DT_3 and DT_4 do not contribute to the total current offset of the rectifier when the degeneration resistance R_g is high enough. For $R_z >> R_g$ (theoretically for $R_z \to \infty$),

$$\alpha_{3+} = \alpha_{c1},\ \alpha_{3-} = -1,\ \Delta I_3 = \frac{\Delta I_{c2}}{\alpha_{c2}} - \Delta I_{c1} . \tag{14}$$

For high values of parasitic R_z, the deviation of the positive slope from its ideal value 1 is caused only by the inaccuracy of transistor No. 1, and the negative slope is set accurately. The current offset is then determined by the current offsets of transistors No. 1 and 2, which can partially compensate each other. For finite values of R_z, other inaccuracies of all transistors have a chance to contribute to the DC imperfections of the rectification process according to (8)–(10).

For high values of R_z, equations (13) for I_{out} are different from (14):

$$\alpha_{out+} = \frac{\alpha_{c1}\alpha_{c4}}{\alpha_{c3}},\ \alpha_{out-} = -\frac{\alpha_{c4}}{\alpha_{c3}} , \tag{15}$$
$$\Delta I_{out} = \alpha_{c4}\left(\frac{\Delta I_{c2}}{\alpha_{c2}\alpha_{c3}} - \frac{\Delta I_{c1} + \Delta I_{c3}}{\alpha_{c3}} + \frac{\Delta V_4 - \Delta V_3}{R_g}\right) + \Delta I_{c4} .$$

Since the formulae in (15) are functions of error terms of more transistors than in (14), and because these terms are uncorrelated for the individual transistors, the worst–case analysis leads to the conclusion that the current I_{out}, compared with the current I_{c3}, can exhibit a potentially larger spread of the values of the slopes "alpha" and also a larger current offset. For example, even if the tracking coefficients of all transistors were exactly one, the maximum offset of I_{out} would be two times greater than for I_{c3}. That is why the question of applying existing methods for offset reduction and bias cancellation technique [26–27], [32] is topical also for this circuitry if extra–low current rectification is required.

4.2 High–Frequency Behavior

In addition to the high–frequency characteristics of the CDTA and the switching properties of the diodes, the high–frequency behavior of the rectifier will be probably

influenced also by the parasitic capacitance of the high-impedance input node. This phenomenon will be studied first. Then a detailed analysis of the rectifier will be performed in terms of the applied sinusoidal input source with various values of frequency and magnitude, and its AC responses will be evaluated via the concept of the so–called GFR (Generalized Frequency Response) [48].

Fig. 9 shows a similar transient analysis as in Fig. 6, i.e. under the rectifier excitation by 50 μA/5 MHz sinusoidal current source, but now with the 1 MΩ/2 pF input impedance taken into consideration. A comparison with Fig. 6 shows a deformation of the output pulses. The reason is obvious from the waveforms I_{d12} (summing current through diodes D_1 and D_2) and I_{cap} (current through the parasitic capacitance) in Fig. 9. The superposition of these two curves gives the waveform of I_{in}. Since the magnitude of I_{cap} is not negligible at 5 MHz, the current, flowing through the diodes to the rectifier, is subject to a distortion which increases with growing frequency. To preserve good high–frequency behavior of the rectifier, it is necessary to keep the parasitic capacitance of the input node as low as possible.

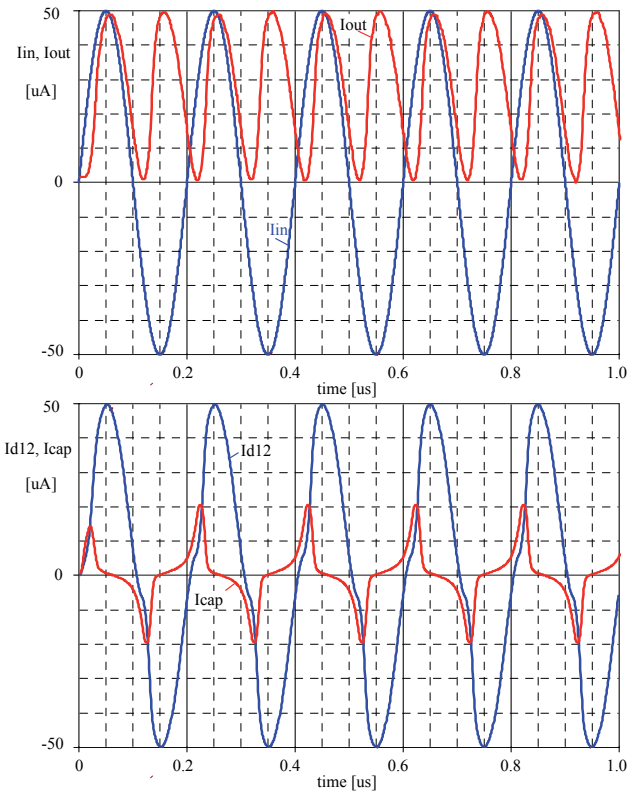


Fig. 9. The waveforms simulated for the input impedance 1 MΩ/2 pF. In the bottom figure, I_{d12} is total current flowing through diodes, and I_{cap} is current through the parasitic capacitance.

Since the rectifier is a highly–nonlinear device, the conventional AC analysis cannot be used for evaluating the quality of its high–frequency operation. On the other hand, it is useful to have a model of the rectification process quality as a function of the magnitude and frequency of the input signal. In order to provide it, let us use the concept of the above mentioned GFR, which works under the following conditions [48]:

(a) The rectifier is excited from a single source of harmonic signal $i(t)$ of frequency f and magnitude I_{max}. The frequency and the magnitude can be selected from the intervals $F \in \langle f_1, f_2 \rangle$ and $I \in \langle I_{max1}, I_{max2} \rangle$.

(b) The rectifier operates in the periodical steady–state.

(c) For concrete $f \in F$, $I_{max} \in I$, the periodical steady state will be evaluated by the so–called one–point characteristic p of selected signals of the rectifier. This characteristic should be chosen such that it is a measure of the quality of rectification. In [48], two types of the characteristic are proposed: The first is the ratio of the average values of the rectified output signal i_{out} and the average value of the sinusoidal input signal after its ideal full–wave rectification p_{AVR} (AVR = Average Value Ratio):

$$p_{AVR} = \frac{\frac{1}{T}\int_T i_{out}(t)dt}{\frac{2}{\pi} I_{\max}}. \tag{16}$$

Here, T is the signal repetition period. The ideal operation of the rectifier is then characterized by the value $p_{AVR} = 1$. When increasing the frequency and decreasing the magnitude of the input signal, the deflection from the ideal operation is indicated by a change, mostly a decrease in p_{AVR} below one.

The second type of the characteristic is defined more rigorously as a ratio of two RMS values, the RMS of the difference of the real and ideal output signals, i_{out} and i_{ideal}, and the RMS value of the ideal signal:

$$p_{RMSE} = \frac{\sqrt{\frac{1}{T}\int_T [i_{out}(t) - i_{ideal}(t)]^2 dt}}{\frac{1}{\sqrt{2}} I_{\max}}. \tag{17}$$

Here, the subscript RMSE is an abbreviation of the term “Root Mean Square Error”. For ideal circuit operation, i.e. $i_{out}(t) = i_{ideal}(t)$, the result is $p_{RMSE} = 0$, while in the case of total attenuation of the output signal it is $p_{RMSE} = 1$. For extra high distortions, when the mutual energy of signals i_{out} and i_{ideal} can be negative, one can obtain $p_{RMSE} > 1$.

(d) For $F \in \langle f_1, f_2 \rangle$ and $I \in \langle I_{max1}, I_{max2} \rangle$, the one–point characteristic p varies within the interval $P \in \langle p_{min}, p_{max} \rangle$.

Then the mapping

$$K: (F,I) \rightarrow P \tag{18}$$

is called Generalized Frequency Response (GFR) K of the rectifier.

The paper [48] describes a procedure of the SPICE analysis of the functional relations

$$p = p(f, I_{\max}), f \in F, I_{\max} \in I, \tag{19}$$

and their interpretation as a set of frequency characteristics, with the magnitude of the input signal as a parameter.

The generalized frequency responses, i.e. AVR and RMS error versus frequency are shown in Figs 10 (for the parasitic capacitance 2 pF of the input node) and 11 (for 5 pF), respectively. These results were obtained via a multiple run of PSpice transient analysis with the frequency of the exciting current stepped, and with subsequent application of the performance analysis. This analysis is supported by special functions for computing the AVR and RMSE values. The measuring functions, programmed in PROBE (OrCAD PSpice v. 16), can identify automatically the last period of the signal and evaluate the *p*–characteristics defined by (16) and (17).

The analysis of Fig. 10 (a) reveals that for a parasitic capacitance of 2 pF, the 1 mA sinusoidal current is rectified properly in a wide frequency range, providing a correct average value up to the –3dB cutoff frequency of about 82 MHz. The corresponding curve of RMS error in Fig. 10 (b) starts from the value of 44m at 1 MHz, reflecting the fact that the waveforms of the input and output currents are not identical (current offset, diode commutation effects, etc.), with RMSE increasing with growing frequency (the effect of parasitic capacitance and dynamic limitations of CDTA and diodes). For lower magnitudes of the rectified current, the cutoff frequency decreases to 15.1 MHz for I_{max} = 100 μA and 4.9 MHz for I_{max} = 10 μA. The latter case shows that the low–frequency AVR value is greater than 0 dB. It is caused by the output offset, which is comparable with the signal magnitudes, increasing the average value of the output current. The corresponding RMS error is high. Several RMSE curves show a "saw–tooth" pattern due to numerical problems with automatic detection of the repetition period in PROBE.

In Fig. 11, the frequency responses are analyzed for the 5 pF parasitic capacitance. Note that the rectifier bandwidth is now decreasing to 42.7 MHz, 7.6 MHz, and 2.4 MHz for I_{max} = 1 mA, 100 μA, and 10 μA, respectively.

5. Conclusion

A novel current–mode full–wave rectifier based on CDTA and two diodes has been presented in the paper. In comparison with the hitherto published current–mode rectifiers, this solution is more economical, employing only one active element, CDTA in this case, and two diodes. For CDTA constructed from commercial integrated circuits (OPA 860), a detailed error analysis has been performed to evaluate DC precision and high–frequency performance. The PSpice simulations confirm good operation of this circuit in a wide frequency range for the amplitude of input

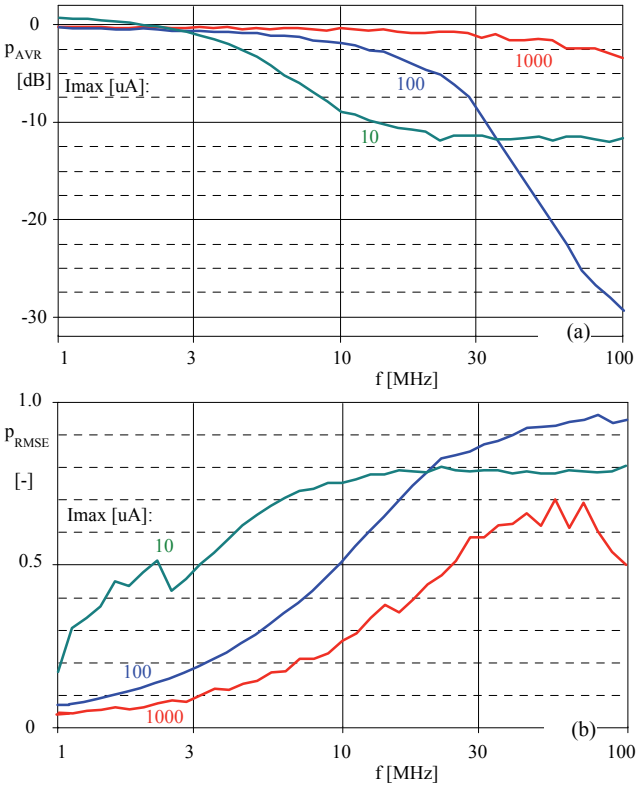


Fig. 10. Generalized frequency responses of the rectifier for the input node impedance 1 MΩ/2 pF: (a) AVR (Average Value Ratio) versus frequency, (b) RMS error versus frequency, for three amplitudes of the input current.

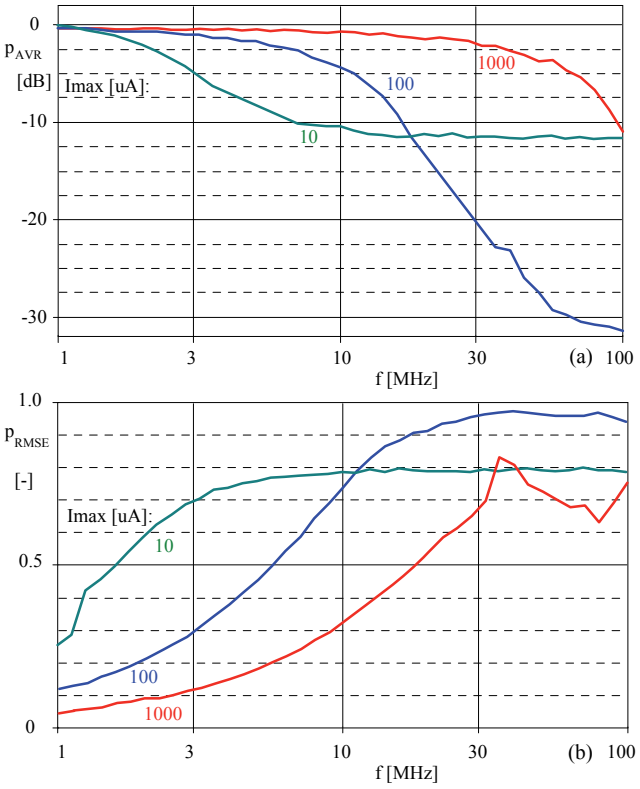


Fig. 11. Generalized frequency responses of the rectifier for the input node impedance 1 MΩ/5 pF: (a) AVG versus frequency, (b) RMS error versus frequency.

current varying within three decades. The weak point of this circuit is its high–impedance input node, whose parasitic capacitance should be maintained as low as possible. The error analysis, presented in the paper, particularly the approach of generalized frequency responses, easily implemented in SPICE, can serve as a useful tool for a quantitative evaluation of the quality of rectification, and thus for a conclusive comparison of the performance of various topologies of current– or voltage–mode rectifiers.

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