

The Effects of Interference Suppression by a Reconfigurable Structure at DSSS-DPSK Receiver

Nenad MILOŠEVIĆ, Zorica NIKOLIĆ, Bojan DIMITRIJEVIĆ, Bojana NIKOLIĆ

Dept. of Telecommunications, University of Niš, Aleksandra Medvedeva 14, 18000 Niš, Serbia

{nenad.milosevic, zorica.nikolic, bojan.dimitrijevic, bojana.nikolic}@elfak.ni.ac.rs

Abstract. In this paper we show the performances of DSSS-DPSK receiver where the interference rejection circuit is reconfigurable and is using ξ -structure. The results will be shown for the case of packet, as well as for the continuous QPSK interference. The results show that the proposed reconfiguration circuit, in case of packet QPSK interference, significantly decreases the error probability, compared to the system using only ξ -structure for signal to noise ratios of practical importance. Also, in case of continuous interference, the reconfigurable structure has equally good performance, regardless of interference power and its bitrate.

Keywords

Interference suppression, spread spectrum system, reconfiguration, error probability.

1. Introduction

The suppression of digitally modulated interference at DSSS/QPSK system using complex adaptive transversal filter [1] is not as successful as the suppression of single or multiple tone interference [2]. This is more pronounced for high interference bitrate when the interference is wideband. Because of this, in [3] a ξ -structure is proposed, and it can be successfully applied for the suppression of interference with a number of different digital modulation formats, regardless of its bitrate. However, in order to ξ -structure performs well, it is necessary to interference power be higher than some minimum threshold value. Therefore, in this paper we proposed a reconfigurable receiver with ξ -structure for the interference suppression. The use of reconfigurable interference rejection structure is especially important for cognitive and software radio [4]. Also, it should be pointed out that most of modern telecommunication systems use packet transmission [5]. It is of high importance to see how the packet nature of the system influences the interference suppression filters.

In this paper we will consider the performances of

DSSS-DPSK receiver where the interference rejection circuit is reconfigurable in cases of packet and continuous interference. Having in mind that the cognitive radio systems are meant to work in frequency ranges that are already in use, there may be a wide variety of interfering modulation formats. As an example of interference, QPSK interference has been chosen.

2. System Model

Block diagram of the receiver is shown in Fig. 1. The useful signal is given as

$$s(t) = d(t) \cdot d(t - Q \cdot \Delta) \cdot m(t) \cdot \cos(\omega_c t + \theta) \quad (1)$$

where $m(t)$ is the PN sequence with chip interval Δ ; $d(t)$ is the information data with bit interval $T = Q\Delta$, ω_c is the carrier frequency, θ is the signal phase, and Q is the processing gain. Besides the useful signal and noise, there is a QPSK interference at the input of the receiver:

$$i(t) = \sqrt{J} p(t) \cdot a(t) \cdot \cos(\omega_i t + \varphi_i) \quad (2)$$

where J is the interference power, $a(t)$ is the interference information data, ω_i is the interference carrier frequency, and φ_i is a random phase with uniform distribution on $(0, 2\pi]$. Variable that describes the packet nature of the interference is

$$p(t) = \begin{cases} 1, & \text{mod}[t/\Delta, (T_s + T_p)/\Delta] < T_s/\Delta \\ 0, & \text{mod}[t/\Delta, (T_s + T_p)/\Delta] \geq T_s/\Delta \end{cases} \quad (3)$$

where T_s is interference packet duration, and T_p is time interval between two packets. For example, $p(t) = 1$ for continuous PSK interference. Let us define the ratio between T_p and T_s (duty cycle) as $\delta = T_p/(T_s + T_p)$.

Signal at the input of the receiver is given by:

$$x(t) = s(t) + i(t) + n(t) \quad (4)$$

where $n(t)$ is the random Gaussian noise with zero mean and variance σ^2 .

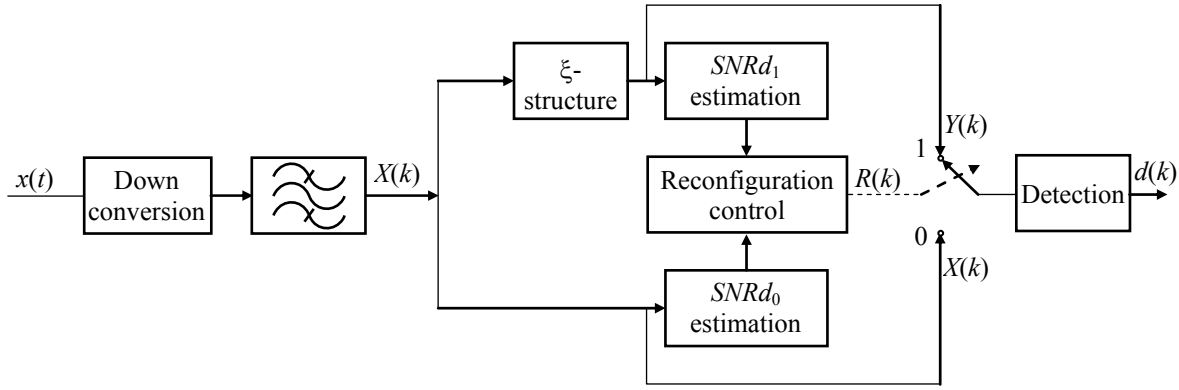


Fig. 1. DSSS/DSPK receiver block diagram

After the input signal down conversion and filtering, the receiver performs sampling. For k th sample, received signal may be represented in complex form as

$$X(k) = S(k) + I(k) + N(k) \quad (5)$$

where

$$S(k) = s_1(k) + js_2(k), \quad (6)$$

$$s_1(k) = d(k) \cdot d(k-Q) \cdot m(k) \cdot \cos \theta \quad (7)$$

$$s_2(k) = d(k) \cdot d(k-Q) \cdot m(k) \cdot \sin \theta$$

$$I(k) = \sqrt{J} p(k) \cdot a(k) \cdot \exp(j(\Delta\omega_i k + \varphi_i)), \quad (8)$$

$$p(k) = \begin{cases} 1, & \text{mod}[k, (T_s + T_p)/\Delta] < T_s/\Delta \\ 0, & \text{mod}[k, (T_s + T_p)/\Delta] \geq T_s/\Delta \end{cases} \quad (9)$$

and $a(k/(T_i/\Delta)) \in \{\pm 1\}$, T_i is the interference bit duration, $m(k)$ is PN sequence $\{\pm 1\}$, $\Delta\omega_i = \omega_i - \omega_c$.

Within the DSP block for interference rejection, reconfiguration, and detection, the interference is suppressed by ξ -structure [2].

The estimated value of the input signal, after the reconfiguration circuit, is:

$$\hat{d}(k) = \begin{cases} D_1(k)D_1(k-Q), & R(k) = 1 \\ D_0(k)D_0(k-Q), & R(k) = 0 \end{cases} \quad (10)$$

where:

$$\begin{aligned} D_0(k) &= X(k) \cdot m(k-L) \\ D_1(k) &= Y(k) \cdot m(k-L) \end{aligned} \quad (11)$$

$$Y(k) = \frac{1}{2L} \sum_{l=-L}^L Y_l(k) \quad (12)$$

$$Y_l(k) = \min_{WS_l(k) \in \{1, -1, j, -j\}} \{ |X(k) - WS_l(k) \cdot X(k-l) \cdot W_l(k)|^2 \} \quad (13)$$

$l = -L, \dots, -2, -1, 1, 2, \dots, L$; $2L$ is the ξ -structure length. $WS_l(k)$ is a variable that represents an estimated modulation content between $X(k)$ and $X(k-l)$.

Since it is known that the optimum (Wiener) values of each pair of filter coefficients, symmetrical with respect to the central point, are complex conjugate [2], it was shown that the balancing of left and right filter side weights slightly improves performances [3]. Also, in order to filter have gain equal to 1, its weights may be normalized. Therefore, filter weights are adjusted with

$$W_l(k+1) = \frac{\frac{1}{2}(W_{-l}^*(k+1) + W_l'(k+1))}{\frac{1}{2L} \sum_{\lambda=-L}^L |W_\lambda'(k+1)|} \quad (14)$$

where

$$\begin{aligned} W_l'(k+1) &= W_l'(k) + E(k)[X_l(k)WS_l(k)]^* \\ E(k) &= \mu \cdot Y(k) \end{aligned} \quad (15)$$

where $(\cdot)^*$ represents the complex conjugate.

In order to decrease the influence of noise on the reconfiguration decisions, a variable M is introduced. In the process of deciding on the change of configuration, besides the estimated SNR value at the considered bit interval, we also take into account the estimated SNR values from the previous $(M-1)$ bit intervals. SNR is the useful signal to noise ratio. The value of parameter $R(k)$ from (10) determines the moment of the reconfiguration, and it depends on the previous state:

- If $R(k-1) = 1$ then

$$R(k) = \begin{cases} 1, & \left[\begin{aligned} & \left[\hat{SNR}d_0(k) > \hat{SNR}d_1(k) \right] \wedge \\ & \left[\hat{SNR}d_0(k-1) > \hat{SNR}d_1(k-1) \right] \wedge \\ & \vdots \\ & \left[\hat{SNR}d_0(k-(M-1)) > \hat{SNR}d_1(k-(M-1)) \right] \end{aligned} \right] \\ 0, & \text{else} \end{cases} \quad (16)$$

It means that the system changes its state ($R(k) = 0$) if all of the latest M estimated SNR s in branch 0 (without interference rejection), $\hat{SNR}d_0$, are higher than the matching estimated SNR s in branch 1 (with ξ -structure), $\hat{SNR}d_1$.

- If $R(k-1) = 0$ then

$$R(k) = \begin{cases} 1, & \begin{cases} \left[\hat{SNR}d_1(k) > \hat{SNR}d_0(k) \right] \wedge \\ \left[\hat{SNR}d_1(k-1) > \hat{SNR}d_0(k-1) \right] \wedge \\ \vdots \\ \left[\hat{SNR}d_1(k-(M-1)) > \hat{SNR}d_0(k-(M-1)) \right] \end{cases} \\ 0, & \text{else} \end{cases} \quad (17)$$

Equation (17) means that the system goes to the ξ -structure interference rejection state ($R(k) = 1$) if all of the latest M $\hat{SNR}d_1$ s are higher than matching $\hat{SNR}d_0$ s.

Here the estimated SNR is

$$\hat{SNR}d_1(k) = \frac{\left[\frac{1}{Q} \sum_{l=k-Q}^k D_1(l) \right]^2}{\left[\frac{1}{Q} \sum_{l=k-Q}^k D_1^2(l) - \left[\frac{1}{Q} \sum_{l=k-Q}^k D_1(l) \right]^2 \right)}, \quad (18)$$

$$\hat{SNR}d_0(k) = \frac{\left[\frac{1}{Q} \sum_{l=k-Q}^k D_0(l) \right]^2}{\left[\frac{1}{Q} \sum_{l=k-Q}^k D_0^2(l) - \left[\frac{1}{Q} \sum_{l=k-Q}^k D_0(l) \right]^2 \right)}. \quad (19)$$

3. Numerical Results

The results shown in this section are calculated using Monte-Carlo simulation. For all the following figures the processing gain of the system is chosen to be $Q = 100$.

The influence of packet QPSK interference on the reception of DSSS-DPSK signal is shown in Fig. 2. The figure shows the error probability as a function of signal to noise ratio in case of interference to signal ratio $J/S = 40$ dB. The parameter for the curves is the ratio of packet to pause duration of packet interference. A set of curves labeled with a represent the system performance when there is no interference rejection circuit; curves b stand for the case of ξ -structure interference rejection, and curves c show the performance of the system using the reconfigurable interference rejection circuit.

The considered SNR range may be divided into three subranges. The first subrange is from SNR_a to SNR_b , and here the performances of the reconfigurable receiver are close to the ones of the receiver without the interference rejection circuit and without interference (curve d). The second subrange is from SNR_b to SNR_c , and that is the area of importance where the best performance has the reconfiguration receiver, and it reduces the error probability for an order of magnitude compared to the ξ -structure interference rejection. The third subrange is for $SNR > SNR_c$, and that is the area of high useful signal powers. In this area,

the performances of the reconfigurable receiver converge to the performances of the ξ -structure receiver.

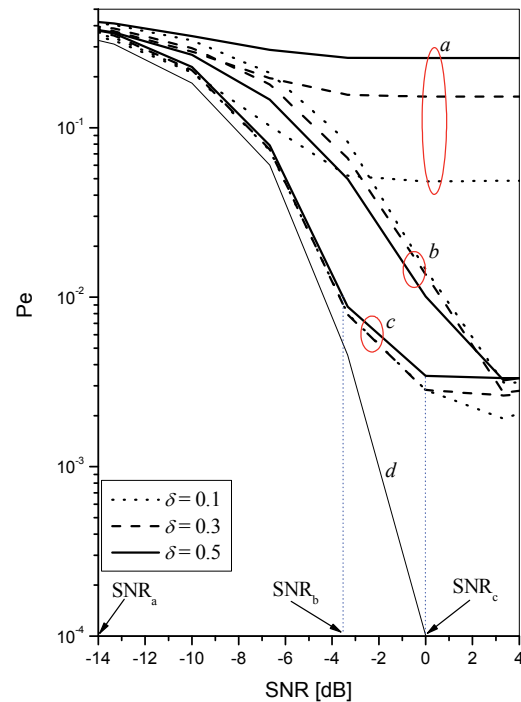


Fig. 2. Error probability as a function of signal to noise ratio.

The figure also shows that the system using the reconfigurable interference rejection circuit, as well as the system using ξ -structure for interference rejection have similar performances for any δ in range (0.1, 0.5). The influence of QPSK interference power, with parameter $\delta = 0.3$, on the performances of DSSS-DPSK signal reception is shown in Fig. 3.

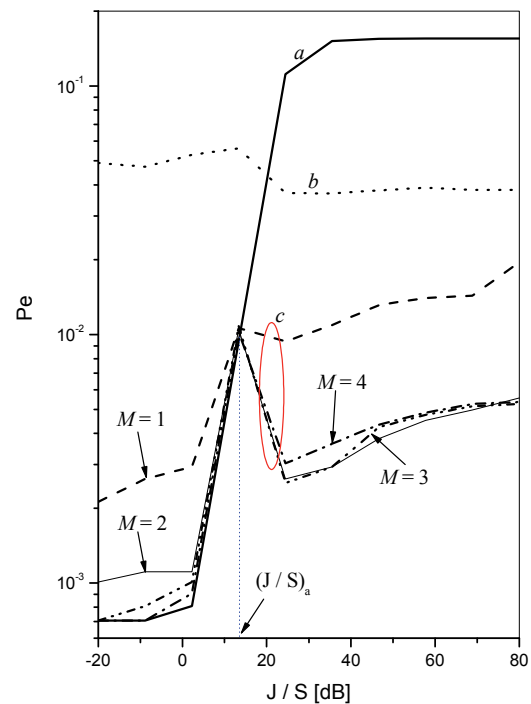


Fig. 3. Error probability as a function of interference to signal ratio in case of packet interference.

In Fig. 3, signal to noise ratio is $SNR = -2$ dB, and labels a , b , and c are have the same meaning as in Fig. 2. In the area $J/S < (J/S)_a$ the best performances has the receiver without the interference rejection circuit. By optimal choice of parameter M (in considered case $M = 3$), in the considered J/S range, the reconfiguration receiver performances can be made to be very close to the receiver without an interference rejection circuit. In the area $J/S > (J/S)_a$ the receiver with ξ -structure has weaker performances than the reconfiguration receiver with the optimized parameter M ($M = 3$).

Performances of the receiver in case of time continuous QPSK interference are shown in Fig. 4. Fig. 4 shows the error probability as a function of interference to signal power ratio for $SNR = -2$ dB. Performances of the reconfigurable receiver depend on the parameter M . In case of optimal value for parameter M (in considered case $M = 3$) for $J/S < (J/S)_a$ performances of the proposed receiver are very close to the receiver without an interference rejection circuit. For $J/S > (J/S)_a$ and in case of optimal value for parameter M , performances of the proposed receiver are very close to the receiver using only ξ -structure.

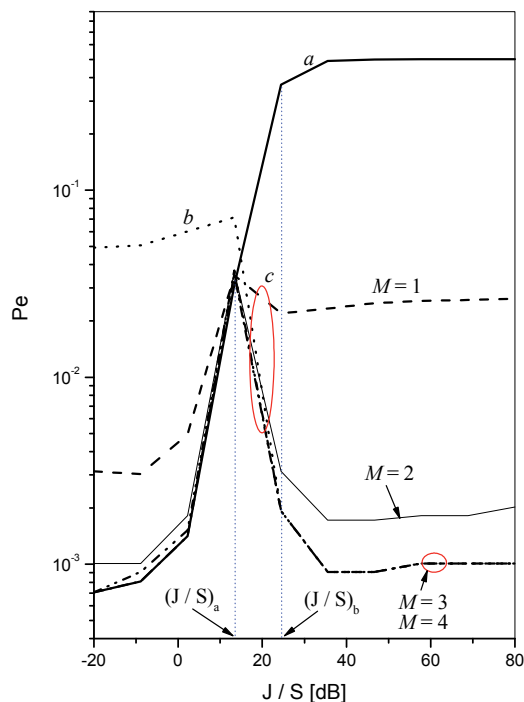


Fig. 4. Error probability as a function of interference to signal ratio in case of continuous interference.

4. Conclusion

A reconfigurable structure for the DSSS-DPSK system interference rejection is proposed in this paper. The system performance in the presence of QPSK interference is considered. The receivers without interference suppression circuit, with ξ -structure for interference suppression, and the receiver with the reconfiguration using ξ -structure

are compared on sense of error probability. Two cases of QPSK interference are considered: packet and continuous. In case of packet QPSK interference, for signal to noise ratios of practical importance, the use of interference rejection reconfiguration structure significantly lowers the error probability, compared to the receiver using ξ -structure for the interference suppression. The ξ -structure, which is developed for the continuous QPSK interference rejection [3], needs high interference to signal ratio for proper operation ($J/S > (J/S)_b$, (curve b in Fig. 4). The receiver without an interference rejection circuit cannot operate in the area of $J/S > (J/S)_b$. The proposed reconfigurable structure, with the optimal choice of parameter M , has equally good performances regardless of the interference power.

The shown results for the interference rejection using reconfigurable structure are very important for cognitive and software radio.

Acknowledgement

This work was financially supported in part by the Ministry of Science of Serbia within the Project "Development and realization of new generation software, hardware and services based on software radio for specific purpose applications" (TR-11030). The research is a part of the COST action IC0803 RFCSET.

References

- [1] NIKOLIĆ, Z., DIMITRIJEVIĆ, B., MILOŠEVIĆ N. Rejection of PSK interference in DS-SS/QPSK system using complex adaptive filter and nonlinear correlation receiver. *Electronics Letters*, 1997, vol. 33, no. 4, p. 268-270.
- [2] HASAN, M. A., LEE, J. C., BHARGAVA, V. K. A narrowband interference canceller with adjustable centre weight. *IEEE Trans. on Communications*, 1994, vol. 42, no. 2/3/4, p. 877-880.
- [3] GLIŠIĆ, S., NIKOLIĆ, Z., DIMITRIJEVIĆ, B. Adaptive self reconfigurable interference suppression schemes for CDMA wireless networks. *IEEE Transactions on Communications*, 1999, vol. 47, no. 4, p. 598-607.
- [4] CHEN, K. C., PRASAD, R. *Cognitive Radio Networks*, London: John Wiley & Sons, 2009.
- [5] HIGUCHI, K., FUJIWARA, A., SAWAHASHI, M. Multipath interference canceller for high-speed packet transmission with adaptive modulation and coding scheme in W-CDMA forward link. *IEEE Journal on Selected Areas in Communications*, 2002, vol. 20, no. 2, p. 419-432.

About Authors ...

Nenad MILOŠEVIĆ was born in Knjaževac, Serbia, in 1973. He received the B.E.E., M.Sc., and Ph.D. degrees at the University of Niš in 1997, 2000, and 2007, respec-

tively. His interests include mobile and wireless communications with special emphasis on cooperative communications.

Zorica NIKOLIĆ was born in 1955 in Niš. She received the B.E.E., M.Sc., and Ph.D. degrees at the University of Niš in 1979, 1985, and 1989, respectively. She is now a Professor at the Faculty of Electronic Engineering, University of Niš, where she teaches basics of telecommunications, telecommunication networks, mobile communications, spread spectrum systems, and wireless communications. Her main fields of interest include mobile and wireless communications.

Bojan DIMITRIJEVIĆ was born in Leskovac, Serbia, in 1972. He received the B.E.E., M.Sc., and Ph.D. degrees at the University of Niš in 1998, 2002, and 2006, respectively. His research interests include interference suppression in mobile and wireless communications.

Bojana NIKOLIĆ was born in Niš, Serbia in 1982. In 2007 she graduated from the Faculty of Electronic Engineering in Niš, major Telecommunications and enrolled Ph.D. studies on same faculty. She is a coauthor of several papers, presented at national and international conferences. Currently, Ms. Nikolić is a Teaching Assistant at the Faculty of Electronic Engineering in Niš.