

# Activation Energy of RTS Noise

Jan PAVELKA<sup>1</sup>, Josef ŠIKULA<sup>1</sup>, Munecazu TACANO<sup>2</sup>, Masato TOITA<sup>3</sup>

<sup>1</sup> Dept. of Physics, FEEC, Brno University of Technology, Technická 8, 616 00 Brno, Czech Republic

<sup>2</sup> AMRC, Meisei University, 2-1-1 Hodokubo, Hino, Tokyo, 191-8506 Japan

<sup>3</sup> Asahi Kasei Electronics, 5-4960 Nakagawara, Nobeoka, Miyazaki, 882-0031 Japan

pavelka@feec.vutbr.cz, sikula@feec.vutbr.cz, tacano@amrc.meisei-u.ac.jp, toita.mb@om.asahi-kasei.co.jp

**Abstract.** Low frequency noise was measured in silicon MOSFET and GaN and InGaAs based HFET devices with special emphasis on the RTS noise. The RTS (Random Telegraph Signal) dependence on the biasing conditions and temperature was analyzed in order to obtain new information regarding production technology. From the time dependence of the RTS noise voltage the mean time of charge carriers capture and emission by traps in the gate oxide layer was determined as a function of applied gate and drain voltage or electron concentration and then several important trap parameters, such as activation energy and position in the channel could be estimated.

## Keywords

RTS noise, 1/f noise, trap, MOSFET, HFET.

## 1. Introduction

In small area devices such as submicron MOSFETs with low number of active charge carriers in channel, a two level fluctuation of drain current may be observed, known as random telegraph signal (RTS) noise. An example of RTS noise measured on 0.35 $\mu$ m n-MOSFET is given in Fig. 1, where low and high current intervals are attributed to drain current modulation by electron capture and emission by single trap in the oxide near the Si-SiO<sub>2</sub> interface. Similar characteristics we observed on the GaN/AlGaAs [1] or InGaAs/AlGaAs [2] HFET devices (Fig. 2).

Electronic noise has been one of the most serious issues regarding analog devices and as device dimensions continue to shrink, RTS will become a prominent issue also in digital logic circuits, especially in flash memory due to threshold voltage fluctuation [3]. Low frequency noise is an important factor in determining the minimum voltage of an input signal and 1/f noise is a key concern even in RF applications such as mixers and voltage-controlled oscillators due to noise up-conversion.

According to the McWhorter theory [4], 1/f noise is generated by superposition of numerous events of RTS and in our previous papers we demonstrated the transition between these two types of current fluctuation in MOSFET channel from 15  $\mu$ m to 0.14  $\mu$ m length [5], [6].

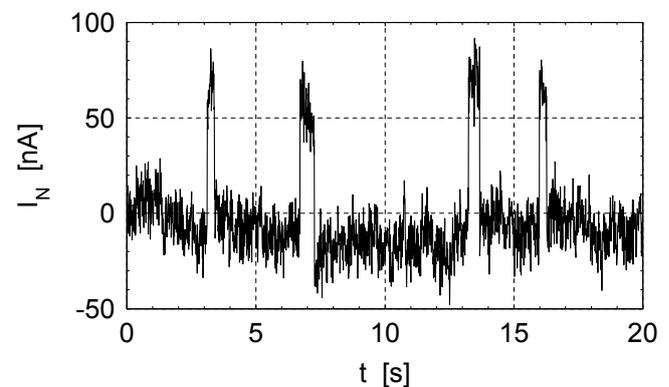


Fig. 2. Time dependence of RTS noise signal measured on GaN HFET with drain current  $I_D = 5.8 \mu\text{A}$ .

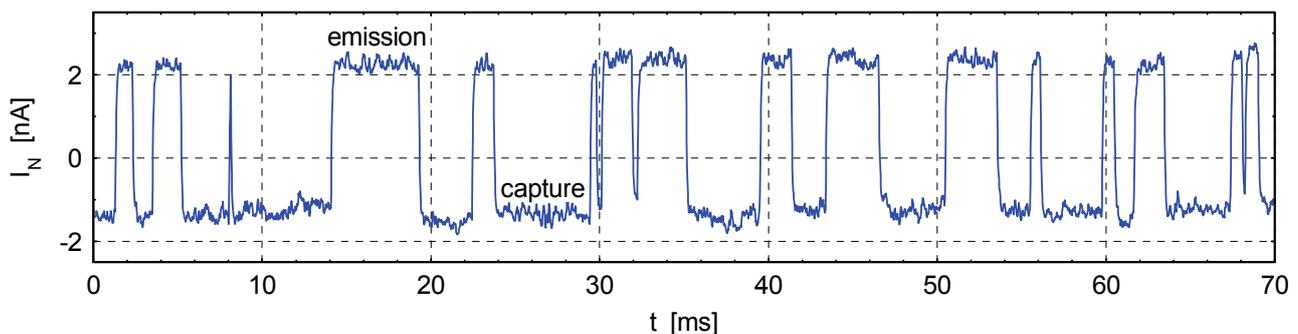


Fig. 1. Time dependence of RTS noise signal measured on 0.35 $\mu$ m MOSFET with drain current  $I_D = 1.75 \mu\text{A}$ .

## 2. Experimental Results

In the following sections, temperature dependence of transport and noise characteristics of various MOSFET and HFET devices is examined and activation energy of drain current and RTS noise time constants is discussed.

### 2.1 VA Characteristics and Activation Energy of Drain Current

Transport characteristics of enhancement mode n-MOSFET devices with LOCOS insulation and LDD channel with  $L = 0.35 \mu\text{m}$  length were measured in wide temperature range using HP4140B semiconductor parameter analyzer and helium cryostat [7]. Drain current  $I_D$  was examined as a function of both drain voltage  $U_D$  and gate voltage  $U_G$  for several operational regimes and results are given in Fig. 3 and 4. In sub-threshold region drain current is an exponential function of applied gate voltage for constant drain voltage:

$$I_D = I_{0G} \exp\left(\frac{eU_G}{nkT}\right) \quad (1)$$

where parameter  $n \cong 1.4$  is related to the ratio of oxide and depleted layer capacitance and interface trap concentration [8]. Analogous quantity subthreshold swing  $S = \partial U_G / \partial \log(I_D)$  with experimental value  $S = 87 \text{ mV/dec}$  corresponds to the substrate dopant concentration of the order of  $10^{17} \text{ cm}^{-3}$ .

For constant gate voltage drain current as a function of source to drain voltage can be expressed as

$$I_D = I_0 * \left[ 1 - \exp\left(-\frac{eU_D}{kT}\right) \right] \quad (2)$$

where pre-exponential parameter  $I_0$  dependence on temperature is described by activation energy  $\Delta E$  according to the Arrhenius equation

$$I_0 = I_C \exp\left(-\frac{\Delta E}{kT}\right). \quad (3)$$

Since drain current changes by several orders for temperature between 200 K and 300 K, normalized VA characteristics of  $I_D/I_0$  measured for several temperatures are given in Fig. 3 and perfect match between experimental dependence and theoretical fit according to equation (2) is obtained in the linear mode for  $U_D < 0.1 \text{ V}$  and  $U_G = 0.5 \text{ V}$ . For higher values of drain voltage up to 1.2 V perfect fit is also possible, when ohmic component  $cU_D$  is superposed.

The pre-exponential factor  $I_0$  given by equation (2) is closely related to the average charge carrier concentration in channel, defined by gate voltage and its activation energy corresponds to the difference of Fermi level and conduction band edge. In Fig. 4 Arrhenius plot of several  $I_0$  values obtained by fitting procedure demonstrated in Fig. 2 is given and resulting dependence of activation energy  $\Delta E$  on gate voltage closely follows theoretical rule  $\Delta E = E_0 - mU_G$  [8] where  $m = 1/n$  and ideality factor  $n \cong 1.4$  (1).

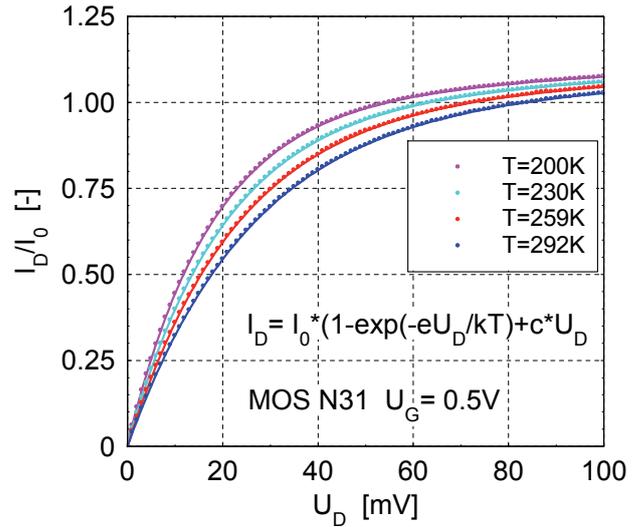


Fig. 3. Normalized drain current VA characteristics measured at several temperatures  $T$  (dots) and theoretical fit.

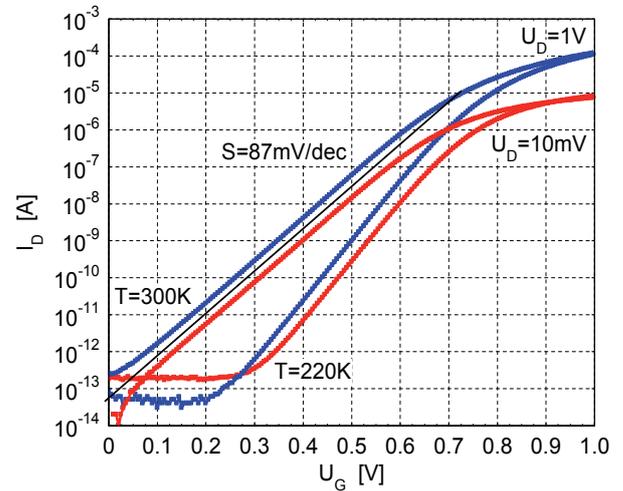


Fig. 4. Drain current  $I_D$  as a function of gate voltage  $U_G$  for constant drain voltage  $U_D = 10 \text{ mV}$  or  $1 \text{ V}$ .

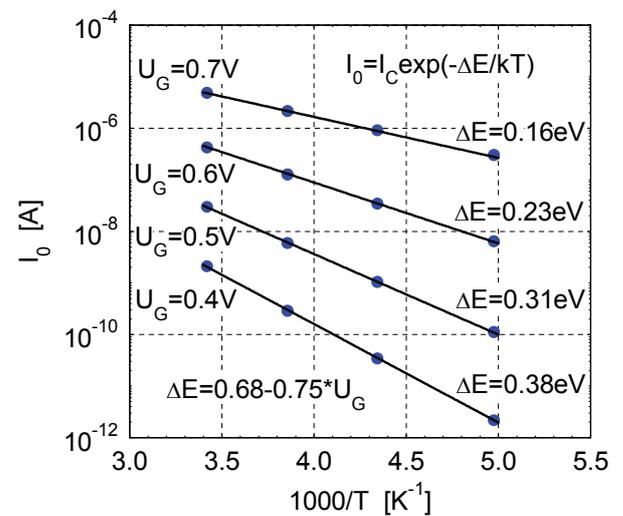


Fig. 5. Temperature dependence of drain current pre-exponential factor  $I_0$  for several values of gate voltage.

### 2.2 RTS Noise and Trap Activation Energy

Activation energy of traps (defects) in semiconductor devices is a very important technological parameter and its value can be determined from the temperature dependence of noise in two ways – either by analysis of noise characteristics in frequency domain, or in time domain.

Charge carrier capture and emission by single trap is a Poisson stochastic process with exponential distribution of RTS switching events duration [9], as is shown in Fig. 6, where histogram of 15 million consecutive pulses measured on Si MOSFET is given and average times in both states evaluated. The probability (per unit time) of a transition between high and low current states, or capture coefficient  $c$  is given by  $1/\tau_C$  and opposite transition (emission) by  $1/\tau_E$ .

In the frequency domain corresponding RTS noise voltage spectral density  $S_U$  frequency dependence is given by Lorentzian-type curve with characteristic time constant  $\tau$  defined by combination of both parameters  $1/\tau = 1/\tau_C + 1/\tau_E$ , as is shown in Fig. 7.

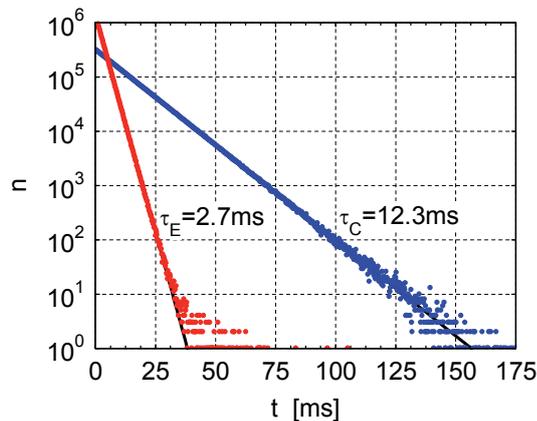


Fig. 6. Histogram of electron capture and emission events duration with mean times indicated (MOSFET N31,  $U_G = 0.68$  V,  $T = 234$  K).

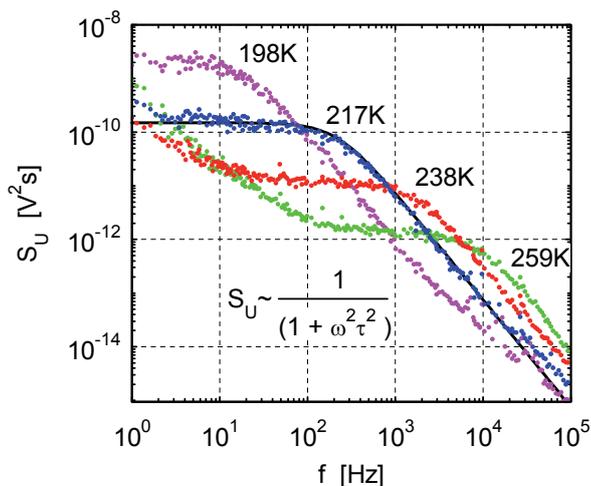


Fig. 7. Voltage noise spectral density frequency dependence measured for several temperatures on Si MOSFET N32, given by superposition of Lorentzian spectrum of RTS noise of dominant trap and background noise.

In order to determine thermal activation energy of involved traps, time dependence of RTS noise similar to signal in Fig. 1. was analyzed in several devices and mean capture and emission time parameters evaluated as a function of temperature for constant gate and drain voltage, as is shown in Arrhenius plot in Fig. 8.

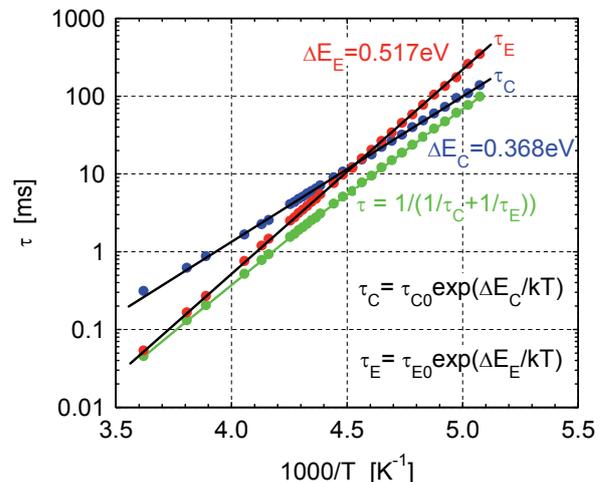


Fig. 8. Temperature dependence of mean capture  $\tau_C$  and emission  $\tau_E$  times (MOSFET N31,  $U_G = 0.7$  V).

In many cases low frequency noise is given as a superposition of several noise sources and then for multiple traps complex multilevel RTS is observed or strong  $1/f$  noise component renders it impossible to determine capture and emission time parameters directly from the time trace of noise voltage. Then frequency domain analysis can be used to estimate at least g-r noise time constant  $\tau = 1/(2\pi f)$ , as is shown in Fig. 7 for temperature  $T = 217$  K. Alternative method, which is more viable for less pronounced Lorentzian bulges and higher background noise, instead of finding  $\tau$  for given  $T$  plots noise amplitude at selected frequency as a function of temperature and finds  $T_{max}$  for given  $\tau$  (Fig. 9).

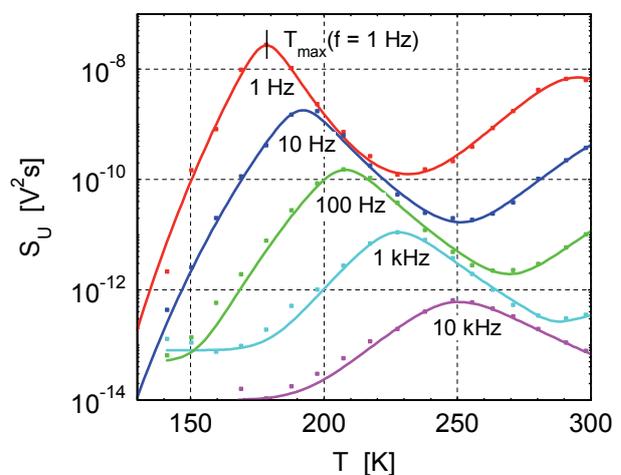


Fig. 9. Temperature dependence of voltage noise spectral density at five fixed frequencies - experimental data measured on sample N32 (dots) and theoretical fit.

Using this method, noise characteristics of GaN and InGaAs/InAlAs HFETs were also evaluated and activation energy  $\Delta E$  of corresponding traps calculated (see Fig. 12). Device parameters are given in [2] and [11]. Unlike Si MOSFET samples, due to the larger GaN active area size of about  $L = 2 \mu\text{m}$  only relatively small bumps of g-r noise are visible on the background  $1/f$  noise spectra and then quantity  $S_{U,f}$  is plotted in Fig. 10 to show the shift of corner frequency with increasing temperature. Similarly for the InGaAs HFET about one order change of the noise spectral density due to the influence of traps generated noise is displayed in Fig. 11, whereas much higher change is characteristic for submicron MOSFETs (Fig. 7 and 9). It should be noted, that raw  $S_U$  data are presented without normalization to sample current and load resistance [6], [12], but even after necessary corrections is the effect of the device size quite pronounced.

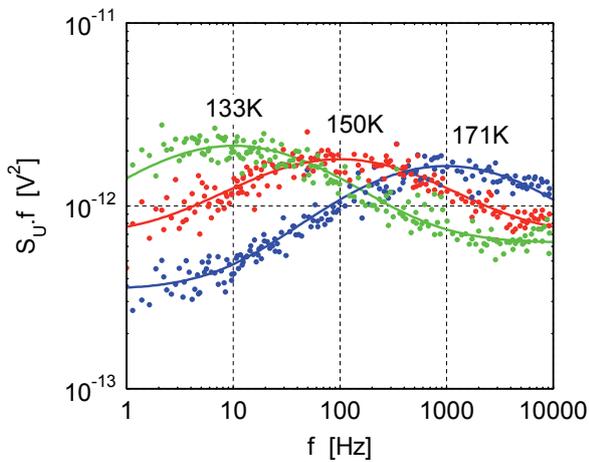


Fig. 10. Frequency dependence of voltage noise spectral density, measured at three temperatures on GaN/AlGaN heterostructure.

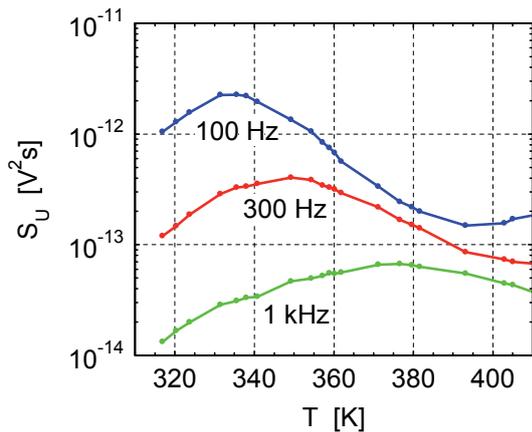


Fig. 11. Temperature dependence of voltage noise spectral density at three fixed frequencies – measured on InGaAs/InAlAs heterostructure.

Thermal activation energy of traps corresponding to the barrier height for electron tunneling from the Fermi energy level at the channel-oxide interface into the oxide trap is a parameter characteristic for each trap type and

then according to the values displayed in Fig. 12. traps could be identified [2], [11] and appropriate measures taken to the production technology, such as additional surface treatment before gate oxidation leading to  $1/f$  noise reduction due to lower interface trap density [13].

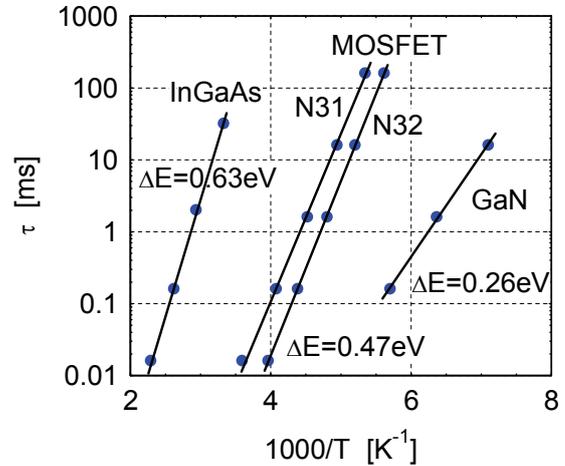


Fig. 12. Arrhenius plot of g-r noise time constant  $\tau$  for several semiconductor devices and corresponding activation energy  $\Delta E$  values.

However, there could be discrepancy between  $\Delta E$  values determined by various methods, such as DLTS and noise measurements and since  $\tau$  is a combined parameter of two components  $\tau_C$  and  $\tau_E$  with different properties, as is shown in Fig. 8, care must be taken when comparing experimental results. The most reliable data are obtained for symmetrical RTS characteristics, when  $\tau_C = \tau_E$  as is shown in Fig. 13. In this case for 50% trap occupation trap energy coincides with local Fermi level and the change of the  $\tau_C / \tau_E$  ratio with gate voltage, temperature and other parameters can be used to determine trap cross-section and position in channel.

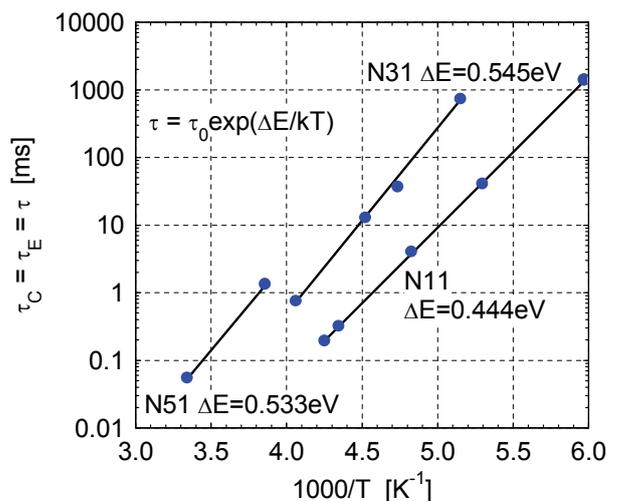


Fig. 13. Temperature dependence of mean capture and emission times for symmetrical RTS noise ( $\tau_C = \tau_E$ ), measured for constant drain voltage and variable gate voltage on three types of silicon MOSFETs.

Generally, charge carrier transitions between the oxide traps and the channel are governed by the Shockley-Read-Hall statistics [14] and capture time decreases with electron concentration  $n$

$$\tau_C = \frac{1}{c \cdot n} = \frac{1}{\sigma \cdot v_{th} \cdot n} \quad (4)$$

where  $\sigma$  is the trap cross section and  $v_{th}$  thermal velocity. Since electron concentration is a function of bias and temperature, capture times change as well and RTS noise could serve as a probe to estimate local concentration in the vicinity of active trap.

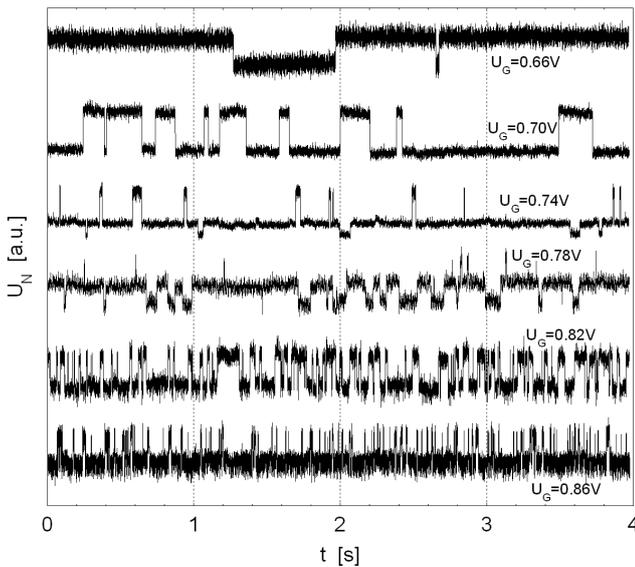


Fig. 14. Time dependence of RTS noise signal for increasing gate voltage  $U_G$ , normalized to the same amplitude.

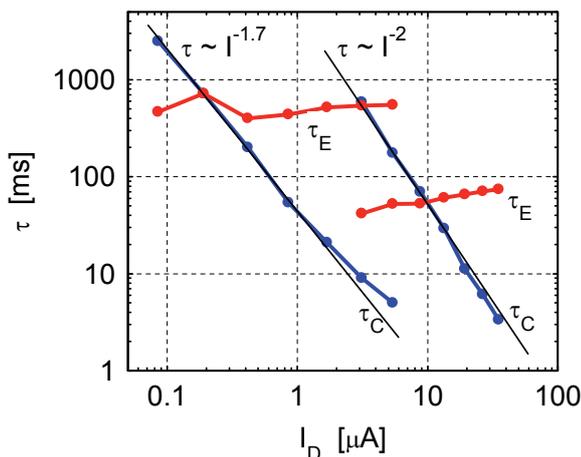


Fig. 15. Drain current dependence of capture and emission times of two traps, evaluated from signal in Fig. 14.

In Fig. 14 time dependence of RTS noise and in Fig. 15 corresponding values of mean capture and emission times are given as a function of drain current, driven by applied gate voltage according to (1). For a constant drain voltage drain current in the first approximation is proportional to the electron concentration in channel  $n$  and then we can

experimentally observe dependence of  $\tau$  on  $n$ . Whereas mean emission time  $\tau_E$  (release of trapped electron into the channel) is independent on  $n$ , capture time  $\tau_C$  decreases with increasing  $n$ , as is evident by shortening of high current intervals in Fig. 14. However, contrary to (4), about quadratic dependence was observed and then several more advanced models of capture kinetics were proposed, such as the Coulomb barrier [15] and two-step mechanism involving another interface trap [16], which we further elaborated into the GRT model [17].

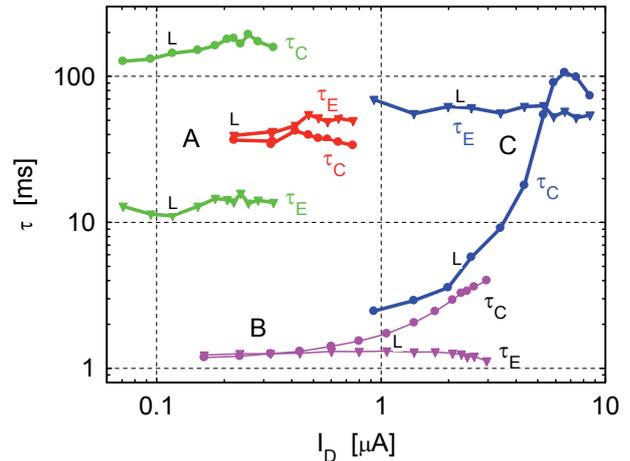


Fig. 16. Capture and emission time dependence on drain current. Measured for three traps A, B and C for constant gate voltage and variable drain voltage up to 1 V. L denotes the end of linear region ( $U_D = 20$  mV). Two curves for A trap due to small difference  $\Delta U_G = 0.04$  V,  $\Delta T = 10$  K.

Drain current modulation by particular trap is observed only when energy level of trapped charge is close enough (within several  $kT$ ) to the local Fermi level in the vicinity of active trap, as is documented in Fig. 14, where the shift from the first to the second trap activity occurs by the change of gate voltage of about 0.12 V, corresponding to about 1.5 orders difference in current/concentration. Similar mechanism applies also for drain voltage induced change of concentration. As we discussed in [12], there is a non-uniform distribution of free charge carriers in channel and in general their concentration decreases from source to drain electrode due to the diffusion current component. Then the position of trap can be estimated depending on the  $\tau_C/\tau_E$  ratio change with  $U_D$ , as is shown in Fig. 16. For the first type of characteristics, denoted as A group, there is no change of capture time with increasing current. We suppose that in this case active trap is located near the source and once the electron concentration is determined by the gate voltage and temperature, it doesn't depend on the drain voltage. Another trap for the C characteristic is probably located close to the drain electrode where channel pinch-off occurs on the transition from linear to saturation region and then strong dependence of  $\tau_C$  on the applied drain voltage and resulting electric field in channel is observed. Finally, the B characteristic corresponds to the intermediate region for trap located half-way between source and drain.

### 3. Conclusion

Temperature dependence of transport and noise characteristics of various silicon MOSFET and compound semiconductor HFET devices was measured and thermal activation energy of drain current and RTS noise capture and emission times evaluated in order to determine trap energy characteristic for particular production technology. A method for estimation of trap position in the channel from noise data is discussed as well.

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### References

- [1] TANUMA, N., TACANO, M., PAVELKA, J., HASHIGUCHI, S., ŠIKULA, J., MATSUI, T. Hooge noise parameter of epitaxial n-GaN on sapphire. *Solid State Electronics*, 2005, vol. 49, no. 6, p. 865 - 870.
- [2] PAVELKA, J., TACANO, M., TANUMA, N., ŠIKULA, J. 1/f noise models and low-frequency noise characteristics of InAlAs/InGaAs devices. *Physica Status Solidi C*, 2011, early view DOI 10.1002/pssc.201000516
- [3] KURATA, H., OTSUGA, K., KOTABE, A., et al. Random telegraph signal in flash memory: its impact on scaling of multilevel flash memory beyond the 90-nm node. *IEEE Journal of Solid-State Circuits*, 2007, vol. 42, no. 6, p. 1362 - 1369.
- [4] McWHORTER, A. L. 1/f noise and germanium surface properties. In *Semiconductor Surface Physics*. University of Philadelphia Press, 1957, p. 207 - 228.
- [5] PAVELKA, J., ŠIKULA, J., TACANO, M., TOITA, M. Scaling of RTS noise in MOSFETs. In *Proceedings IMAPS CS International Conference Electronic Devices and Systems*. Brno (Czech Republic), 2008, p. 126 - 131.
- [6] PAVELKA, J., ŠIKULA, J., TACANO, M., TOITA, M. Amplitude of RTS noise in MOSFETs. In *Proceedings IEEE 21<sup>st</sup> Int. Conference on Microelectronics ICM*. Marrakech (Morocco), 2009, p. 340 - 343.
- [7] ŠIKULA, J., PAVELKA, J., SEDLÁKOVÁ, V., TACANO, M., HASHIGUCHI, S., TOITA, M. RTS in submicron MOSFETs and quantum dots. In *Proceedings of 2<sup>nd</sup> SPIE Symposium Fluctuation and Noise*, SPIE vol. 5472. Maspalomas (Spain), 2004, p. 64 - 73.
- [8] SZE, S. M., NG, K. K. *Physics of Semiconductor Devices*. 3<sup>rd</sup> ed. Hoboken: J. Wiley, 2007.
- [9] KIRTON, M. J., UREN, M. J. Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/f) noise. *Advances in Physics*, 1989, vol. 38, no. 4, p. 367 - 468.
- [10] CELIK-BUTLER, Z., AMARASINGHE, N. V. Random telegraph signals in deep sub-micron metal-oxide-semiconductor field-effect transistors. In *Noise and Fluctuations Control in Electronic Devices*. American Scientific Publishers, 2002, p. 187 - 199.
- [11] PAVELKA, J., TANUMA, N., TACANO, M., ŠIKULA, J. Noise spectroscopy of AlGaIn/GaN HFETs on SiC and sapphire substrates. Submitted *Microelectronics Reliability*, 2011.
- [12] PAVELKA, J., ŠIKULA, J., CHVÁTAL, M., TACANO, M., TOITA, M. RTS noise amplitude and electron concentration in MOSFETs. In *Proceedings of the 27<sup>th</sup> International Conference on Microelectronics MIEL*. Niš, (Serbia), 2010, p. 475 - 478.
- [13] TOITA, M., AKABOSHI, T., IMAI, H. 1/f noise reduction in PMOSFETs by an additional preoxidation cleaning with an ammonia hydrogen peroxide mixture. *IEEE Electron Device Letters*, 2001, vol. 22, no. 11, p. 548 - 550.
- [14] LUNDSTROM, M. *Fundamentals of Carrier Transport*. 2<sup>nd</sup> ed. Cambridge: Cambridge University Press, 2000.
- [15] SCHULZ, M. Electrical characterisation of the SiO<sub>2</sub>-Si system. *Microelectronic Engineering*, 1998, vol. 40, p. 113 - 130.
- [16] FU, H. S., SAH, C. T. Theory and experiments on surface 1/f noise. *IEEE Transactions on Electron Devices*, 1972, vol. ED-19, no. 2, p. 273 - 285.
- [17] ŠIKULA, J., PAVELKA, J., TACANO, M., TOITA, M. GRT model of RTS noise in MOSFETs. In *Proceedings IEEE 21<sup>st</sup> Int. Conference on Microelectronics ICM*. Marrakech, (Morocco), 2009, p. 290 - 293.

### About Authors ...

**Jan PAVELKA** (1973) graduated in physics at Masaryk University, Brno and received the Ph.D. degrees in physics of condensed matter (2001) and microelectronic technology (2002) at the Brno University of Technology, where he currently works as Associate Professor. He spent three years as JSPS postdoctoral fellow at Meisei University, Tokyo. His research interests include noise in silicon and compound semiconductor devices.

**Josef ŠIKULA** (1933) graduated in electronics at the Czech Technical University, Prague and got Ph.D. degree in semiconductor physics from Masaryk University, Brno. During 1967-72 he was the head of the Physics Department at the Technical College of Cairo, Egypt and since 1980 Professor at the Brno University of Technology. His research work comprises fluctuation phenomena in materials and devices and non-destructive testing.

**Munecazu TACANO** (1940) received the Ph.D. degree in applied physics from the University of Tokyo. He was a Research Associate at the University of Washington in Seattle (1971-2), the Electrotechnical Laboratory of MITI, leading scientist of the Kyocera Central Research Laboratory during 1992-6 and since then Professor at the Dept. of Electrical Engineering, Meisei University, Tokyo. He investigates mainly wide band gap materials and devices for high speed communications.

**Masato TOITA** got Ph.D. degree in semiconductor engineering from Tohoku University, Sendai and worked in the Center for Integrated Systems, Stanford University until joining Asahi Kasei Microsystems as senior process engineer specialized in compound semiconductors devices.