

Development in Electronic Packaging – Moving to 3D System Configuration

Ivan SZENDIUCH

Dept. of Microelectronics, Brno University of Technology, Technická 10, 616 00 Brno, Czech Republic

szend@feec.vutbr.cz

Abstract. *The electronic industry is reducing package dimensions of components as well as complete electronics systems. Surface mount device passives and semiconductor chips have to be mounted together bringing a functional system that must realize the required function with necessary reliability and acceptable price. To make up a reliable and cost effective system, the size and weight is being reduced by employing lower voltages and higher speeds. For example, the typical size of SMD passives 30 years ago was 1206 when they were first introduced. Generally, all components including electrical joints are becoming miniaturized and smaller. The industry is moving toward a reduced size of 0201 and 01005 for passives, new fine pitch packages for actives, but the PCB now feature limits for further integration. System on Package (SOP) is one way to reach the three-dimensional package concept where components will be placed in three-dimensional configuration. A similar concepts are "Package on Package" (PoP) or "Package in Package" (PiP).*

Keywords

Electronic Packaging, Integration in Electronics, System on Package (SoP), Package on Package (PoP), 3D Package.

1. Introduction

The current development in electronic packaging tends to achievement of the higher integration by utilizing new materials, processes and configurations. That requires a new approach to electronic design and layout of semiconductor chips, circuits and systems. The roadmap of modern packaging, which became the path to system integration, is presented in this paper.

First, we need to define the term 'electronics packaging.' A simple and logical definition is based on the fact that packaging in electronics incorporates all technologies used between the IC (semiconductor chip) and the electronics system. The electronics packaging is also the bridge between ICs and electronic systems. The packaging design requires the most efficient solutions for interconnections, which means that ICs and components are assembled onto system level boards – requiring a base

substrate (PCB or ceramic) and assembly technologies such as surface mount technology (SMT), low temperature co fired ceramics (LTCC), high temperature co fired ceramics (HTCC), polymers etc.

Modern electronics requires miniaturized but more complex products (electronic devices). Moreover, the quality and cost must be balanced. Consequently, an increasing number of components, semiconductor chips and passives need to be placed inside the system. All kinds of problems must be solved – electrical (signal processing), physical (heat transfer and cooling), mechanical, chemical and also technological. The technology has to cope with implementation of small connections and interconnection to build high density circuits, and at the same time achieve a competitive cost. Electronic packaging represents a wide range of problems to be solved to achieve optimal system integration.

Basically two types of packaging concepts emerge:

- System on Chip (SoC)
- System on Package (SoP).

In SoP the value of 'package' becomes even more important because there are a countless number of solutions. The basis of this concept is simply that while CMOS is good / suitable for certain functions such as logic and memory, it is not good / suitable for functions such as filters, antennas, capacitors, resistors, power amplifiers, switches, baluns, optical waveguides, surface acoustic, bulk acoustic components, etc. [1]. Also usually As a rule, to resolve the problem of modern packaging to create a modern packaging system means to build a complete electronic system in the 3D configuration.

2. The Role of Advanced Packaging

The approach to electronic packaging has dramatically changed during last decades. In the past, semiconductor chip, integrated circuit (IC) design was completely separate from the package design. IC was designed first and then a suitable package selected for assembly. Packages created a standardized set defined with ISO registered outlines. Advanced IC and package development was mainly driven by military, aeronautics and space applications, and commercial design rules

followed these with reduced requirements. That means the package type had only a very small effect on design and performance of IC.

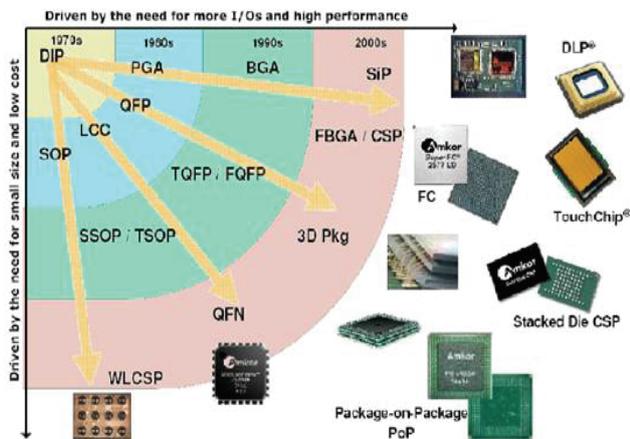


Fig. 1. Development of packages in the last decades (from [5]).

However, it can be observed that as early as in the 1980s the move from Dual in Line (DIL) packages to Leaded Chip Carrier (LCC) and other (PGA, QFP etc.) in some cases dramatically affected components, especially microprocessors, memories, etc. (Fig.1). This development is going on this time with series of new solutions.

With development of semiconductor chips, where Moore's law plays a significant role, chips become more complicated, which is featured by two major facts:

- An increased number of terminals (pads) in chips,
- terminals (pads) can have different shapes implemented by various techniques.

The present-day advanced packaging has to meet the following requirements [2]:

- Increased performance is required (need for a concrete application),
- package is designed specifically for an IC and application (proliferation of package styles),
- IC / Package co-design environment (some ICs now being designed could not be repackaged into a different format without complete re-design),
- now emerging the request for memories and others systems used for PoP stacking (communication sector applications and other),
- 3D interconnection method (higher frequency requirements related to new processors),
- low cost becomes primary consideration.

Looking at advanced package development it is obvious that electronic packaging is primarily driven by demand for overall system cost reduction. The result is that there is request for improved technology, but without an increase of the cost. Consequently, improved technology is required, but increased cost is not desirable. This situation

actually signals a lack of standard sizes and outlines because demands for package performance vary and the final solution results in compromise in parameters. That is why a new market is emerging in this sector – OSAT companies developing new packaging technologies (PacTech, Amkor, Tessera etc.) [6].

3. Why Standardized Packages Are Not Suitable

For a long time there were two types of packaging for semiconductor chips non-hermetic (plastic) and hermetic (metal and ceramic).

Plastic packages used to be very popular in commercial applications for their low cost and small size compared to ceramic and metal packages. The cost of plastic packages is roughly one half to one tenth the cost of comparable ceramic or metal packages. In a plastic package, the chip is encapsulated in a polymer, usually called encapsulant, which is an electrically insulating material that protects the chip including lead frame assembly from the adverse effects of handling and storage. At first the lead frame with a 2,5 mm pitch was commonly used, until in the late 1980s, the 1,27 mm pitch (surface mount technology) became prominent. As device complexity increased, the I/O count increased too. To keep electrical performance and package size reasonable, the lead pitch decreased, and fine-pitch leaded devices (lead pitch 0,65 mm and less) were introduced. Encapsulation techniques include molding, potting, glob-topping, and conformal coating, but the majority of encapsulated packages are molded.

Hermetic packages have been used foremost for military, space and medical applications because of their perceived reliability advantage over plastic packages. They have also been employed in some high power applications where heat must be dissipated from the device. Metal packages are typically used for small integrated circuits with low lead count and in applications that require electromagnetic shielding. Both metal and ceramic packages can be made nearly impervious to moisture when hermetically sealed. A package is classified as hermetic if it has a minimal leak rate (the rate at which gases can diffuse into or out of the package). Typical acceptable helium leak rates depend on the package size and helium pressure in the package.

Today there are many producers and many more users of semiconductor chips worldwide. Electronic circuits and systems are used in nearly all economic sectors including consumer electronics. Various types of chips in terms of function have different requirements for package or encapsulation. An alternative package is not an option to be used without assessing the affected parameters. High frequency ICs now require a package optimized for chip topology. For example, potting can be suitable for chip applications in the consumer sector, but in a medical application the same chip requires more reliable packaging, such as CSP (Chip Scale Package) [1] [10].

Looking at Fig. 1 it is obvious that there are many packages at disposal today, where the number of pins, size and cost are the fundamental factors for an optimal solution. Today’s packaging is not only one package but more compositions put in order for this purpose. A new approach to modern electronic system package construction is shown in Fig. 2. The prime reason is the decreased size of pads on first-level interconnection from (40–100) μm to (10–20) μm pitch, which gives many various solutions.

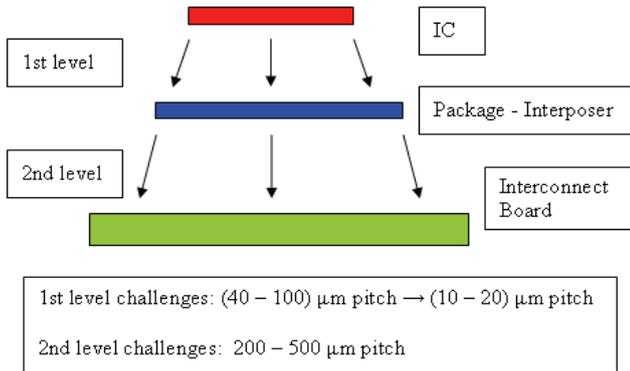


Fig. 2. Modern electronics system interconnection.

4. Wire Bonding vs. Flip Chip

Two main types are characteristic after the first level packaging interconnection performance for packaging finalizing in the dependence of chip connection:

- Wire bonded chips,
- bump bonded chips (flip chip).

Wire bonding interconnection is formed by metallurgical bonding a small-diameter wire, from the pad of semiconductor device to the lead frame or pad on substrate. The bonded wire creates a low resistance path for signal propagation. Typical materials are aluminum (ultrasonic), gold (thermocompression and thermosonic), and copper (thermosonic). Materials for pads on bondable surfaces include aluminum, gold, silver, nickel, and copper. Silver has been used as a bondable plating material on lead frames and as a bondable thick-film metallization in alloy with platinum or palladium. As mentioned above, there are three bonding techniques in microelectronics:

- Thermocompression (two metals are brought into pressure-tight contact through a controlled time approx. 40 ms, in a temperature range 300 - 400°C, and pressure cycle) producing through the capillary a ball bond (first) and a wedge bond (second).
- Ultrasonic (the source of energy is a transducer vibrating the bonding tool parallel to the bonding pad in a frequency range from 20 to 60 kHz) producing wedge-wedge bonds.
- Thermosonic (the capillary is not heated and substrate temperatures are maintained between 100 and 150°C) combines ultrasonic energy with the

ball-bonding capillary technique of thermocompression bonding.

In flip chip bonding (bump bonding) the chip is connected face down onto the substrate (Fig. 3). There are three main possibilities for attachment, solder bumps (reflow to matching footprints of pads on a substrate), solder less polymer adhesive (glued to footprints of pads on a substrate by conductive polymer) and thermosonic assembly process (gold to gold). Flip chip technology has several advantages over wire bonding:

- Self-alignment during die joining,
- low lead inductances, due to shorter interconnection lengths than in the case of wire bonding,
- reduced need to attach precious metals,
- increased productivity, due to the ability to make higher numbers of bonds simultaneously.

The flip chip assembly performance is a composite of multiple, thin layers of metals. On the die bond pads, the pad structure is called under-bump metallurgy (UBM). On the substrate bond pads, the connection structure is called top-surface metallurgy (TSM). The space between the chip and the substrate contains underfill, which interposes adhesive creating mechanical and thermal coupling to connect the chip to the substrate. Fig. 3 shows a typical flip chip bond structure.

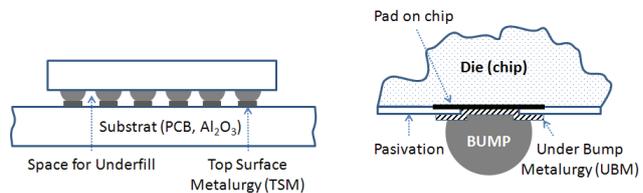


Fig. 3. Flip chip: a) general view, b) detail of solder bump.

The UBM structure and solder bump manufacturing can be implemented using a variety of materials and methods, including metal masking, photolithography, electroplating, ultrasonic soldering, mask-less bumping, copper bumping etc. The TSM structure is made of a metal that increases wettability and has a surface suitable for solder reflow and bonding. It means it is able to retain wetting properties and provide an adequate shelf life prior to die attachment. What is more, it can be created on different substrate materials. It is obvious that there is space for many various combinations of package solutions and the designer can select an optimal solution for each particular application.

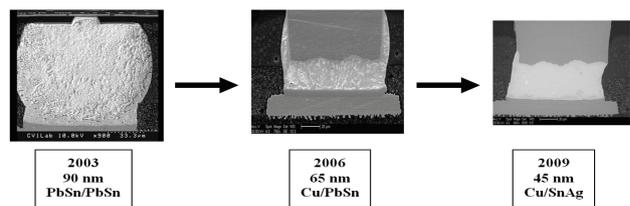


Fig. 4. Development in Flip-chip bump implementation.

Plating and evaporating are the major methods of bump formation. Evaporated bumps can be smaller and more uniform than plated bumps. The dimensions of bumps decrease as shown in Fig. 4 from approx. 125 μm diameter and 100 μm height in 2003 to 80 μm diameter and 25-80 μm height in 2009. That is one of the reasons for the current development in both, 1st and 2nd level packaging technologies.

5. New Packaging Trends

Three-dimensional (3-D) packaging including interconnection provides increased electrical performance and packaging density compared to two-dimensional (2-D) approaches which have been used for a long time. Three-dimensional packaging and interconnection can increase density by a factor of more than 50 by stacking integrated circuits (ICs). Schematically illustrated in time path, four generations of integration stages are shown in Fig. 5: single chip packaging, 2-D system packaging, 3-D system packaging and future polymer multi-functional solution.

Packaging development is accompanied by increasing component I/O densities, substrate or package technology is migrating to the high-density interconnection (HDI) and new materials and principles are utilized. Currently available are the following solutions for high-integration constructions:

- Die Stacking,
- 3D Design,
- IC and Package co-design,
- Embedding,
- Direct die/wafer wafer/wafer bonding,
- Optical Interconnect,
- System in Package (SiP),
- Package on Package (PoP),
- Plastic packages for high-power,
- Effects of Regulation / Legislation.

A characteristic feature of current packaging development is utilizing the third dimension (z axis) to build a complex 3D electronic circuit, block or system.

6. Three-Dimensional Packaging (3D)

Fig. 5 shows three stages of 3D packaging system development. The first stage, creating the system on package level, is composed of standard package techniques or chips based on combination of film technology with chips embedded in substrate. Conventional chips and packages are stacked in 3D configuration on basic substrate and encapsulated. The package to substrate interconnection is usually solder bumps or pad arrays. Next generation is

based on stacking of chips and wafers, where precise alignment is necessary as well as low temperature bonding. The fundamental operation is forming of vias in single wafers that are thinned to be used for interconnection of stacked wafers. A future generation configuration is the 3D structure built in Si epitaxial lateral growth based on low temperature crystallized Si. As evidenced by Fig. 6, there is a tendency to incorporate a significant part of the system in each single level.

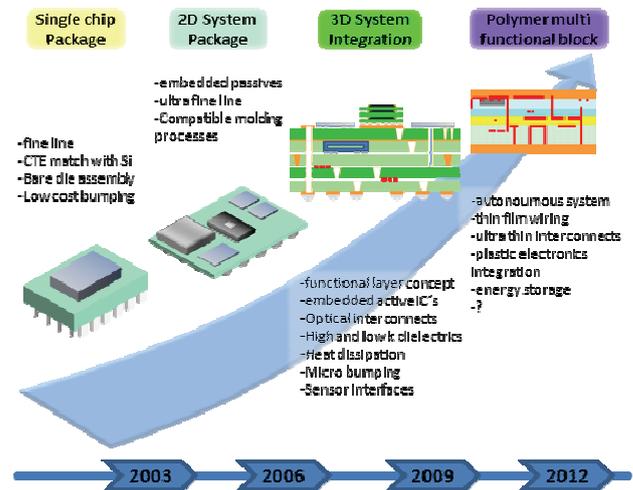


Fig. 5. Integration development of Electronic Packaging [5].

In 3-D packaging some new aspects in the behavior of components have to be predicted, especially in their interactions. Both single-level, horizontal cross-talk and cross-talk between stacked layers can be a problem, which may intensify in very high-speed applications. Furthermore, the approach may require use of heat spreaders in multiple high-power devices to achieve thermal operating specifications as well as thermal and thermo mechanical stress design limits.

The manufacturing process for 3-D microelectronic devices depends on the format chosen for the final product. Different technologies are used, from challenging semiconductor to the less expensive non-vacuum technology. The package elements of layered dies include the chips themselves, dielectrics between the die, and interconnects. The elements of dies stacked on edge, layered dies, and a vertically stacked module include dies, attachments between dies or components and interconnects between dies or modules.

System-on-Package (SOP) technology has the potential to provide modular design flexibility and high-performance integration of heterogeneous chip technologies and to support robust chip and component manufacturing with high-yield/low-cost chips for a wide range of product applications. The SOP concept has two fundamental drivers for miniaturization:

- Miniaturization of system components (to ultrathin – film embedded),
- reduction of three level hierarchy (package-board) to two level (system package).

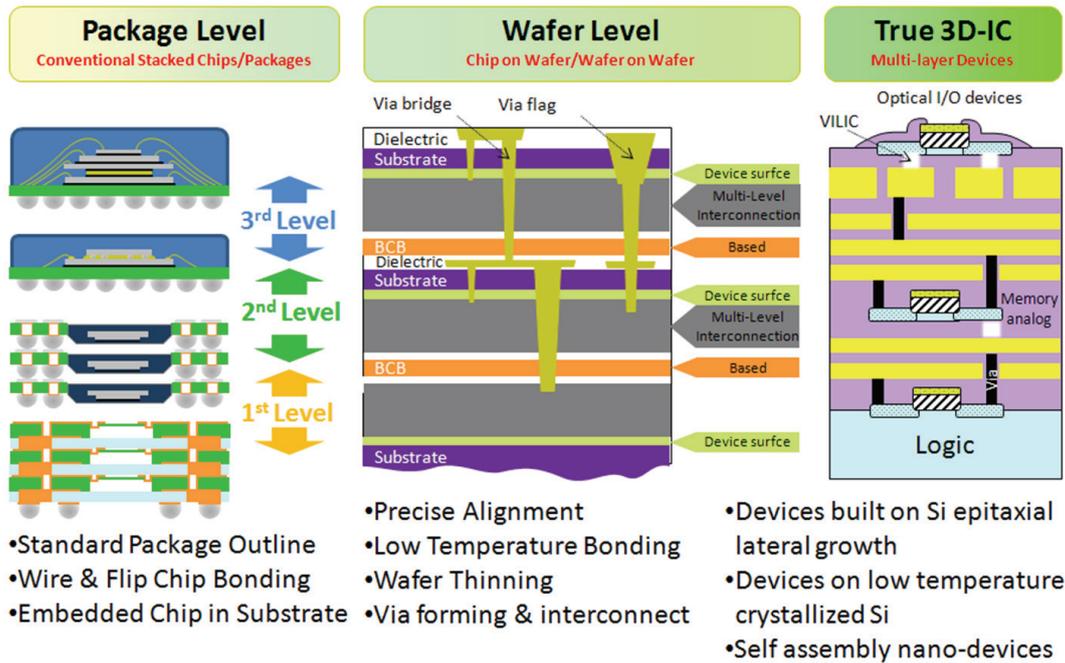


Fig. 6. Three stages of 3D package development [5].

Horizontal Structure (2/3D)		Wire Bonding Type	Flip Chip Type
Stacked Structure (3D)	Interposer Type	Wire Bonding Type	Wire Bonding + Flip Chip Type
	Interposer-less Type	Terminal Through Via Type	
Embedded Structure (3D)		Chip (WLP) Embedded + Chip on Surface Type	3D Chip Embedded Type
		WLP Embedded + Chip on Surface Type	

Fig. 7. Directions in concepts of SOP development and performance.

The key technology enables different parts as silicon dies, chip and embedded components, high-density interconnection including wiring, thick/thin film and assembly technologies to be incorporated (Fig. 7). It is obvious that SOP can be focused on various aspects arising from an application [3]. Two types are significant: the SOP that continues on 1st level packaging (includes Flip chip, WLP, SiP etc.) and a continuation of PCB technology - a non-vacuum assembly in 2nd level packaging. Only the 2nd level interconnect reliability is becoming a real concern where I/O count, package size and cost considerations lead to reductions in pitch and solder volume.

In the interposer-less structures and embedded systems the silicon through-vias are the key features

permitting efficient area array signal, power, and ground interconnection through these thinned silicon packages. A common characteristic of them all is high-density wiring and high-density chip I/O interconnection may be significant for tight integration of heterogeneous chip technologies. This approximates the performance of an integrated System-on-Package (SOP). In addition to heterogeneous integration, SOP may leverage integration of passive components, active devices and electro-optic structures to enhance system-level performance.

To make use of all the benefits of miniaturization and integration, such as increased performance, low cost, smaller footprint, power management, and time-to-market, the chip or single package must be created with regard to customers need. Now, electronic market demand is for convergent and integrated microsystem functions such as MPUs, graphics, memory (SRAM, Flash, DRAM), logic, SRAM, mixed signal, Radio Frequency (RF), sensors including MEMS, photonics and peripheral functions in one single package. Our work is focused on second-level, non-vacuum SOP construction, including interconnection of chips, modules, substrates and other components in one single package.

The first step to achieve a 3D construction by the non-vacuum process is based on various combinations of stacking, inorganic Al₂O₃ and organic flame resistant (FR-4) substrates. These substrate configurations, also called Package on Package (PoP), can be basically implemented in two ways. First, by solder bumps deposited by stencil printing and second, by bumps using a combination of solder balls and paste. This three dimensional configuration provides a good potential to make compact structures on the basis of thick film and polymer technology, especially

for non-conventional applications (sensors, antennas, components with distributed parameters etc.). Fig. 4 shows a flip chip bump (1st level packaging interconnection), Fig. 8 shows solder bumps formed on alumina substrate (2nd level interconnection).

By stacking of substrates, both organic and inorganic, it is possible to create various configurations of electronic systems as one single package [4]. A smaller size and higher reliability, in contrast to conventional PCBs, are the main advantages of this solution. The very high routing density, thin substrate and small form factor requirements, driving innovations in substrate design, materials (especially for higher frequency) and lithography improvements are challenges for future.

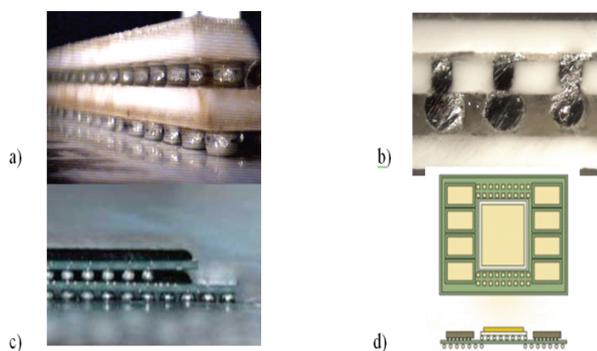


Fig. 8. 3D structure: a) alumina substrates and solder balls created using paste, b) edging through bump connection, c) combined by PCB and alumina, d) possible configuration.

7. Conclusion

The role of packaging is changing from traditional interconnections of discrete components to thick and thin film component integration. The System on Package (SoP) is a system concept with this package integration, in contrast to SiP, a modular concept. The SoP, a system-centric technology, is based on film components embedded in organic boards or packages, and together with SiP modules, SoC devices, battery and user interface, leads to multi-functional systems in the short term and mega-function systems in the end.

The future development of electronic packaging promises accelerating changes. The most recent finding is that cost is today the leading factor in nearly all applications and together with increased density of elements on chip it is the main reason for creating variability in package selection. The cost, a major driver in the advancement of technology generally, is also driving the trend toward electronics manufacturing specialized in packaging, working as contract manufacturers OSAT (Outsourcing Semiconductor Assembly Technology). The advantages of OSAT include optimizing manufacturing cycle times, reducing working capital, and improving quality. If the new

system integration technology cannot achieve cost parity with existing component technologies, then industry acceptance will be delayed.

Fig. 9 shows an electronic system production chain where many interactions and connections between chip performance and application area are evident.

Electronic packaging technology will continue during the 21st century to offer many new and compact products, above all for high-speed applications. The need for innovations in cost, yield and productivity will undoubtedly represent a challenge for engineers and researchers involved in packaging. The resulting new products will contribute to a better quality of life.

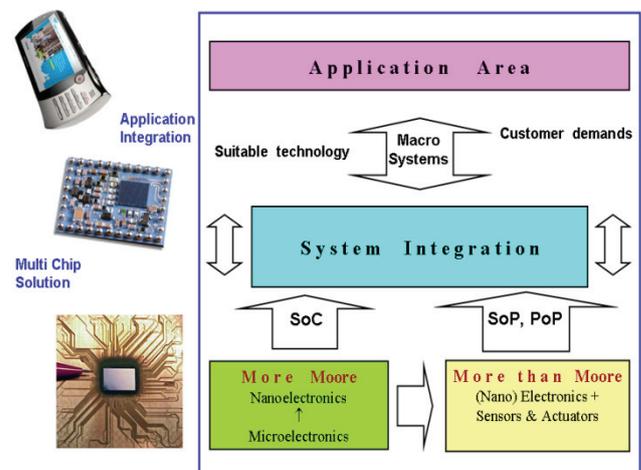


Fig. 9. Roadmap of system integration.

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About Author ...

Ivan SZENDIUCH was born in 1944 in Brno. He received his M.Sc. and PhD degrees in radioelectronics and microelectronics from Brno University of Technology in 1967 and 1987, respectively. He also completed a postgraduate study programme on semiconductor devices at the Czech Technical University in Prague in 1973. Since 1980 he has been with the Department of Microelectronics at the Faculty of Electrical Engineering and Communication, Brno University of Technology, where he became associate professor in 1990. His research interests include a wide area of microelectronics assembly and interconnection technology including thick and thin film circuits and their non-conventional applications, surface mount technology applications, soldering and packaging processes. He is an author of five books and more than 100 publications worldwide. Since 1990 member of ISHM/IMAPS Czech and Slovak chapter, where in the period 1996 - 2002 he was President and now he is honor member. In 2007 he received Fellow of the International Microelectronics and Packaging Society in San Jose, as the first Czech citizen.