# Basic Block of Pipelined ADC Design Requirements

*Vilem KLEDROWETZ, Jiri HAZE*

Dept. of Microelectronics, Brno University of Technology, Technicka 3058/10, 616 00 Brno, Czech Republic

kledrowetz@phd.feec.vutbr.cz, haze@feec.vutbr.cz

**Abstract.** *The paper describes design requirements of a basic stage (called MDAC - Multiplying Digital-to-Analog Converter) of a pipelined ADC. There exist error sources such as finite DC gain of opamp, capacitor mismatch, thermal noise, etc., arising when the switched capacitor (SC) technique and CMOS technology are used. These non-idealities are explained and their influences on overall parameters of a pipelined ADC are studied. The pipelined ADC including non-idealities was modeled in MATLAB - Simulink simulation environment.*

## Keywords

Pipelined ADC, MDAC, SC technique, MATLAB model, thermal noise, opamp.

## 1. Introduction

A pipelined ADC architecture offers good trade-off between conversion rate, resolution and power consumption. Fig. 1 shows a conventional pipelined ADC architecture. It consists of several cascaded stages (each resolve *n* – bit), timing circuits and digital correction block. The concurrent operation of all pipelined stages makes this architecture suitable to achieve very high conversion rates. The overall speed is determined by the speed of the single stage.

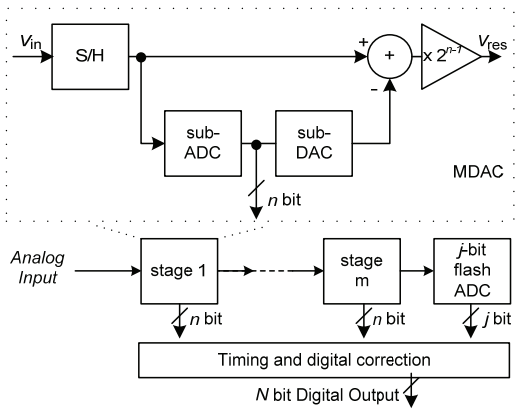


**Fig. 1.** Pipelined ADC architecture.

First, the input signal $v_{in}$ is captured by the sample and hold amplifier. Second, this signal is quantized by the sub-ADC, which produces a digital output (*n* – bit). This signal passes into the sub-DAC which converts it back to the analog signal. This analog signal is subtracted from the original sampled signal $v_{in}$. The residual signal goes into the opamp where it is amplified to the full scale range. The residue for 1.5-bit stage is expressed mathematically by

$$v_{res} = 2v_{in} - V_{ref} \text{ if } v_{in} > \frac{1}{4}V_{ref}, \quad (1)$$

$$v_{res} = 2v_{in} + V_{ref} \text{ if } v_{in} < -\frac{1}{4}V_{ref}, \quad (2)$$

$$v_{res} = 2v_{in} \text{ otherwise} \quad (3)$$

where $v_{in}$ is input signal of MDAC and $V_{ref}$ is voltage reference, which depends on the maximum input signal swing.

## 2. MDAC Design Requirements

MDAC consists of four parts - sample and hold stage, sub-ADC, sub-DAC and subtracting and amplifying stage. All these parts are sources of non-idealities. It is necessary to know important blocks, which have indispensable influence onto overall properties, to achieve good parameters such as resolution, power consumption and speed.

### 2.1 MDAC Resolution

It is a difficult optimization problem to determine the optimal number of bits resolved in each stage [1][2][3]. Typically a multi-bit first stage results in lower power consumption and matching and also amplifier gain requirements of the following stages. However the implementation of multi-bit stage possesses two major challenges. First, low feedback factor limits the maximum sampling frequency to low-to-mid rates. Secondly, and more importantly, multi-bit DAC requires several floating switches. These floating switches are a serious impediment to the design of low-voltage SC circuits. Due to this reason a conventional 1.5-bit stage was employed. The SC technique was utilized in the design of the MDAC to obviate the need for floating switches [4].

### 2.2 Thermal Noise

Thermal noise is caused by random movement of electrons in resistors. The thermal noise of resistor appears as white noise and its spectral power is

$$\overline{e_R^2} = 4kTR \cdot \Delta f \tag{4}$$

where $k$ is Boltzmann constant, $T$ is the temperature and $R$ is the resistor value.

All particles at temperatures above absolute zero are in random motion. Since electrons carry charge, the thermal motion of electrons results in a random current that increases with temperature. This noise current is in all circuits and corrupts any signals passing through. The sample and hold circuit is the most important source of noise in pipelined ADC. Two noise sources are significant in the sample and hold circuit: the sampling switches and the sample and hold amplifier. The sampling switch is used to sample the input signal onto a sampling capacitor. When the input signal is sampled, noise from the sampling switch is sampled by the sampling capacitor as well.

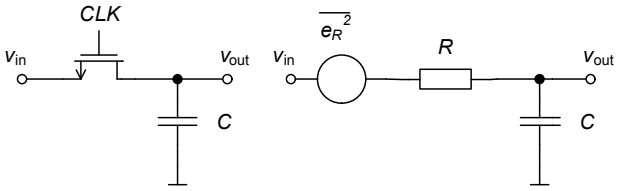


**Fig. 2.** Simple MOS sampling circuit and its equivalent circuit with on-resistance and thermal noise.

The thermal noise of switch is filtered by a single pole response low-pass filter created by the resistance of a switch and sampling capacitor. The transfer function of the low pass filter is

$$A(j\omega) = \frac{1}{1+j\omega RC}. \tag{5}$$

Total noise power can be obtained by integrating noise power spectral density over frequency and it is given by

$$\overline{e_{MOS}^2} = \frac{1}{2\pi}\int_0^\infty e_R^{-2} \cdot |A(j\omega)|^2 \cdot d\omega,$$
$$= \frac{1}{2\pi}\int_0^\infty \frac{4kTR}{1+(\omega RC)^2} \cdot d\omega, \tag{6}$$

$$\overline{e_{MOS}^2} = \frac{1}{2\pi} \cdot \frac{4kTR}{RC} \cdot arctan(\omega RC)\Big|_0^\infty = \frac{kT}{C} \tag{7}$$

where $C$ is the size of the sampling capacitor.

Source of thermal noise is commonly referred to as $kT/C$ noise because the noise power is proportional to $kT/C$. The sample and hold amplifier also contributes thermal noise degradation to the signal while being processed. The contribution of the sample and hold amplifier is also inversely proportional to capacitance. It is inversely proportional to the load capacitance in single stage amplifier. It is inversely proportional to the compensation capacitance in a Miller compensated amplifier. Thermal noise is perhaps the most fundamental source of error in pipelined ADC [11]. Since it is random error source from one sample to the next, it is not possible to correct this noise by calibration. Thermal noise can be alleviated by using large components (increases sampling capacitor size) or by oversampling. However, for a fixed input bandwidth specification, both of these remedies increase the power dissipation. Thus, a fundamental trade-off exists between thermal noise, speed and power dissipation. The impact of thermal noise on ADC is shown in Fig. 3.

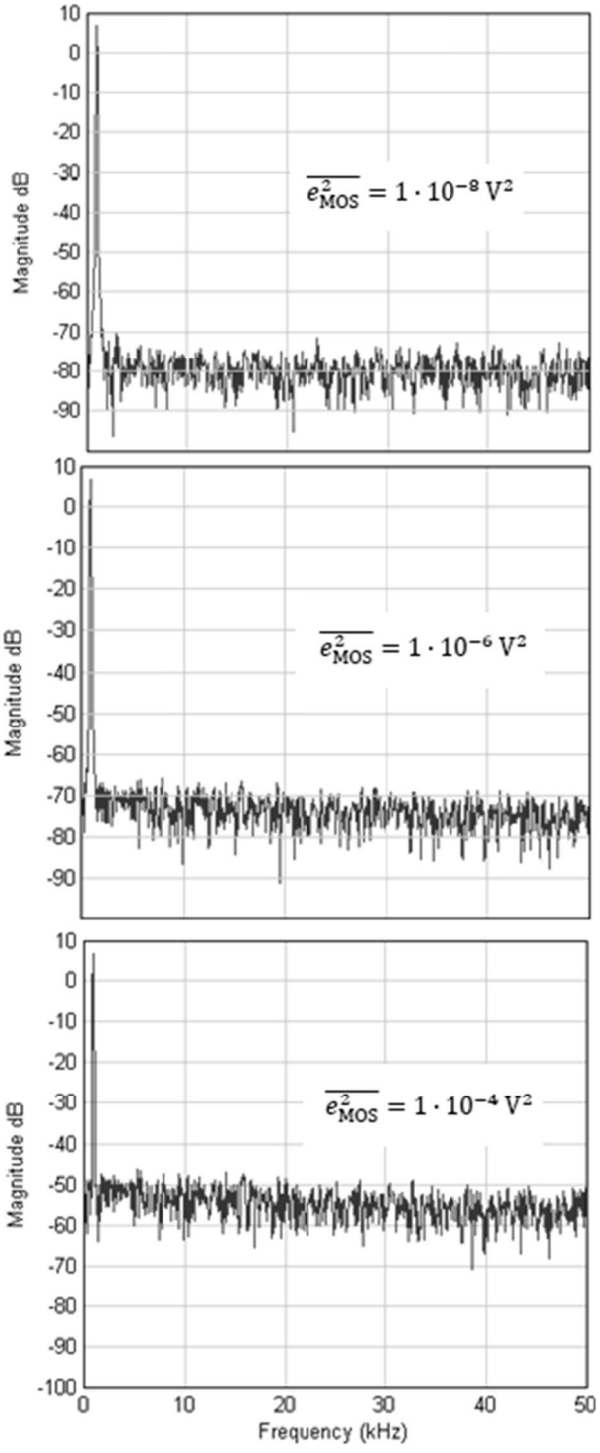


**Fig. 3.** Effect of thermal noise.

When the overall noise is in MDAC about $10^{-8}$ V$^2$, its influence is small (*ENOB* = 9,67 bits). A higher noise above approximately $10^{-6}$ V$^2$ is much more critical for *ENOB*. It is 9,1 bits for noise $10^{-6}$ V$^2$ and 5,8 bits for noise $10^{-4}$ V$^2$.

## 2.3 Comparator Offset

The offset voltage of comparators (Fig.4) is main source of errors in the sub-ADC of pipelined ADC [5].

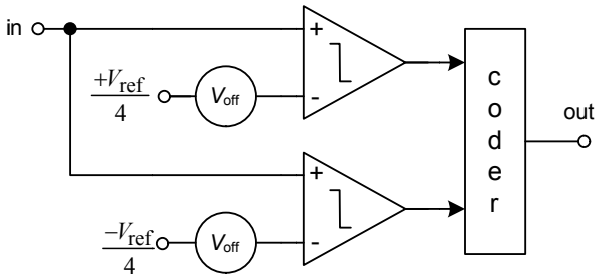


**Fig. 4.** Comparator offset in sub-ADC.

A comparator produces an output signal indicating whether or not an input signal is larger than a reference level. When the comparator computes the difference between two input signals, an internal offset voltage is added to this difference. Thus, when the two inputs are close together, the comparator may make an incorrect decision. When the comparator makes wrong decision, the output code is incorrect, and the incorrect reference is subtracted from the input. The result is residue that is out of range of the next stage of the pipeline when amplified.

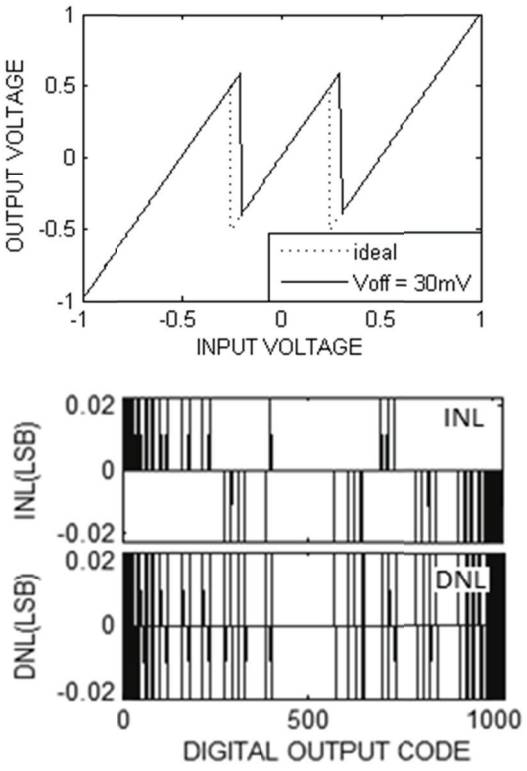


**Fig. 5.** The effect of comparator offset.

The effect of offset error in comparator on 1.5-bit stage transfer function is shown in Fig. 5. The dotted line represents ideal transfer function and the full line shows transfer function with offset voltage in comparator. The *INL* and *DNL* of the 10-bits pipelined ADC are small for comparator offset 30 mV (all comparators in ADC) thank to RSD (redundant signed digit) correction [2][4].

## 2.4 Opamp DC Gain Requirements

An opamp is one of the most important building blocks in analog circuits and also in switched capacitor implementation of pipelined ADCs [6]. Therefore, it is necessary to study the impact of the non-idealities of opamps on pipelined ADCs. Opamp contains input parasitic capacitance $C_P$. The open loop DC gain of the opamp is $A0$.

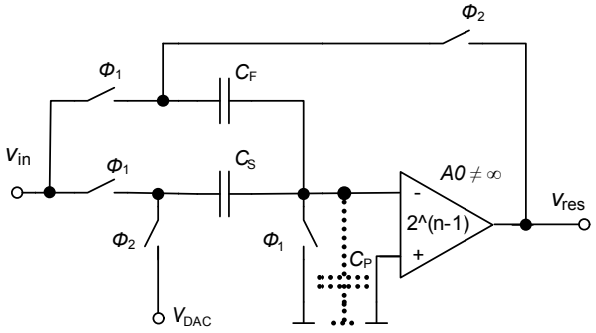


**Fig. 6.** Circuit diagram with opamp.

The sampling capacitor $C_S$ and the feedback capacitor $C_F$ are connected with input during the sampling phase and sampling an input signal on the capacitors. The total charge stored on capacitors $C_S$ and $C_F$ during sampling phase is

$$q_s = (0 - v_{in}).(C_F + C_S). \tag{8}$$

Feedback capacitor $C_F$ is connected with output of the opamp and sampling capacitor $C_S$ is connected with $\pm V_{DAC}$ or with ground (depending on the output of a sub-ADC) during the amplifying phase. The total charge stored during this clock phase is given by

$$q_a = (V^- - V_{DAC}).C_S + (V^- - v_{res}).C_F + V^-.C_P \tag{9}$$

where $V^-$ is negative input of the opamp and $V_{DAC}$ is output signal from the sub-DAC.

The total charge is conserved

$$q_s = q_a. \tag{10}$$

From the above equation

$$v_{res} = v_{in}.\left(\frac{C_S + C_F}{C_F}\right) + V^-.\left(\frac{C_S+C_F+C_P}{C_F}\right) - V_{DAC}.\frac{C_S}{C_F}. \tag{11}$$

The feedback factor $\beta$ depicts how much of the output voltage of opamp is fed back to opamp input and is given by

$$\beta = \left(\frac{C_F}{C_S+C_F+C_P}\right). \tag{12}$$

The DC gain requirement of opamp can be obtained from (11). Error portion due to finite opamp gain should be

smaller than 1/4 LSB of remaining resolution. The gain can be found from

$$\frac{1}{A.\beta} < \frac{1}{4}.LSB. \tag{13}$$

The effect of the finite DC gain error of opamp in 1.5-bit MDAC is shown in Fig. 7. It is transfer function of 1.5-bit stage. The dotted line represents ideal transfer function and the full line shows transfer function with finite DC gain error. The *INL*, *DNL* for *A*0 = 20 dB are shown at the right side.

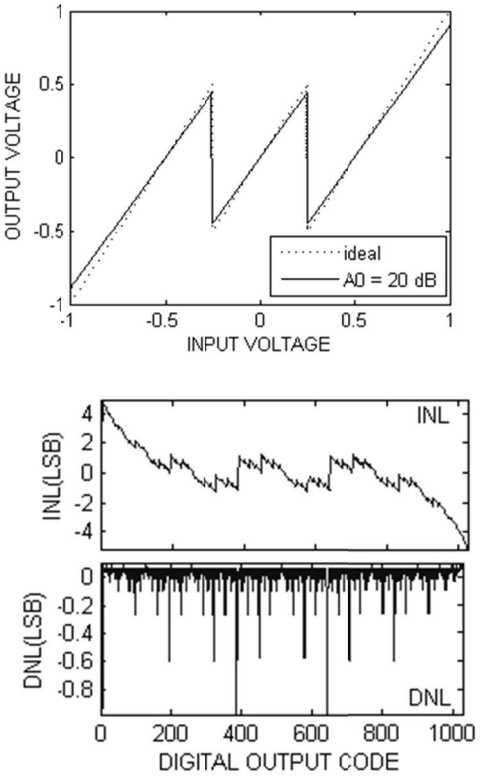


**Fig. 7.** The effect of finite DC gain of opamp.

## 2.5 Opamp Bandwidth Requirements

The DC gain requirements of opamp were defined in Section 2.4. In order to have opamp which is sufficiently settled within a given timeframe the opamp must have enough bandwidth. However opamp which has a large bandwidth requires high power consumption - thus to minimize power it is critical to optimize opamp bandwidth [11].

Referring the settling error of the first pipeline stage to the input of the ADC and noting that the total error must be less the quantization noise (i.e. < $2^{-N}$) the required unity gain frequency of the opamp $f_{GBW}$ to achieve *N*-bit settling is thus given by

$$f_{GBW} = \frac{(N-n)log2}{\beta\pi} \cdot f_s \tag{14}$$

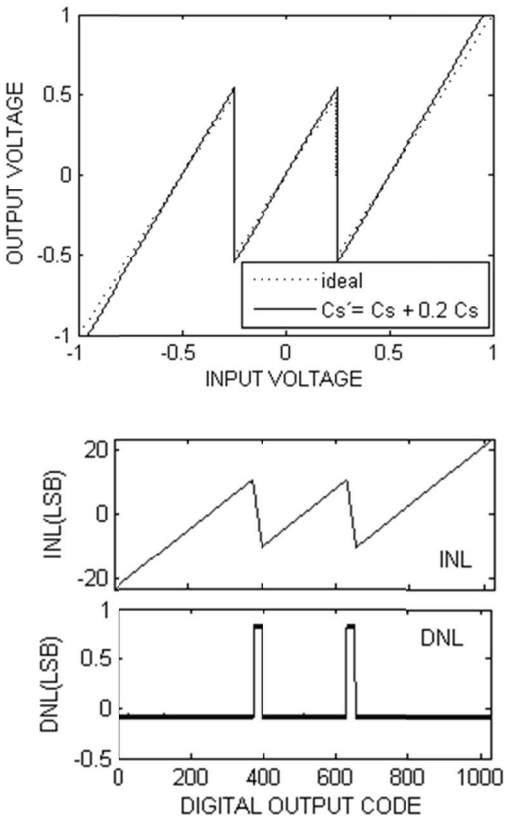


**Fig. 8.** The effect of capacitor mismatch.

where $f_s = 1/T$ is the sampling rate of the pipelined ADC, *N* is the ADC resolution, *n* is the MDAC resolution and $\beta$ is the feedback factor.

## 2.6 Capacitor Matching

The gain of SC MDAC is determined by capacitor ratio $C_S/C_F$ (Fig. 6). If the capacitors $C_S$ and $C_F$ are not equal, then an error proportional to the mismatch is generated in the residue output. Thus, accurate capacitor matching is required to design a high resolution pipelined ADC [7][8][9][10]. The capacitor value is given by

$$C = A.\frac{\varepsilon_{ox}}{t_{ox}} = A.C_{ox} \tag{15}$$

where *A* is the area of a capacitor, $\varepsilon_{ox}$ is the dielectric constant of silicon dioxide, $t_{ox}$ is the thickness of oxide, and $C_{ox}$ is capacitance per unit area.

Capacitance value depends on the area and oxide thickness of capacitor. The main causes of capacitor mismatch are due to over-etching and the oxide-thickness gradient. Since $C_{ox}$ is fixed by process technology, the accuracy of capacitance can be improved by simply increasing the area. However, in SC circuits the accuracy of capacitor ratio is more important than the accuracy of capacitance because the gain of MDAC is defined by the capacitor ratio $C_S/C_F$.

The integrated circuit capacitor can be defined as

$$C' = C + \Delta C \tag{16}$$

where $\Delta C$ is the mismatch error of capacitor $C$.

Then, the ratio of $C'_F$ to $C'_S$ can be written as

$$\frac{C'_S}{C'_F} = \frac{C_S + \Delta C_S}{C_F + \Delta C_F}. \tag{17}$$

Accuracy of capacitor ratio can be improved if the difference of the mismatch errors of both capacitors is as small as possible. A mismatch error in the accuracy of capacitor ratio due to over-etching can be minimized by implementing capacitors with an array of small equal sized unit capacitors. A mismatch error in the ratio accuracy of capacitors due to the variation of oxide thickness can be minimized by laying out capacitors in common centroid geometry.

The influence of capacitor mismatch on the transfer function of 1.5-bit MDAC is illustrated in Fig. 8. The dotted line represents ideal transfer function and the full line shows transfer function with capacitor mismatch. The *INL*, *DNL* for $C_S' = C_S + 0.1C_S$ is shown at the right side. Ideal *ENOB* is 10 bits and after inclusion of mismatching should be closely 10 bits. Therefore good matched capacitor is needed.

## Conclusions

This work deals with basic block of pipelined ADC design requirements. In the first step MATLAB – Simulink model was created, where the ADC resolution, offset of the comparators, gain of the opamp and capacitor mismatch error can be set. Influence of comparator offset is small thanks to RSD correction. However the RSD correction of offset is not infinite – depends mainly on a MDAC resolution [1]. Minimum open loop gain of opamp is defined in (13) and minimum opamp bandwidth in (14). An exact value capacitor is impossible to be fabricated, but mismatch error in the ratio accuracy of capacitors due to the variation of oxide thickness can be minimized enough by laying out capacitors in common centroid geometry.

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## About Authors ...

**Vilem KLEDROWETZ** passed the Bachelor study in microelectronics and technology and master degree in microelectronics at the Faculty of Electrical Engineering and Communication, Brno University of Technology. The topic of his diploma thesis is The Influence of MDAC Resolution on Basic Blocks of Pipelined AD Converter. Nowadays he studies the first year of doctoral degree branch Microelectronics, he is mainly focused on the design of analog integrated circuits and AD/DA converters. He passed a professional internship in ON Design Czech during 2008 and 2009.

**Jiri HAZE** was born in Nachod. He received his MSc., Ph.D. and Ass. Prof. degrees from Brno University of Technology, Faculty of Electrical engineering and Communication, Department of Microelectronics, Czech Republic, in 2002, 2005 and 2009, respectively. Currently he is working as associated professor at the same institution. His research is in the field of integrated circuit design, where his interests include analog and mixed-mode integrated circuit design, signal processing and sensor applications.