Analysis and Design Procedure of LVLP Sub-bandgap Reference - Development and Results

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Abstract. *This work presents an thorough analysis and design of a low-voltage low-power voltage reference circuit with sub-bandgap output voltage. The outcome of the analysis and the resulting design rules are universal and it is supposed to be general and suitable for similar topologies with just minor modifications. The general analysis is followed by a selection of specific topology. The given topology is analyzed for particular parameters which are standard industrial circuit specifications. These parameters are mathematically expressed, some are simplified and equivalent circuits are used. The analysis and proposed design procedure focuses mainly on versatility of the IP block. The features of the circuit suit to low-voltage low-power design with less than 10μA supply current draw at 1.3V supply voltage. For testing purposes a complex transistor level design was created and verified in wide range of supply voltages (1.3 to 3.3V) and temperatures (-45 to 95°C) all in concrete 0.35μm IC design process using Mentor Graphics® and Cadence® software.*

Keywords

Low-voltage, Low-power, Bandgap reference, step-by-step design.

1. Introduction

The bandgap references are most common voltage referencing circuits used both in ASICs or in standard integrated circuits. With reasonable complexity they offer sufficient accuracy and operating range wide enough to be implemented in analog, mixed-signal and memory applications. This work comes after a deep literature study in the BGR field mostly through the IEEE journals etc. (more details in [2]). Since the first publication of a BGR not much development has been done. In 1999 H. Banba et al. presented a circuit allowing low voltage sub-bandgap operation [1]. Since then, a lot of different designs have been presented mostly only modifying Banba's principle, extending it with several types of compensation, additional circuitry etc. The recent attempts to achieve better device to device variation were described e.g. in [4] or the theory was analyzed in [5]. The paper [4] considers injecting the compensation current into the BGR core. The current has similar generation principle and therefore it compensates the process variation. The most of the published papers treat a specific circuit topology and focus on some particular parameter such as accuracy, noise or low-voltage operation. Some papers focus on low-voltage operation optimization beginning with [1] to such designs at the edge of minimal supply voltage of 0.6V in [6] where very low voltage OTA is presented. Nowadays the low-voltage operation is an essential property.

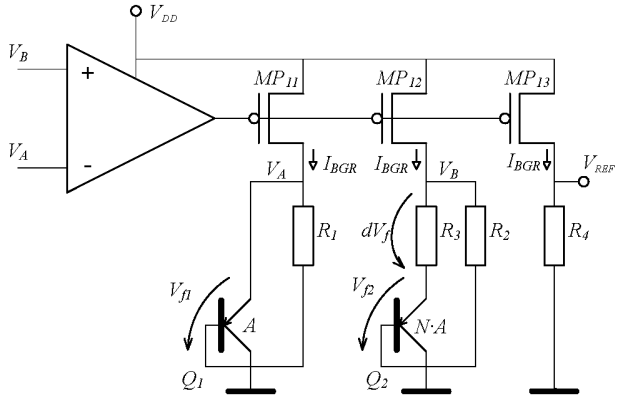

Fig. 1. BGR design according to H. Banba [1].

The aim of this work is to collect, sort and present an understandable BGR design flow with support of necessary analysis and experience with simulations. Each application has different requirements for the voltage reference. This work also shows how to modify or tune the circuit for use in specific designs. The circuit being described here is again a version of Banba's design [1] from Fig. 1. It uses vertical BJTs as generators of both CTAT and PTAT voltage, current mirror as a simple voltage-current converter and OPAMP as a gain component in the feedback loop. The resistors set the correct bias point to achieve minimal (ideally zero) temperature coefficient of the output voltage. The circuit uses common current instead of common voltage as in conventional BGR and therefore it allows low voltage operation. The schematic is shown in Fig. 1. The theoretical minimal supply voltage is given as $V_{DD_{min}} = V_{f1_{max}} +$

$V_{DS_{sat\_min}}$, where $V_{DS_{sat\_min}}$ is a minimal saturation voltage of MP_{11}. The design in Fig. 1 has naturally limited accuracy without any compensation. The value of the output voltage varies with the process and with the temperature although the first order thermal coefficients are canceled. The reference voltage is given by Eq. 1.

$$V_{REF} = R_4 \left(\frac{V_{f1}}{R_2} + \frac{\Delta V_f}{R_3} \right) \tag{1}$$

We assume $R_1 = R_2$ and V_{f1} is defined as voltage across the first (smaller) junction (Q_1). As can be seen the core produces current and the output voltage is determined by the resistor R_4. When more detailed look on device theory is applied, it can be derived that the current is proportional to the bandgap energy of the silicon. Besides the very low-voltage operation, the structure according to Fig. 1 has several disadvantages. The matching in the current mirror introduces an error and the drain-source impedances of $MP_{11,12,13}$ determine the PSRR properties together with the OPAMP. In the conventional BGR only the OPAMP determines the PSRR of the circuit.

1.1 Recent Development

The BGR proceeded though several phases of system design. The basic idea is to divide the entire BGR block into several sub-blocks. Besides the core with the OPAMP it contains the output buffer and startup circuitry. The simulations proved that similar startup properties can be achieved also with self-biased OPAMP. The original idea is depicted in Fig. 2. In recent IP block the startup circuit and Vittoz loop are made optional. For research purposes it is possible to enable/disable those blocks. This solution together with externally biased OPAMP and startup circuitry are made as selectable options. Since a research MPW is planned, there is no constraint on chip area. Externally biased OPAMP has several advantages such as stable parameters (gain, PM, PSRR, etc.) but self-biased OPAMP also comes with interesting properties for this purpose. It also shows lower current consumption of the loop and thus the whole circuit. The self-biased OPAMP is biased by the feedback loops.

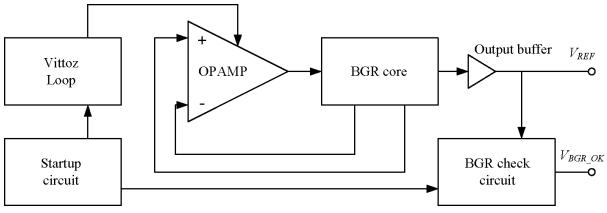

Fig. 2. Block schematic with external biased OPAMP selected.

The BGR check circuit is supposed to be able to distinguish between correct startup and failure of the circuit. It also determines the startup time of the BGR. The high voltage level on the V_{BGR_OK} output signs the circuit is up and has correct output voltage. It compares the reference voltage with a voltage across a PN diode. Since the circuit works as a simple comparator with finite gain the voltage across the diode must be several tens of millivolts lower than V_{REF} at all times.

2. Analysis and Modeling of Used Topology

The expression for the output voltage for the DC bias point (large signal) is written in (1). The reality is different because of several inaccuracies. Those are mainly the spread of the technological process and the mismatch in the same designed devices. The effect of those can be easily seen as an equivalent offset voltage added to one of the inputs of the OPAMP. It is then very readable and comparable with the other sources of inaccuracies expressed as the equivalent offset voltage. The large signal influence of systematic inaccuracies is expressed as:

$$V_{REF} = V_{os\_ls} \left(\frac{R_4}{R_2} + \frac{R_4}{R_3} \right) + R_4 \left(\frac{V_{f1}}{R_2} + \frac{\Delta V_{f1}}{R_3} \right) \tag{2}$$

where V_{os_ls} is sum of all non-random (large signal) factors such as: effect of the finite OPAMP gain, non-ideal current mirror (finite g_m and r_{DS}) etc. The small signal variations can be added-up the same way using the expression:

$$V_{REF} = A_V g_m R_4 \left(V_B - V_A - V_{os\_ss} \right) \tag{3}$$

where A_V is the voltage gain of the OPAMP, g_m is the transconductance of MP_{11} in Fig. 3. Using this, an effect of statistical factors such as mismatch can be calculated all summed up to equivalent small signal offset V_{os_ss}.

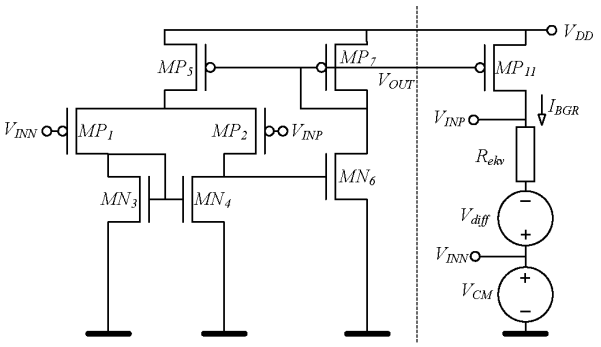

Fig. 3. The simplified feedback loop.

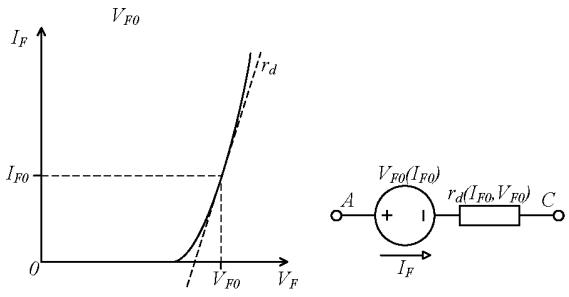

Fig. 4. PN junction linearization.

The topology in Fig. 1 must be treated as a feedback loop. That is a simplification because in fact there are two feedback loops. To be able to estimate the bias point of the loop, it is necessary to simplify the circuit for modeling. The PN junctions are linearized as in Fig. 4. The basic circuit generates the output voltage on the basis of a feedback loop which includes BJTs, the resistor network and the OPAMP. The gain of the OPAMP stabilizes the bias point in the correct position if the values of components are carefully adjusted. This type of BGR employs the logarithmic V-I characteristic of the PN junctions (represented by the vertical BJTs in standard CMOS process). The range of almost pure logarithmic V-I dependence is according to [7] $3 \cdot 10^3 \cdot J_S$ to $3 \cdot 10^4 \cdot J_S$ where J_S is saturation current of PN junction known from the device theory. The bias point of the junction should then be adjusted to be settled reliably in this region. To be able to estimate the bias point of the whole loop, it is necessary to simplify the circuit for further modeling. The differential resistances of the PN junctions and the resistor network can be simplified into an equivalent circuit (Fig. 3). The loop is then closed with the OPAMP and one single PMOS transistor. Fig 3 shows the equivalent circuit of the BGR where: V_{CM} is a voltage across the smaller PN junction at the desired bias point. V_{diff} is given by (4).

$$V_{diff} = V_{f1}\left(1 - \frac{R_2}{R_3 + R_2}\right) + V_T \ln N \left(\frac{R_2}{R_3 + R_2}\right). \quad (4)$$

The equivalent resistance R_{ekv} can be calculated by neglecting differential resistances of PN junctions as in Fig. 4.

$$R_{ekv} = \frac{R_2^2 R_3}{(r_d + R_2)(r_d + R_2 + R_3)} \approx \frac{R_2 R_3}{R_2 + R_3} = R_2 \| R_3. \quad (5)$$

This predicts the behavior and demands on the common voltage range needed for the OPAMP and the current mirroring. In the case of infinite gain of the OPAMP the voltage across R_{ekv} is equal to V_{diff} and the difference between V_B and V_A is zero. In case of finite loop gain and presence of non-zero offset voltage of the OPAMP, the differential voltage varies in small range around zero and can be either positive or negative depending on the current bias conditions.

The circuit has two stable points into which it can converge. First, the correct one with defined non-zero output voltage, and a zero state, when there is no current through BJTs thus no voltage at the output. The crucial properties of the BGR loop for proper start-up strongly depend on the desired supply voltage range and also on the speed, phase and gain characteristic of the OPAMP. These must be evaluated in the designed circuit by a simulation because even rough estimate would be very complicated and probably not very informative. The PSRR and the current consumption directly depend on the resistor network adjustment and the output conductivity of the PMOS current mirror. The PSRR is mostly determined by the current mirror and can be estimated as

$$PSR_{BGR} = \frac{\partial V_{REF}}{\partial V_{DD}} = R_4 \left(\lambda I_{BGR} + A_V g_m PSRR_{OA}\right) \quad (6)$$

where λ is channel length modulation parameter and $PSRR_{OA}$ is PSRR of the OPAMP. A more detailed analysis can be found in [2].

3. Design Procedure of the Core Loop

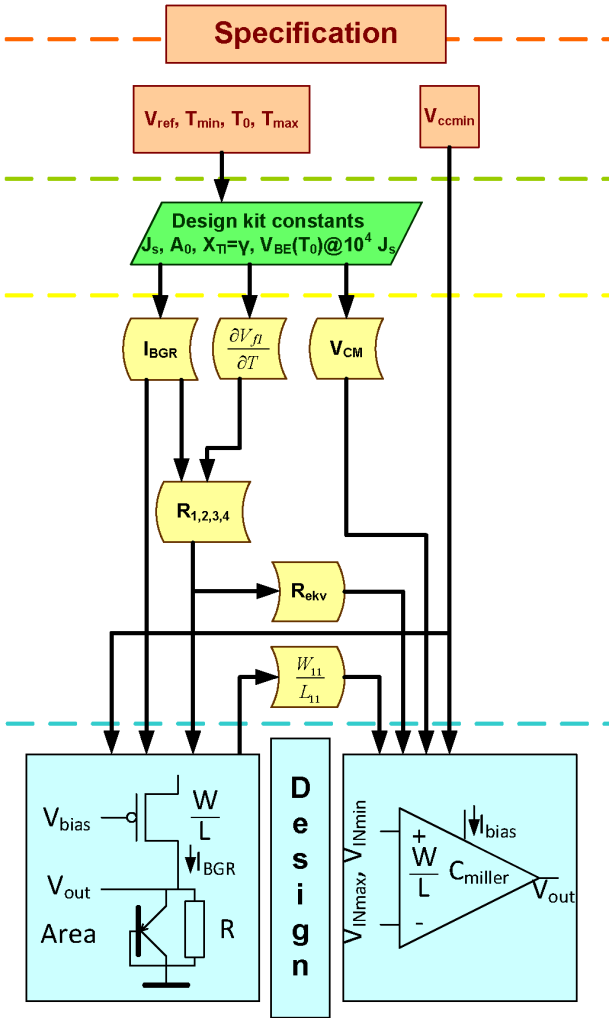

Fig. 5. A flowchart illustrating the design flow.

The very first step of the design has to be the estimation of the forward current through the BJTs. This current is approximately half of the current of I_{BGR} from Fig. 1. The estimate of I_{BGR} is one tenth of the desired current consumption (I_{SUP}) of the entire circuit with some reserve. To minimize the effect of higher orders in the PN junction temperature characteristic, the forward current should be at the high edge of the logarithmic region. This can be found in [7]. If the saturation current density (J_S) is known from the model, the area of the BJTs can be calculated.

$$A_{PN} = \frac{0.1 I_{SUP_{max}}}{3 \cdot 10^4 J_S}. \quad (7)$$

By substitution of device parameters X_{TI} and $V_{f1}(T_0)$ at I_0 to the equation:

$$V_{f1}(T) = V_{G0} + (V_{BE}(T_0) - V_{G0})\frac{T}{T_0} - \\ -X_{TI}V_T \ln\left(\frac{T}{T_0}\right) + V_T \ln\left(\frac{I_C}{I_{C0}}\right) \tag{8}$$

and developing it into Taylor series around T_0 the temperature coefficient $(\partial V_{f1}/\partial T)$ is known.

This theory would probably be better to be applied in the simulator in the chosen design kit. Extraction of all parameters needed would be quite time consuming and not so precise. The selection of N - the ratio between the junction areas is constrained only by maximal area of the chip. Larger ratio means, according to [2], smaller effect of some unwanted features. The ratio should be selected also in order to be able to create common centroid layout.

With the information about the BJT model at specific bias current the resistor network has to be calculated.

$$R_3 = \frac{V_T \ln N}{I_f}, \tag{9a}$$

$$R_2 = R_1 = -R_3 \frac{T\partial V_f/\partial T}{V_T \ln N}. \tag{9b}$$

Now the aspect ratio $(S_X = W_X/L_X)$ of the mirroring transistors $(MP_{11,12,13})$ can be calculated. The estimation of the aspect ratio of the mirroring PMOSTs comes mainly from the voltage budget and requirements that those must be saturated and rather in strong inversion. The maximal aspect ratio of those should be:

$$S_{11_{max}} = \frac{2I_{BGR}}{K_P V_{DS}^2} \tag{10}$$

where $K_P = \mu_P C_{ox}$ and $V_{DS} = V_{DD_{max}} - V_{f1}(T_{min})$. In order to keep the highest possible r_{DS} (thus good PSRR properties) the PMOSTs should be as long as possible.

The suggestions for optimizing the design could be: Resistors $R_{1,2}$ and R_3 adjust the temperature curvature. According to the principle the increase of R_3 causes tilting the slope of the curve at T_0 to negative values, increase of $R_{1,2}$ causes tilting the slope more to positive values and vice versa. Adjusting of R_4 causes proportional increase or decrease of the output voltage at T_0.

The design of the OPAMP must be done with respect to the voltage headroom budget which is likely very low (intended minimal supply voltage is 1.27V). The OPAMP must handle the voltages in their entire range. As a simple and good topology for this the self biased two stage OPAMP depicted in Fig. 3 was chosen as a feedback loop. For the first estimate, transistors MP_5 and MP_7 shall have the same aspect ratio as MP_{11}(the mirror). In the same manner as Eq. 10, considering the maximal and the minimal voltage needed to drive the correct current through MP_{11} in Fig.3, the aspect ratio of MN_6 can be calculated. The first stage of the OPAMP shall be designed with respect to the general rules. More details can be found for example in [8]. The clue for estimating the overall DC gain of the loop is: where A_V is the voltage gain of the OPAMP. For proper startup a Miller compensation capacitor must be added. Calculation of poles and zeros is quite straight forward and is e.g. in [8]. The compensation capacitor is very critical for proper startup and it is probably better to test its value in the simulator with the entire circuit. That is known from the experience with the transistor level simulations.

3.1 Recent Development

A feature of temperature slope trimming was added to the design. Since the effect of the voltage offset of the OPAMP, the accuracy of the devices on wafer and the wafer lot produced are predictable only very roughly or not at all, the resistor network was made trimmable by external digital signal. Each of the resistors R_1, R_2, R_3, R_4 are made as a ladder connected with NMOST switches. The principle os on Fig.6. The signal for gates of the switching NMOSTs is decoded from 4-bit digital signal.

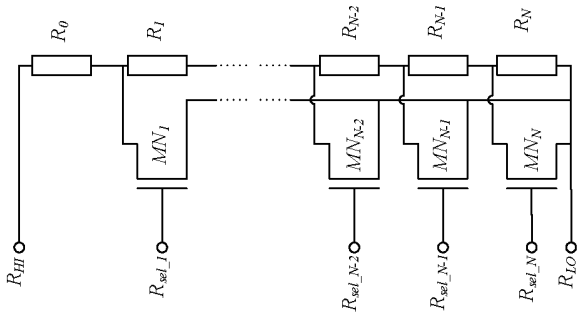

Fig. 6. The resistor ladder for trimming.

4. Partial Verification of the Designed Circuit

The circuit is supposed to be able to establish correct bias point in the entire range of supply voltages, full range of temperatures and, of course, in all technology corners. This is shown in Fig. 8 and also a detailed look at the typical corner is in Fig. 7. The output voltage is set to be approximately 0.7 V. The trimming range of the temperature slope can be seen in Fig. 9. Only extreme values for minimal, typical and maximal trimming word are depicted. The part of the numerical results is in Tab. 1.

A rough estimation of the layout of the main blocks has been made. This is illustrated by Fig.10.

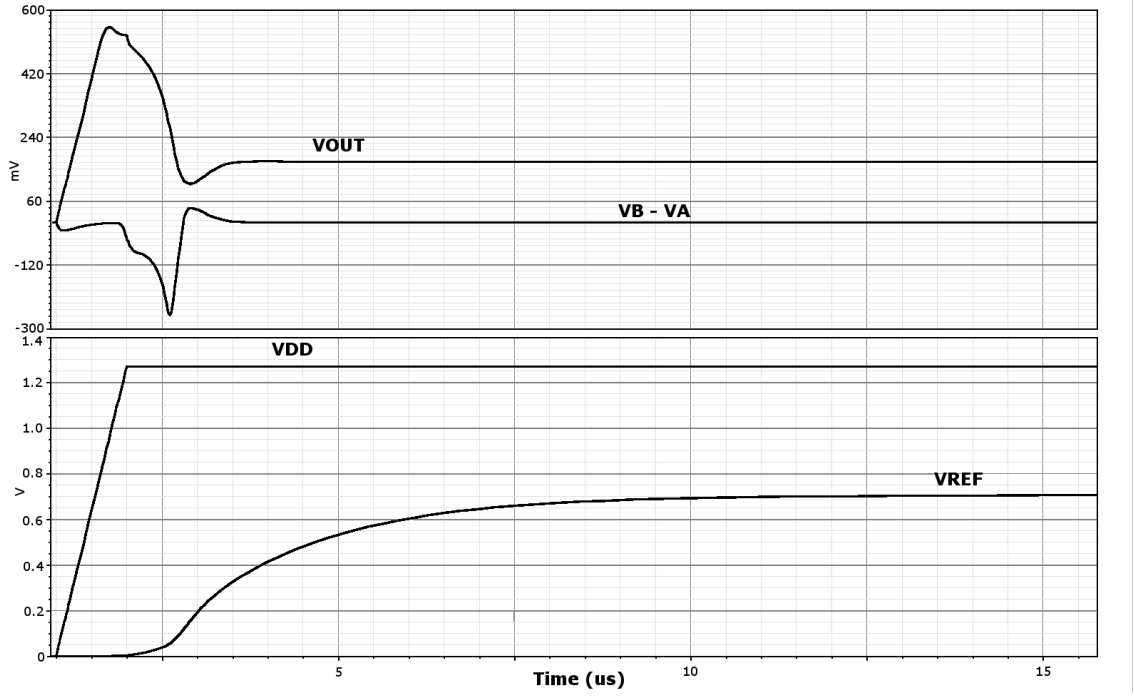

Fig. 7. Startup of the complete circuit in the typical technology corner. **VDD** curve shows ramped supply voltage simulating the real power supply. **VOUT** displays the voltage at the output of the OPAMP. The second waveform shows the differential voltage (**VB - VA**). **VREF** shows the startup of the output voltage from zero to defined voltage.

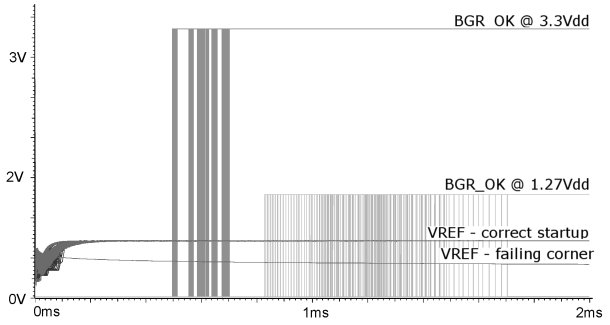

Fig. 8. Startup and BGR OK signal generation in all simulation corners.

	Conditions	Min	Max	Unit
V_{REF} at 27°C	setting 0000 to 1111 V_{DD} =1.27 to 3.33V all corner simulation **Min:** FFmin, 3.33V, 1111 **Max:** SFmax, 1.27V, 1111	697.6	701.9	mV
$T_{C\pm}$ temp. slope	setting 0000 to 1111 V_{DD} =1.27 to 3.33V all corner simulation **Min:** FFmin, 1.27V, 1111 **Max:** SFmax, 3.33V, 0000	-39.42	47.76	μV/K
I_{SUP}	all corner sims setting 0000 to 1111 V_{DD} =1.27 to 3.33V steady state after startup		4.4	μA

Tab. 1. The numerical values of $V_{REF_{min,max}}$ and the temp. slope values for 0000 and 1111 trimming words all across the corners (TT, FFmin, SSmax, FSmin,max, SFmin,max).

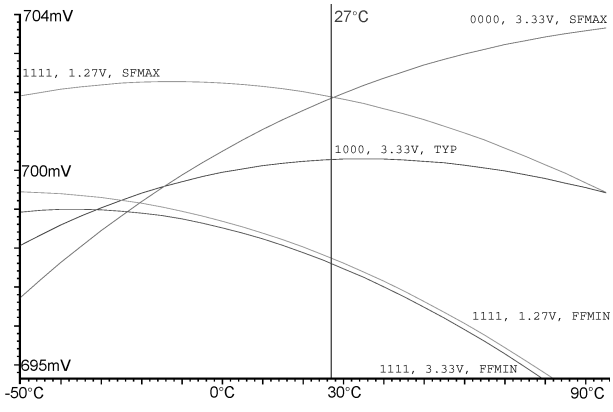

Fig. 9. Trimming range - temperature dependence.

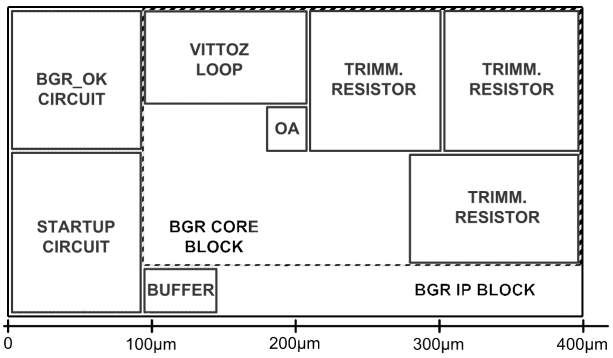

Fig. 10. A layout proposal.

5. Conclusions

A design flow and a part of the verification results of a low-voltage sub-bandgap reference had been presented. It has been verified with commercial simulation tools on the transistor level. The concept was successfully proven to be feasible to prototype as an MPW or as a basic building block of analog or mixed-signal ASICs for example in power management ICs. The actual prototyping (MPW fabrication) is being prepared.

The presented step-by-step design process also underlies the asset of this work. It is focused on creating robust design through estimating reasonable parameter values which follows with the optimization and adjustment according to presented flow.

This article also brings some extension to [9] which has been not included in the original paper.

Acknowledgments

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Pravoslav MARTINEK was born in Ústí nad Labem on 6 September 1936. He received the Electrical engineering degree (Ing.) and PhD (CSc.) degree from the Czech Technical University in Prague, faculty of Electrical Engineering in 1967 and 1974 respectively. In 1968 he joined the Department of Circuit Theory at CTU and has been an associate professor since 1984. His primary research interest is analog signal processing, continuous- and discrete-time analog filters and current-mode electronic circuits. He has been a member of European Circuit Society (ECS) since 1995.