Voltage-Controlled Floating Resistor Using DDCC

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Abstract. *This paper presents a new simple configuration to realize the voltage-controlled floating resistor, which is suitable for integrated circuit implementation. The proposed resistor is composed of three main components: MOS transistor operating in the non-saturation region, DDCC, and MOS voltage divider. The MOS transistor operating in the non-saturation region is used to configure a floating linear resistor. The DDCC and the MOS transistor voltage divider are used for canceling the nonlinear component term of MOS transistor in the non-saturation region to obtain a linear current/voltage relationship. The DDCC is employed to provide a simple summer of the circuit. This circuit offers an ease for realizing the voltage divider circuit and the temperature effect that includes in term of threshold voltage can be compensated. The proposed configuration employs only 16 MOS transistors. The performances of the proposed circuit are simulated with PSPICE to confirm the presented theory.*

Keywords

Floating resistor, voltage-controlled resistor, CMOS, differential difference current conveyor (DDCC)

1. Introduction

The voltage-controlled resistor (VCR) is widely used in analog signal processing. Its applications can be found in telecommunications, electronics and measurements such as active RC filters with variable cutoff frequencies, controlled oscillators, variable gain amplifiers, voltage or current dividers, voltage or current to frequency converters. In VLSI technology, a resistor is formed on silicon wafer. However, resistors of practical values on silicon wafer suffer from limited values and high variability due to process variations. Moreover, its resistance values are not variable. Therefore, they are generally replaced by active resistors. During the last three decades, many approaches for implementing active resistors have been found in the literature [1-9]. In [1], a floating resistor circuit has been proposed to use a transconductance operational amplifier (OTA) as an active element with the inputs connected to the outputs. The active resistor circuits based on the use of the intrinsic resistance of the class-AB configuration have been proposed in [2-3]. However, the limitation of these reported circuits is suffered from the narrow input voltage range (≈ 26 mV). The limitation of the simulated resistance based on the intrinsic resistance of the bipolar class-AB and bipolar OTA configuration is caused by its resistance directly proportional to absolute temperature. Moreover, the high value of total harmonic distortion (THD) and the narrow dynamic range are occurred when the large value of simulated resistance is achieved. The floating resistor circuit based on MOS transistor operating in saturation region has been proposed in [4], but it still suffers from the small input voltage range. The second-generation current conveyor (CCII)-based floating resistor has been reported [5]. However, this CCII is composed of four OTAs and one floating resistor. Then, for a floating resistor, the circuit in [5] employs four OTAs and one floating resistor. New techniques to realize a floating resistor using junction field effect transistor (JFET) and operational amplifiers (op-amps) have been developed by [6-7]. However, they utilize too many external resistors and a number of them float which is not ideal for integrated circuit implementation. Although op-amps is still commercial availability, unlike current conveyors which is very few in integrated circuit (IC) form but this does not affect their popularity amongst researchers, as is evident from the many of published literature [5], [10–20]. Moreover, the circuits based on newer active elements are better targeted for IC implementation rather than for realization using commercial ICs.

Recently, a voltage-controlled resistor using MOS transistor operating in non-saturation region and voltage follower circuit, which is suitable for integrated circuit implementation, has been reported [8]. However, it suffers from the complexity. Due to the design of voltage followers for canceling the nonlinear component term of MOS transistor in non-saturation region, i.e. $(K/2)(V_{DS})^2$. Moreover, it employs two-matched floating resistor. Although, two floating resistors used in [8] do not need to have specified values. However, the floating resistor value about 30 kΩ is used for simulation. The floating resistor realization in [9] requires no passive resistors but still suffers from the difficult design of adder, subtractor and voltage follower circuits for canceling the nonlinear component term. It should be noted that the VCSs in [8] and [9] employ 20 and 17 MOS transistors, respectively.

Recently, Chiu et al. [10] proposed a new current conveyor circuit called a differential difference current conveyor (DDCC). The DDCC has the advantages of both the CCII and the differential difference amplifier (DDA) (such as high input impedance and arithmetic operation capability) [10]. As a result, a number of DDCC-based circuits have been presented in technical literature [10-16].

In this paper, a new voltage-controlled resistor based on DDCC, which is suitable for integrated circuit implementation, is presented. The proposed circuit employs one DDCC and four MOS transistors. By using voltage addition and voltage follower properties that are already included in a DDCC, the nonlinear component term of MOS transistor in non-saturation region $\{(K/2)(V_{DS})^2\}$ can be easily cancelled. Also, the voltage divider can be achieved by using two MOS transistors in cascode form. The proposed resistor employs only 16 MOS transistors. The circuit is simulated by PSPICE program to verify the theoretical prediction.

2. Circuit Description

Fig. 1 shows the principle concept of the proposed VCR, which NMOS M_1 in the non-saturation region is used to configure a floating linear resistor. The voltages V_{D1} and V_{S1} are summed by the summer circuit. The output voltage of the summer circuit will be divided by resistor voltage divider R-R. In the non-saturation region, the drain current of the MOS transistor M_1 can be expressed as [21]

$$I_{D1} = K_n\left((V_{GS1} - V_{Tn})V_{DS1} - \frac{V_{DS1}^2}{2}\right) \quad (1)$$

where the transconductance parameter $K_n = \mu_n C_{ox} W/L$, μ_n is the mobility of the carrier, C_{ox} is the gate capacitance per unit area, W is the effective channel width, L is the effective channel length, V_{Tn} is the threshold voltage NMOS, V_{GS1} and V_{DS1} are the gate-to-source voltage and the drain-to-source voltage, respectively. The equation (1) can be simply rewritten as [9]

$$I_{D1} = K_n\left(V_{GS1} - V_{Tn} - \left(\frac{V_{D1} + V_{S1}}{2}\right)\right)V_{DS1}. \quad (2)$$

From (2), the component term $K_n\{(V_{D1}+V_{S1})/2\}$ should be eliminated to obtained a linear current/voltage (I/V) relationship. Therefore, to obtain a linear I/V relationship, the gate-source voltage of MOS transistor M_1 (V_{GS1}) should be given by

$$V_{GS1} = \frac{V_{D1} + V_{S1}}{2} + \frac{V_B}{2} + V_C \quad (3)$$

where V_C is the control voltage and V_B is the constant voltage.

Equation (3) can be achieved by using the voltage follower and resistive voltage divider R-R as shown in Fig. 1. Substituting (3) into (2), the drain current of the MOS transistor M_1 can be given as

$$I_{D1} = K_n\left(V_C - V_{Tn} + \frac{V_B}{2}\right)V_{DS1} \quad (4)$$

According to (4), a linear relationship between drain current and drain-to-source voltage in Fig. 1 can be obtained.

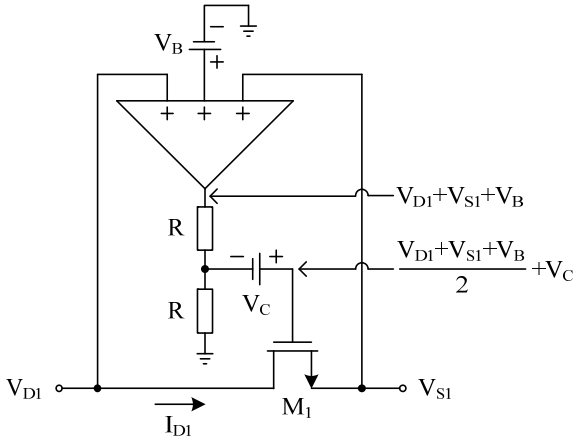


Fig. 1. Principle concept of proposed floating resistor.

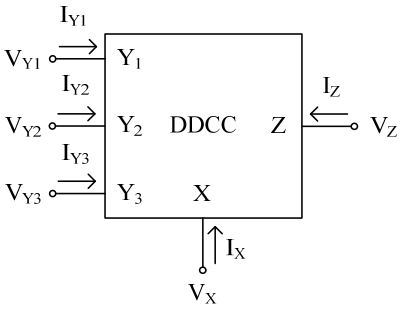


Fig. 2. Circuit symbol of DDCC.

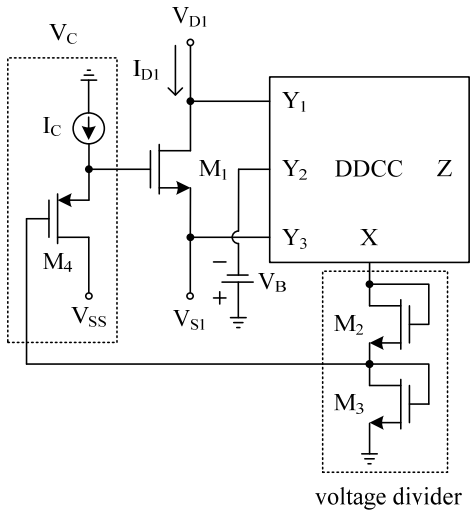


Fig. 3. Proposed DDCC-based floating resistor.

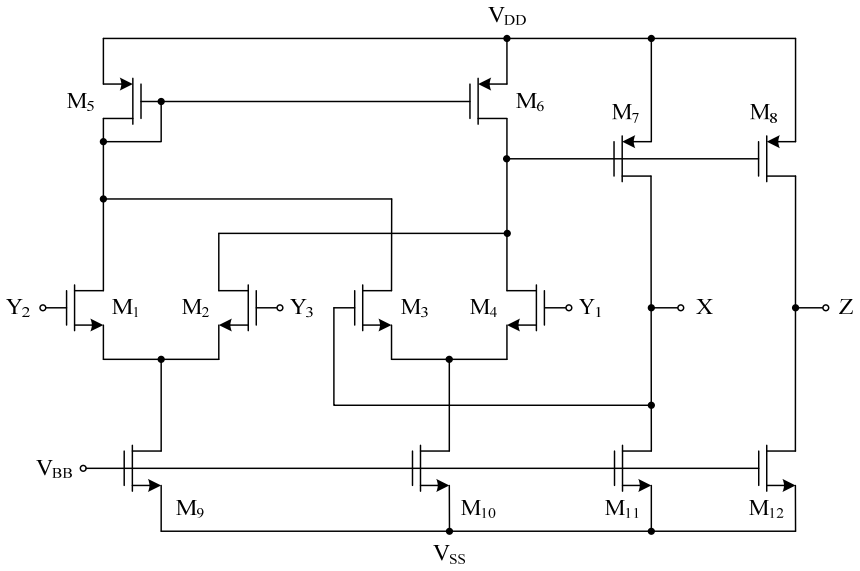


Fig. 4. CMOS implementation for DDCC.

If we let V_B=2V_{Tn}, the resistance value of Fig. 1 can be expressed as

$$R_{DS1} = \frac{V_{DS1}}{I_{D1}} = \frac{1}{K_n(V_C)} \tag{5}$$

which is controlled by V_C. Thus, we have a non-saturation floating resistor with the equivalent resistance inversely proportional to the control voltage V_C. Also, it can be seen from (5) that the circuit can be realized with the resistance without temperature effect in term of the threshold voltage. The linear operation of the proposed resistor, described by (5), is obtained under the assumption that the MOS transistor M_1 operates in the non-saturation region. This assumption is satisfied if

$$V_{GS1} > V_{DS1} - V_{Tn}. \tag{6}$$

From (3) and (6), it follows that the lowest value of the control voltage V_C that provides the linear operation of the proposed resistor is given by

$$V_{C(min)} = \frac{V_{DS1}}{2}. \tag{7}$$

Consequently, from (5) and (7), the maximum equivalent resistance can be achieved for a given V_{DS1} is

$$R_{DS1(max)} = \frac{2}{K_n V_{DS1}}. \tag{8}$$

Fig. 2 shows the electrical symbol of DDCC. It was proposed in 1996 [10] and enjoys the advantage of CCII and DDA such as larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry, low power consumption, high-input impedance [10]. The DDCC has three voltage input terminals: Y_1, Y_2 and Y_3, which have high input impedance. The terminal X is a low impedance current input terminal. There is a high impedance current output terminal Z. The input and output characteristics of the DDCC are described as [10]

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{pmatrix} = \begin{pmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{pmatrix} \tag{9}$$

The proposed floating resistor is shown in Fig. 3. The MOS transistor M_1 in the non-saturation region is used to configure a floating linear resistor. The DDCC operates as voltage summer and voltage follower. Using equation (9), namely V_{Y1}-V_{Y2}+V_{Y3}=V_X, hence the voltage at X-terminal of Fig. 3 is V_X=V_{D1}+V_{S1}+V_B. Also, using MOS diode voltage divider M_2–M_3, it is obvious that the relation of equation (3) is valid. Note that the MOS transistors in the voltage divider M_2–M_3 do not need to have specified conditions but only the same characteristics. In addition, it should be noted that the voltage divider in this paper is the cascode of two MOS transistors M_1-M_2 with grounded form whereas the voltage divider in [8] is two resistors with ungrounded form which is achieved by diffused or polysilicon resistor. Therefore, compared to [8], the voltage divider in this paper has easy implementation. From the proposed floating resistor in Fig. 3, the MOS transistor M_4 and current source I_C are operated as a floating control voltage V_C. The MOS transistor M_4 is the source follower operation. The control voltage can be realized as a variable source-to-gate voltage (V_{SG4}) of MOS transistor M_4 in the saturation region. The control voltage V_C can be given by

$$V_C = V_{GS4} = \sqrt{\frac{2I_C}{K_p}} + V_{Tp} \tag{10}$$

where the transconductance parameter $K_p=\mu_p C_{ox} W/L$ for PMOS transistor, μ_p is the mobility of the carrier of PMOS transistor, C_{ox} is the gate capacitance per unit area, W is the effective channel width, L is the effective channel length, V_{Tp} is the threshold voltage of PMOS transistor. Substituting (10) into (5), yields

$$R_{DS1} = \frac{V_{DS1}}{I_{D1}} = \frac{1}{K_n\left(\sqrt{\frac{2I_C}{K_p}} + V_{Tp}\right)}. \quad (11)$$

Letting $K_n=K_p=K$, equation (11) can be rewritten as

$$R_{DS1} = \frac{1}{\sqrt{2KI_C} + KV_{Tp}}. \quad (12)$$

Thus, this proposed resistor can be additionally considered as a current-controlled resistor. From (12), the temperature effect that is included in term of threshold voltage (V_{Tp}) slightly changes the resistance value. According to (8) and (12), the lowest value of the current control I_C can be given as

$$I_{C(\min)} = \frac{KV_{DS1}^2}{8} - \frac{K^2V_{Tp}^2}{2}. \quad (13)$$

Note from the proposed VCR in Fig. 3 that DDCC-based VCR can be provided the simple configuration. With respect to the proposed VCR, the circuit complexity of voltage follower in [8] is reduced. With respect to the VCR circuit in [9], the proposed circuit enjoys easier realization than the previous VCR circuit where the summer and follower circuits can overcome by using DDCC. Therefore, the resistors can be simply achieved by using one DDCC, one MOS transistor operated in non-saturation region and two MOS transistors operated in saturation region. From Fig. 3 and 4, it can be seen that the proposed circuit consists of 16 transistors and can be fully integrated in CMOS technology.

3. Non-Ideal Effects

To consider the non-ideal effect of a DDCC, taking the non-idealities of the DDCCs into account, the relationship between the terminal voltages and currents can be rewritten as [10]:

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{pmatrix} = \begin{pmatrix} \alpha_1 & -\alpha_2 & \alpha_3 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \beta \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{pmatrix} \quad (14)$$

where $\alpha_1=1-\varepsilon_{1v}$ and ε_{k1v} ($|\varepsilon_{1v}|\ll 1$) denotes the voltage tracking error from V_{Y1} terminal to V_X terminal of the DDCC, $\alpha_2=1-\varepsilon_{2v}$ and ε_{2v} ($|\varepsilon_{2v}|\ll 1$) denotes the voltage tracking error from V_{Y2} terminal to V_X terminal of the DDCC, $\alpha_3=1-\varepsilon_{3v}$ and ε_{3v} ($|\varepsilon_{3v}|\ll 1$) denotes the voltage tracking error from V_{Y3} terminal to V_X terminal of the DDCC and $\beta=1-\varepsilon_i$ and ε_i ($\varepsilon_i\ll 1$) denotes the output current tracking error. Using (12), equation (3) becomes

$$V_{GS1} = \frac{\alpha_1 V_{D1} + \alpha_2 V_{S1}}{2\delta} + V_C \quad (15)$$

where δ is the matching error of the resistor voltage divider R-R (M_2-M_3). Substituting (15) into equation (2), equation (2) becomes

$$I_{D1} = K_n\left(\frac{\alpha_1 V_{D1} + \alpha_2 V_{S1}}{2\delta} + V_C - V_{Tn} - \frac{V_{D1} + V_{S1}}{2}\right)V_{DS1} \quad (16)$$

From (16), the tracking error and the matching error slightly increase the non-linearity of the resistor circuit, namely the nonlinear component $(K/2)(V_{DS})^2$ maybe not eliminated to zero. The matching error of two MOS transistors M_2-M_3 (δ) can be improved by adjusting the aspect ratios (W/L) of MOS transistors M_2 or M_3. Note that the resistance value in Fig. 3 is tuned by adjusting the bias current. If the floating resistor in Fig. 3 is required for tuning by the bias voltage, the bias voltage may be replaced directly instead of the current source or an additional voltage-to-current converter may be used.

4. Simulation Results

The proposed VCR has been simulated by PSPICE. The PSPICE model 1.2μm CMOS parameter through MOSIS for NMOS and PMOS is listed in Tab. 1 [17]. The supply voltages used are ±5 V. The aspect ratios for DDCC are given in Tab. 2 [17]. The bias voltage V_{BB} used for DDCC is -4.5 V and the constant voltage V_B used is 1.38 V. The aspect ratios (W/L) MOS transistors in Fig. 3 for M_1, M_2, M_3, and M_4 are 20μm/10μm, 4.8μm/4.8μm, 4.8μm/4.8μm, and 33.2μm/4.8μm, respectively.

.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=3.0500E-08 XJ=0.200000U TPG=1 VTO=0.6315 DELTA=6.8460E-01 LD=2.8040E-08 KP=7.6909E-05 UO=679.3 THETA=8.2320E-02 RSH=4.4110E+01 GAMMA=0.6672 NSUB=1.7190E+16 NFS=5.9090E+11 VMAX=2.2420E+05 ETA=1.6160E-01 KAPPA=5.1440E-01 CGDO=5.0000E-11 CGSO=5.0000E-11 CGBO=4.2794E-10 CJ=2.8658E-04 MJ=5.3467E-01 CJSW=1.3469E-10 MJSW=1.0000E-01 PB=9.9000E-01
.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=3.0500E-08 XJ=0.200000U TPG=-1 VTO=-0.7989 DELTA=1.7180E+00 LD=1.1000E-09 KP=2.0198E-05 UO=178.4 THETA=8.8040E-02 RSH=1.1510E+02 GAMMA=0.3752 NSUB=5.4370E+15 NFS=5.5960E+11 VMAX=1.4890E+05 ETA=1.0030E-01 KAPPA=1.0000E+01 CGDO=5.0000E-11 CGSO=5.0000E-11 CGBO=4.0045E-10 CJ=2.8863E-04 MJ=4.3630E-01 CJSW=1.7894E-10 MJSW=1.0000E-01 PB=7.5965E-01

Tab. 1. The model parameter of CMOS used in simulation.

MOS transistor	W/L (μm/μm)
M_1-M_4	7.2/4.8
M_5, M_6	39.6/4.8
M_7, M_8	111.6/3.6
M_9-M_{12}	144/4.8

Tab. 2. Transistor aspect ratio of DDCC.

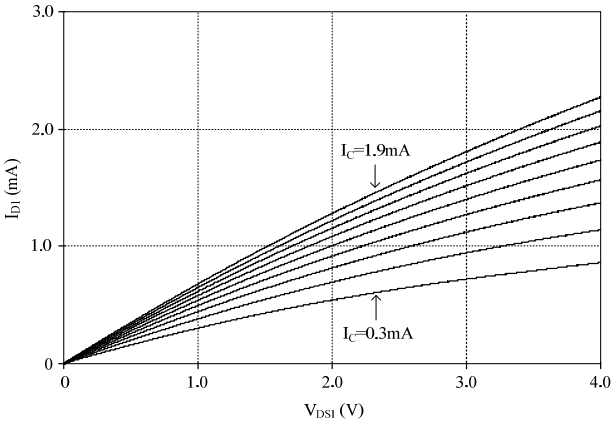


Fig. 5. Simulated resistor current against resistor voltage.

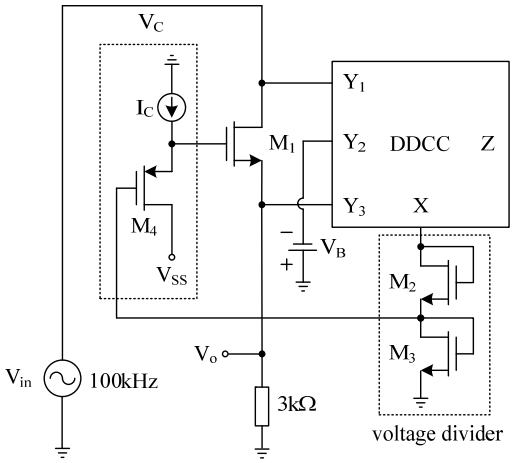


Fig. 6. Voltage divider using the proposed floating resistor.

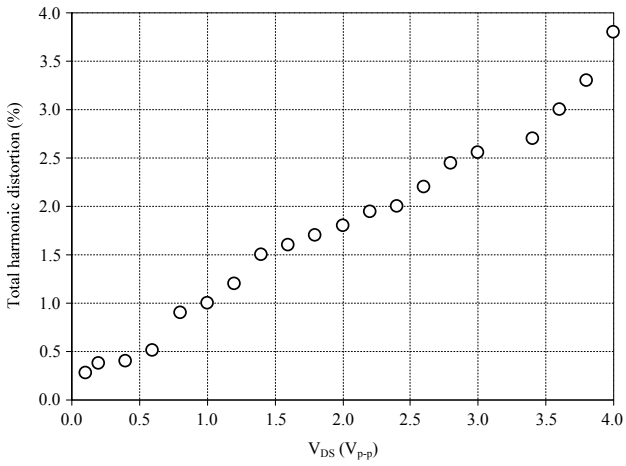


Fig. 7. Distortion against signal amplitude.

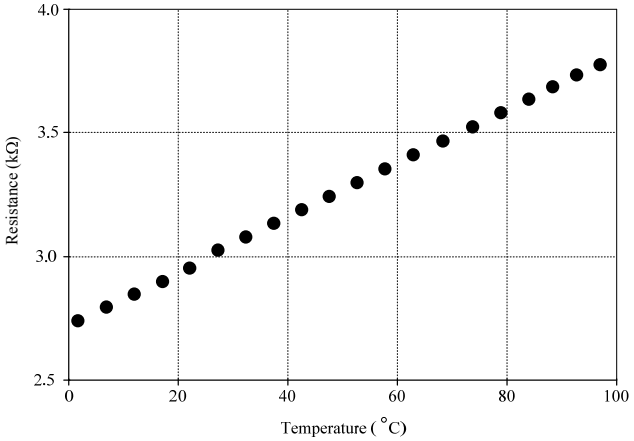
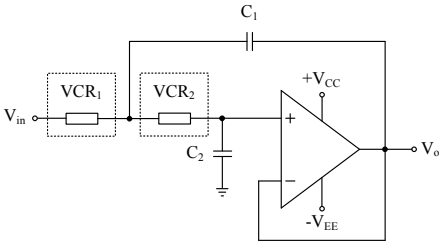
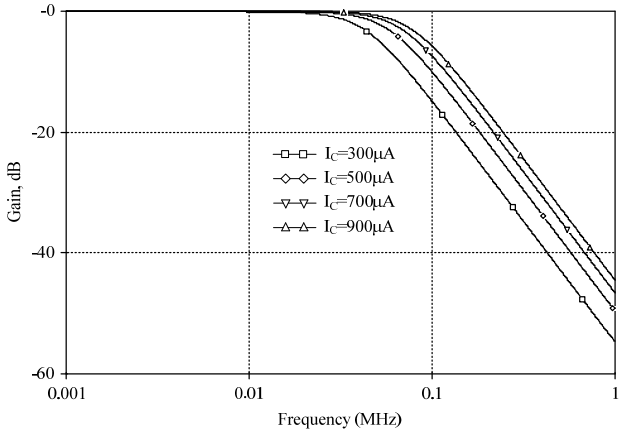


Fig. 8. Resistance values at different temperatures.



(a)



(b)

Fig. 9. (a) The Sallen-Key low-pass filter, (b) the frequency response of the Sallen-Key filter with IC as a parameter.

To avoid the channel length modulation effect, the effective channel length should be larger than 5 μm [6]. Fig. 5 shows the simulation results of I_{D1}-V_{DS1} characteristics with I_C as a parameter. The drain-to-source voltage V_{DS1} of MOS transistor M_1 is swept from 0 V to 4 V. The minimal control voltage $V_{C(min)}$= 2 V is calculated according to (7) and it corresponds to the control current $I_{C(min)}$= 300 μA (K=153.8 μA/V^2) calculated according to (13). To analyze the frequency characteristics of the proposed floating resistor, a voltage divider circuit was designed as shown in Fig. 6. Simulation results at the output V_o showed that, for a $4V_{P-P}$ signal and 100kHz sine wave across the proposed floating resistor, where the current I_C is fixed as 500 μA, the THD was about 3.8%.

Parameter	Proposed VCR	Senani [7]	Tadic et al. (8)	Prommee et al. [9]
Components	1 DDCC (12 MOS's), 4 MOS's, 1 current source	1 or 3 op-amps, 1 MOS of JFET, 4 floating resistors, 1 grounded resistors	20 MOS's, 2 floating resistors, 1 current source	17 MOS's
Supply voltage	±5V	±15V	±6V	±5V
Input range (V_{DS})	4V (V_S=0)	±1V	3V(V_S=2V)	±1V
Suitable for IC	Yes	No	No	Yes
Ease for realization	Yes	Yes	No	No

Tab. 3. Comparison of the proposed VCR with those of previous papers.

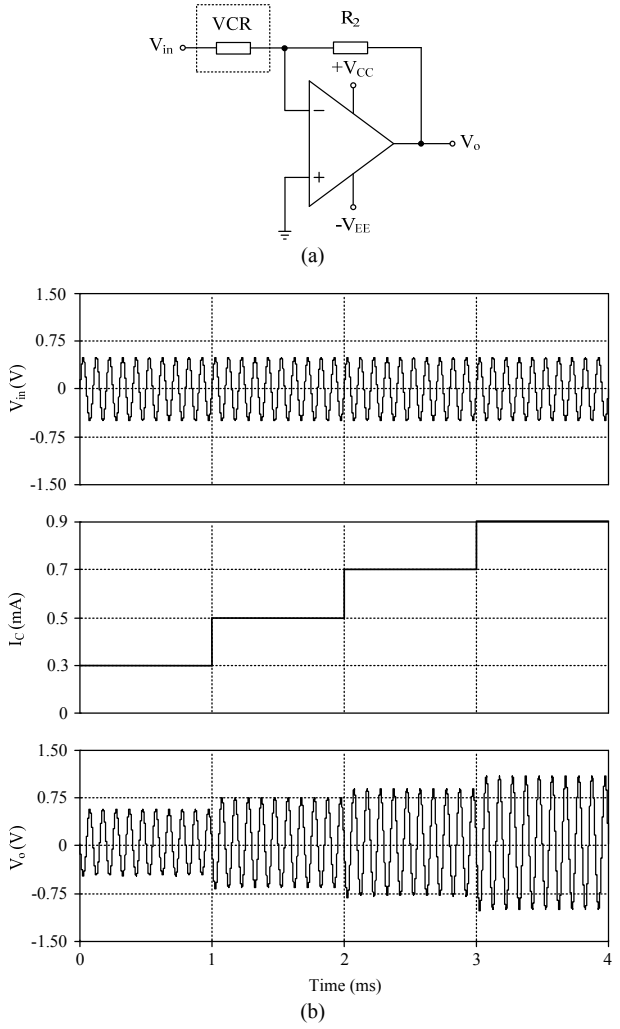


Fig. 10. Voltage controlled amplifier, (b) operation of current-controlled amplifier.

The variation of THD with input signal amplitude for a nominal resistance of 3 kΩ (I_C= 0.5 mA and W/L=20μm/10μm) is illustrated in Fig. 7. Fig. 8 shows the resistance values at temperature of 0 to 100°C where I_C= 500 μA and V_{DS}= 1.5 V. From Fig. 8, the resistance is 2.9 kΩ and 3.64 kΩ at the temperature 0°C and 100°C, respectively. This evaluates that the resistance error is about 20% when the temperature changes from 0°C to 100°C. It is the effect of the transconductance parameter ($K = \mu_n C_{ox} W/L$) that dominates parameters of the proposed circuit which appear in equation (11). This effect may be cancelled by interconnection with the voltage-to-current converter. The parameter μ associated with the temperature effect can be described as $\mu(t) = \mu(T_r)(T/T_r)^{-k3}$[9], where T is absolute temperature, T_r room temperature (kelvin), and k_3 is the constant (1.5 to 2). Finally, sine wave signals ($2V_{peak}$) were supplied to V_{in} of Fig. 6. When the frequencies were increased, it was found that the proposed VCR could operate with the –3dB bandwidth of about 140 MHz.

5. Application Examples

The proposed floating resistor can be applied by analog signal processing circuits. The Sallen-Key low-pass filter and current-controlled amplifier have been used to confirm the operation of the proposed circuit. Fig. 9(b) shows the frequency response of the maximally flat magnitude Sallen-Key low-pass filter shown in Fig. 9(a), where the values of the capacitors are C_1= 1.414 nF and C_2= 0.707 nF. The two floating resistors are implemented using the proposed floating resistor. The resistor magnitudes are controlled by the control current I_C, which is varied from 300 μA to 900 μA. The op-amp was used with the Harris HA 2544, which has a gain-bandwidth product of 50 MHz. Fig. 10(b) shows the operation of current-controlled amplifier shown in Fig. 10 (a) where the value of the resistor R_2 is 4 kΩ. The resistor R_1 is implemented using the proposed floating resistor. The 1 V_{p-p} sine wave of frequency 10 kHz is applied into the input V_{in} of Fig. 10 (a). The resistor magnitudes are controlled by the control current I_C, which is increased as 300 μA, 500 μA, 700 μA and 900 μA.

6. Conclusions

A new simple voltage-controlled floating resistor is presented. The proposed circuit consists of one DDCC and four MOS transistors, and can be fully integrated in CMOS technology. The DDCC is employed to provide a simple circuitry of the circuit. The voltage divider in this paper is implemented by cascode of two MOS transistors M_1-M_2 and the nonlinear component term $\{(K/2)(V_{DS})^2\}$ can be easily eliminated by using DDCC. The proposed voltage-controlled resistor is very suitable for implementation in CMOS VLSI circuits which interface the continuous analog signal carrying the measuring information to the digital signal processing circuits. A comparison of this paper and previous works is summarized in Tab. 3.

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