A New Low-Power CMOS Quadrature VCO with Current Reused Structure

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Abstract. *A new quadrature voltage controlled oscillator (QVCO) circuit topology is proposed for low-voltage and low-power applications. In the proposed circuit, two oscillators with current-reused structure are coupled to each other by two P&N-MOS pairs. In this way, low phase noise quadrature signals are generated with low-voltage and low-power. The simulation is made by Cadence in chartered 0.18 μm CMOS process. The simulation result shows that the QVCO phase noise is approximately -117.1 dBc/Hz at 1MHz offset from 1.8 GHz operation frequency. The QVCO dissipates 1.92 mW with a 1.1 V supply voltage.*

Keywords

Coupling, P&N-MOS pair, VCO, Low-power, Low-voltage, Phase noise, Oscillator, Quadrature.

1. Introduction

Recently, the monolithic integrated chip with low-voltage and low-power has been increasingly concerned in wireless communication systems. The direct-conversion transceiver has been dramatically increased in recent years because of low-power, low cost, and low phase error requirement [1]. The quadrature VCO is one of the key elements in direct-conversion transceiver system. The design of QVCO mainly focuses on low cost, low phase noise, low-power [2]. There are normally three ways to generate quadrature signals [3]. Firstly, the quadrature signals can be obtained by feeding the differential outputs of VCO to a poly phase filter [4]. It is hard to get accurate quadrature signals because the resistors and capacitances are seriously sensitive to parasitic and process variation at a high operation frequency. The second way is to make the VCO work at double the desired frequency, and the quadrature signals at the desired frequency can be gotten by a frequency divider [5], [6]. This approach has the advantage of avoiding any pushing and pulling effect on the VCO. However, a higher oscillation frequency and the frequency-dividing circuit result in an increased power consumption level. The third way is to couple two identical LC-tank oscillators [7-12]. This method provides wide-band quadrature accuracy and superior phase noise performance. However, it should be pointed out that this QVCO needs two identical LC-VCOs. Therefore, the power and the area should be carefully considered.

In the third method, several kinds of VCOs are used to generate quadrature signals by different coupling methods. One of the most common LC-tank oscillators is the complementary LC-VCO [13], which can be coupled to generate quadrature signals through simple coupling ways [7-9]. This structure has the benefit of generating symmetric waveforms and minimizing the up-conversion gain of low frequency noise. However, it is not easy to operate under low voltage environment because the supply voltage flows through three stacks of MOS transistors, and the power is very large. Then only NMOS cross-coupled VCO [14] and only PMOS cross-coupled VCO [15] are used to generate quadrature signals [10], [11], those structures can be operated under a low supply voltage, and it is also very convenient to be coupled by simple MOS transistor pairs. However, the cross-coupled MOS transistors are always in conductive state during the whole period. Then the power is still relatively large. Since low power is becoming the focus in the design, the current-reused structure VCO [16] is adopted to generate quadrature signals. It is different from the conventional cross-coupled LC VCO [17], the transistors of this VCO are only switched on in the first half of period, which greatly reduces the power dissipation. However, the coupling way of this VCO is different from the conventional VCO. The conventional parallel or serial coupling way can not make this VCOs work normally. For this reason, Huang [12] proposed CR-QVCO by combining the current-reused topology with the transformer-coupling scheme, which can achieve low power and low supply voltage. However, the phase noise is not very good because the quality-factor of the integrated transformer is very low, and the implement circuit is also complicated.

In this paper, a new QVCO for low-voltage and low-power applications is proposed. The circuit is based on two identical current-reused VCOs, which are coupled to each other by simple P&N-MOS pairs. It not only takes the advantage of current-reused structure VCO, but also adopts the simple P&N-MOS coupling way, which reduces the complication of the related QVCO, and avoids the draw-

backs caused by transformer coupling in reference [12]. Therefore, the proposed QVCO has the characteristics of low voltage, low power, low phase noise and simple structure.

2. Proposed Quadrate Oscillator

The schematic of the proposed P&N-MOS pair QVCO is shown in Fig. 1. It mainly consists of two identical current-reused structure LC-VCOs. The P&N-MOS pairs are used to couple the VCOs for generating quadrate output signals, and four resistors are used to adjust the DC operation point of this circuit, which makes the output voltage more symmetrical. Unlike the operation of the complementary transistors in a conventional CMOS QVCO, this topology uses both NMOS and PMOS transistors as a negative conductance generator. The series stacking of the NMOS and PMOS drive the current in the half of period and let the LC tank discharge in another half period to create the oscillation, then the power is greatly reduced. As there is no current limiting structure in this VCO, a relatively large transistor's length should be set to limit the circuit's operation current. The threshold voltage of the transistor can be reduced by enlarging the transistor's width, and only two stages of transistors are used from supply voltage to ground voltage, which makes this VCO work under low voltage environment. Furthermore, the phase noise is better than conventional low power dissipation VCO.

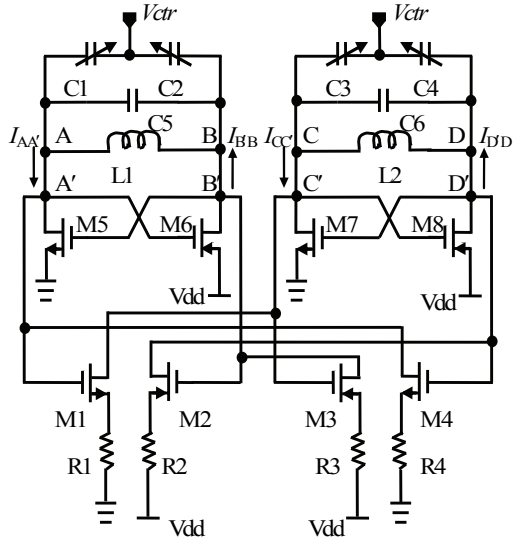

Fig. 1. The proposed P&N-MOS pair coupling QVCO.

2.1 The Current Reused LC-VCO Analysis

The large signal equivalent circuit of the current-reused LC-VCO [16] is shown in Fig. 2, where C_L is the tank loaded capacitor and C_P are the parasitic capacitors of the transistors of M1 and M2. As is shown in Fig. 2(b), the voltage of node A is high and the voltage of node B is low, which makes the transistors of M1 and M2 switched on simultaneously in the first half of period. On the contrary, as is shown in Fig. 2(c), the transistors are switched off simultaneously in the last half of period. The transistors of the conventional LC VCOs are switched on alternately, but the transistors of the current reused VCO are switched on and off simultaneously, which makes the VCO save half of the power.

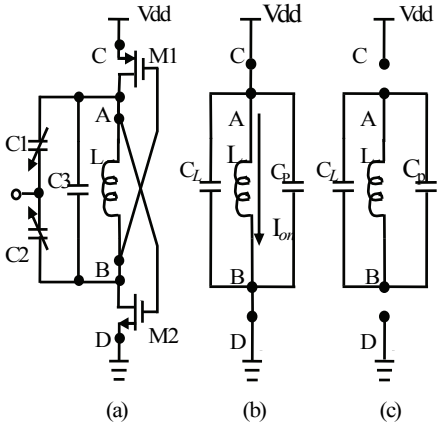

Fig. 2. The current reused LC-VCO.

2.2 P&N-MOS Pair Coupling Analysis

The coupling principle is as follows. As shown in Fig. 1, the current across the transistor M1 (I_{ds1}) and M7 (I_{ds7}) are expressed in (1):

$$I_{ds1} = (V_A - V_{R1}) \cdot g_{m1}, \; I_{ds7} = V_D \cdot g_{m7} \tag{1}$$

where V_A and V_D are the voltages of node A and node D respectively, V_{R1} is the voltage across the resistor R_1, g_{m1} and g_{m7} are the transconductances of the transistors M1 and M7 respectively.

The current $I_{CC'}$ is depicted in (2):

$$I_{CC'} = I_{ds1} + I_{ds7} = (V_A - V_{R1}) \cdot g_{m1} + V_D \cdot g_{m7}. \tag{2}$$

Since the resistances in this circuit are mainly to make the output waveform stable and the value is very small, the voltage across the resistor R_1 can be ignored.

At the time of AC signal analysis,

$$v_C = -v_D. \tag{3}$$

Therefore, (2) can be simplified, as depicted in (4):

$$i_{CC'} = v_A \cdot g_{m1} - v_C \cdot g_{m7}. \tag{4}$$

The voltage of Node C is expressed in (5) at the time of AC signal analysis.

$$v_C = v_D - i_{CC'} \cdot Z(jw) \tag{5}$$

where $Z(j\omega)$ is the impedance of the resonance net.

Combining (3) and (5), the equation (6) can be obtained as

$$v_C = \frac{-i_{CC'} \cdot Z(jw)}{2}. \quad (6)$$

Combining (4) and (6), the equation (7) can be obtained as

$$v_C = \left(v_C - \frac{g_{m1}}{g_{m7}} v_A\right) \cdot \frac{g_{m7} Z(jw)}{2}. \quad (7)$$

The current $I_{AA'}$ is depicted in (8):

$$I_{AA'} = I_{ds4} + I_{ds5} = (V_D - V_{R4}) \cdot g_{m4} + V_B \cdot g_{m5}. \quad (8)$$

The voltage across the resistor R_4 can be also ignored, the reason is the same as mentioned above.

At the time of AC signal analysis:

$$v_B = -v_A. \quad (9)$$

Combining (3), (8) and (9), equation (8) can be simplified, as depicted in (10):

$$i_{AA'} = -v_C \cdot g_{m4} - v_A \cdot g_{m5}. \quad (10)$$

The voltage of Node A is expressed in (11) at the time of AC signal analysis.

$$v_A = v_B - i_{AA'} \cdot Z(jw). \quad (11)$$

Combining equations (9), (10) and (11), the equation (12) can be obtained as

$$v_A = \left(v_A + \frac{g_{m4}}{g_{m5}} v_C\right) \cdot \frac{g_{m5} Z(jw)}{2}. \quad (12)$$

Now adjust the parameters of the transistors, and make sure the transconductances of the transistors meet equation (13):

$$g_{m1} = g_{m4}, \; g_{m7} = g_{m5}. \quad (13)$$

Combining (7), (12) and (13), the equation (14) can be obtained as

$$v_A^2 + v_C^2 = 0, \; v_A = \pm j \cdot v_C \quad (14)$$

According to the principles described above, (15) can be obtained:

$$v_B^2 + v_D^2 = 0, \; v_B = \pm j \cdot v_D. \quad (15)$$

Equation (14) and (15) show that quadrature differential signals are generated.

3. Simulation Result

The proposed quadrature LC-VCO is simulated in chartered 0.18μm CMOS process by Cadence. The output quadrature waveforms in 1.8 GHz are shown in Fig. 3. Fig. 4 shows the simulated phase noise of this work, the phase noise at 1 MHz offset is -117.1 dBc/Hz while the carrier is 1.8 GHz. The VCO's output frequency tuning range is illustrated in Fig. 5. The layout is shown in Fig. 6, and the chip area is 0.28 x 052 mm^2. This VCO operates with the 1.1 V supply voltage and the power consumption is 1.92 mW.

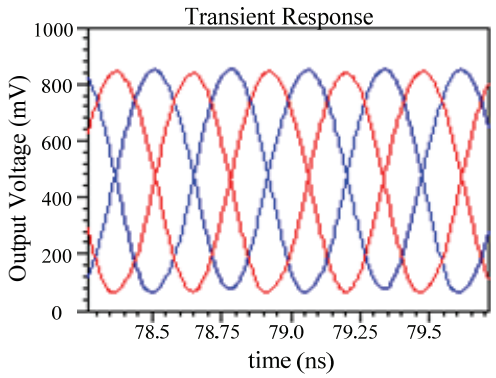

Fig. 3. The quadrature output waveforms at 1.8 GHz.

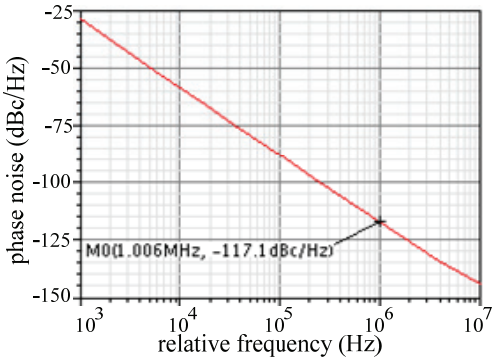

Fig. 4. The output phase noise at 1.8 GHz.

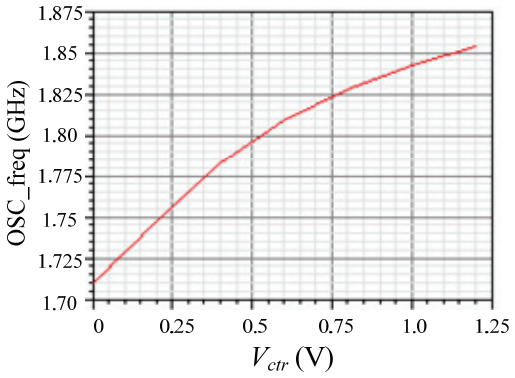

Fig. 5. The output frequency versus the control voltage of QVCO.

The Figure of Merit (FOM) introduced in [18] is used:

$$FOM = L(\Delta\omega) - 20 \log\left(\frac{\omega_0}{\Delta\omega}\right) + 10 \log\left(\frac{P_{dc}}{1mW}\right) \quad (16)$$

where L(△ω) represents the phase noise at the offset frequency of △ω, P_{dc} is the power dissipation in the QVCO. Based on this definition, the *FOM* of the proposed QVCO is -179.4 dBc/Hz. A list of performance of this

work and previously published QVCO is shown in Tab 1. This QVCO has the characteristic of low power, low phase noise and simple structure by contrast.

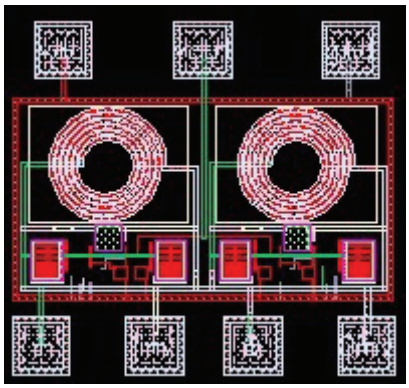

Fig. 6. The layout of the proposed QVCO.

Ref.	Tech [μm]	Freq [GHz]	Power [mW]	Vt (V)	P.N [dBc/Hz]	FOM [dBc]
[7]	0.18 CMOS	4.06	13.7	1.8	-108 [@1MHz]	-172.5
[8]	0.18 CMOS	5.28	11.2	1.4	-119.3 [@1MHz]	-183
[9]	0.18 CMOS	2.4	10.8	0.6	-104.69 [@1MHz]	-171*
[10]	0.18 CMOS	5.2	14.7*	1.5	-116 [@1MHz]	-179.8*
[11]	0.18 CMOS	3.6	14.6	1.8	-113.5 [@1MHz]	-173*
[12]	0.18 CMOS	7.128	2.2	1.0	-111.2 [@1MHz]	-184.8
This work	0.18 CMOS	1.8	1.92	1.1	-117.1 [@1MHz]	-179.4

*the result is estimated

Tab.1. Performance summaries of the proposed QVCO and comparison with other published QVCO.

4. Conclusion

A new P&N-MOS pair coupling QVCO has been presented in this paper. It has the advantage of low voltage, low power, and simple structure. The simulation is made by Cadence in chartered 0.18 μm CMOS process. The QVCO phase noise is approximately -117.1 dBc/Hz at 1 MHz offset from 1.8 GHz operation frequency while dissipating 1.92 mW from a 1.1 V supply. It is suitable for low-voltage and low-power wireless communication system applications.

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