Current-Mode Dual-Phase Precision Full-Wave Rectifier Using Current-Mode Two-Cell Winner-Takes-All (WTA) Circuit

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Abstract. *In addition to the recently proposed full-wave rectifier by Prommee et al. [25] using voltage-mode (VM) two-cell winner-takes-all (WTA) circuit, we present current-mode (CM) precision full-wave rectifier using CM two-cell WTA circuit. The popular Lazzaro's CM WTA circuit has been employed for the purpose and there is no requirement of inverting the input signal as in [25]. Also, dual complimentary phases of the output current signal are available from high-output impedance terminals for explicit utilization. As compared to many recently proposed CM rectifiers using complex active devices, e.g. dual-X current conveyor or universal voltage conveyor, our circuit is very compact and requires a total of 21 transistors. SPICE simulation results of the circuit implemented using 0.35 μm TSMC CMOS technology are provided which verify the workability of the proposed circuit.*

Keywords

Analog signal processing, current-mode, precision full-wave rectifier, instrumentation, measurement, WTA circuit.

1. Introduction

Precision rectifiers serve as very important blocks for instrumentation and measurement and they are used in numerous applications such as ac volt- and ampere-meters, signal polarity detectors, frequency doubling, RMS to DC conversion, peak/valley detection and averaging circuit [1]. Consequently, a number of realizations of both voltage-mode (VM) and current-mode (CM) precision rectifiers using variety of active building blocks (ABBs) can be found. Basic and well known solutions using operational amplifiers [1] operate well only at low frequencies [2], [3] due to the finite slew-rate and effects caused by diode commutation. Therefore, for high-frequency applications other active elements such as current conveyors (CCs) [4]–[8], current-controlled current differencing buffered amplifiers (CC-CDBAs) [9], operational transconductance amplifiers (OTAs) [10]–[12], current differencing transconductance amplifiers (CDTAs) [13], [14], voltage conveyors (VCs) [15] (and references cited therein). Most of these realizations are non-optimal in terms of the number of transistors employed and they require multiple ABBs (often, with unused terminals) for their creation. For example, the CM rectifier in [9] employs three CC-CDBAs. The resulting circuit has several unused terminals of the employed ABBs, e.g. the *w* terminals of the second and third CC-CDBA are unused, that is, the voltage-buffers of the second and third CC-CDBA have no functionality and should be removed, since they unnecessarily consume the biasing current and serve no "real-purpose". Similarly, the circuits in [15], employing current and voltage conveyor, also have several unused terminals which are not required. An interesting all-CMOS rectifier has been proposed in [16] which utilized the class B operation of the CMOS second-generation current conveyor (CCII). This circuit, however, requires the input current signal to be four times more than the biasing current of the CCII, i.e. $I_{in} > 4I_B$ and thus offers reduced precision for very low input signal amplitudes. The circuit also requires differential current signals for full-wave rectification. Other solutions of all-CMOS precision rectifiers can be found in [17]–[19]. In [18] and [19] the authors present a high-frequency half-wave rectifier that, however, requires a number of different bias currents and is generally based on the solution of an full-wave rectifier already discussed in [20], where current conveyor and current mirrors are used.

One of the most recent additions to all-CMOS precision rectifiers is by Minaei *et al.* [21]. The circuit in [21] is a current-mode precision rectifier and uses a small number of transistors (including bias voltage generators), however, this circuit requires precise threshold voltage extractors and bases itself on the concept that MOS transistors are OFF when the magnitude of gate-source voltage difference is less than the threshold voltage (V_{TN} or V_{TP}). This is of course never the case for practical MOS transistors and sub-threshold conduction can lead to large errors in the output if the input signal is of small amplitude.

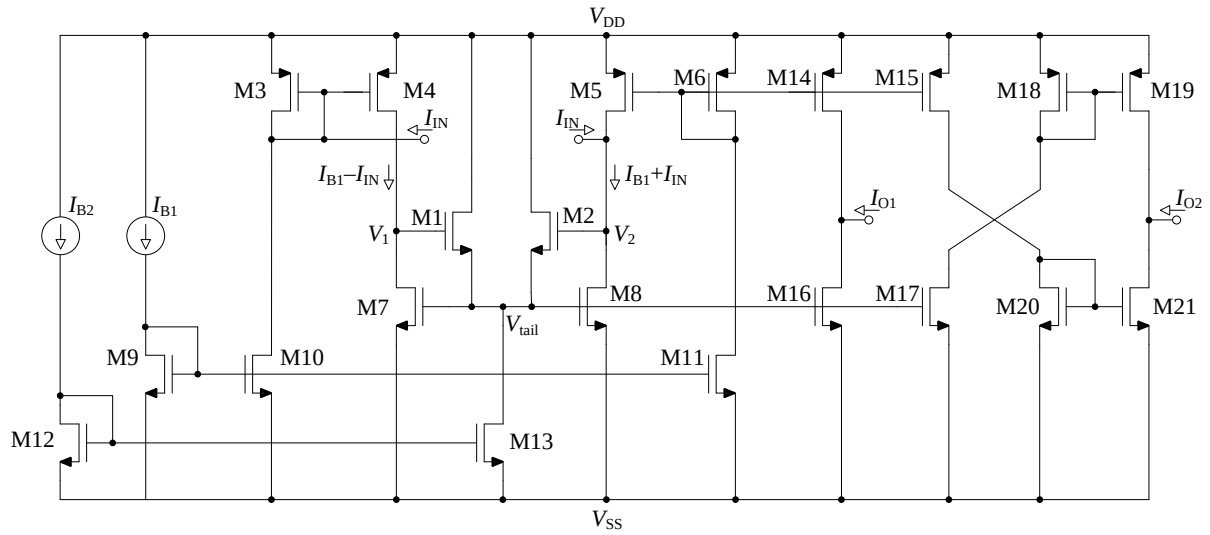

Fig. 1. CMOS implementation of the precision CM full-wave rectifier using WTA circuit.

The use of winner-takes-all (WTA) maximum/minimum circuits for wide-band precision voltage rectification has been discussed by Opris in [22]. Two input maximum circuit has been used for full-wave rectification of 500 kHz voltage input signal (see Fig. 4.4 of [22]). Other min-max current selectors are described in [23] and [24] that, however, provide small input range (about 20 μA). Recently, Prommee *et al.* proposed a new type of VM full-wave rectifier based on their voltage-mode winner-takes-all (WTA) circuit [25]. Since a WTA circuit chooses a winner from a group of input signals, a two-cell WTA maximum circuit with inputs of V_{in} and $-V_{in}$ produces the output as $|V_{in}|$. This circuit, however, requires an additional voltage inverter to produce a 180° phase shifted signal for the second input of the WTA and hence, the signal distortion (in terms of both the amplitude and phase of the second-input with respect to the first input) affects the output. The affect of distortion would become prominent at high input frequencies near the closed-loop bandwidth of the inverting amplifier. In this work, we present the current-mode version of [25], wherein a two-cell CM Lazzaro's WTA circuit [26] is employed. The circuit does not require a buffer to invert the input signal as in [25], since owing to the current inputs, addition and subtraction of the currents can be accomplished by feeding the current at appropriate terminals. Moreover, our circuit also provides dual complimentary phase output signals from high-output impedance terminals. SPICE simulation results of the circuit implemented using 0.35 μm TSMC CMOS technology are provided which verify the feasibilities of the proposed circuit.

2. Proposed Precision Rectifier

The proposed dual-phase full-wave CM rectifier is shown in Fig. 1. The circuit is built around two-cell CM Lazzaro's WTA circuit [26]. The circuit operation can be understood as follows: when $I_{IN} = 0$, $V_1 = V_2$ and the drain current of $M1$ and $M2$ is $I_{B2}/2$ (that is the tail current of the differential amplifier is shared equally between both the cells). Now when the input current is slightly increased, i.e. $I_{IN} < 0$, there is a large increase in V_1 due to the high impedance at this node and which causes increased drain current in $M1$. The rise in V_1 further increases V_{tail} causing large decrease in V_2 due to the high impedance at this node and which causes the drain current of $M2$ to reduce. This regenerative action continues to increase drain current of $M1$ and reduce the drain current of $M2$ until all the tail current I_{B2} is steered in the left cell, i.e. $I_{D_{M1}} = I_{B2}$ and $I_{D_{M2}} = 0$. Under these conditions transistor $M8$ enters deep triode region and $I_{D_{M7}} = I_{D_{M16}} = I_{B1} + I_{IN}$. With the same reasoning as above, when $I_{IN} > 0$, the complete tail current I_{B2} is steered into the right cell, $I_{D_{M2}} = I_{B2}$, $I_{D_{M1}} = 0$ and $I_{D_{M8}} = I_{D_{M16}} = I_{B1} - I_{IN}$. In either case, $I_{O1} = -I_{O2} = |I_{IN}|$. From Fig. 1 it is clear that the input current has to drive both neurons of the winner-takes-all circuit. Therefore an additional dual-output current mirror has to be used (e.g. as shown in Fig. 2, a simple CCII+/+ [27] with Y-terminal grounded).

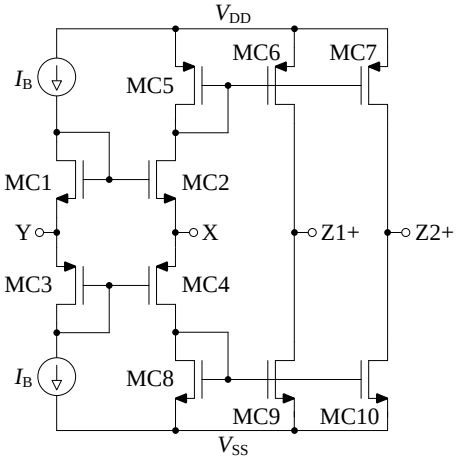

Fig. 2. Basic CMOS implementation of dual output CCII+/+.

3. Simulation Results

To verify the behavior of the proposed current-mode precision rectifier, the structure in Fig. 1 together with CCII+/+ from Fig. 2 has been simulated. The transistor parameters used for the simulations are taken from TSMC 0.35 μm process [28] (level 7). The aspect ratios of all NMOS and PMOS transistors are 17/0.9 μm/μm and 30/0.9 μm/μm, respectively. The supply voltages are taken as $V_{DD} = -V_{SS} = 1.5$ V, the bias currents are $I_{B1} = I_{B2} = 20\,\mu$A, $I_B = 50\,\mu$A. The simulated DC current transfers of the rectifier are shown in Fig. 3. From Fig. 3a, for input signal with amplitude 105 μA the error in current gain of the rectifier remains bellow 5 %. Analysing the graph from Fig. 3b showning the zero crosing arrea, the offset is $-0.5\,\mu$A for I_{O1} and 0.3 μA for I_{O2}, the minimal amplitude of the input signal that can generally be rectified is 0.74 μA.

To evaluate the accuracy of the current-mode full-wave rectifier from Fig. 1 the DC value transfer p_{DC} and RMS error p_{RMS} have been analyzed [29]:

$$p_{DC} = \frac{\int\limits_T y_R(t)\,dt}{\int\limits_T y_{ID}(t)\,dt}, \tag{1}$$

$$p_{RMS} = \sqrt{\frac{\int\limits_T [y_R(t) - y_{ID}(t)]^2\,dt}{\int\limits_T y_{ID}^2(t)\,dt}} \tag{2}$$

where the $y_R(t)$ and $y_{ID}(t)$ represent the actual and ideally rectified signal and T is the period of the input signal. The ideal behavior of the rectifier is characterized by the values $p_{RMS} = 0$ and $p_{DC} = 1$.

The simulation results of the frequency dependent DC value transfer and RMS error for chosen values of amplitudes I_{IN} are shown in Fig. 4a and Fig. 4b. If the frequency increases and/or amplitude decreases distortions occur and the p_{DC} decreases below one and p_{RMS} increases.

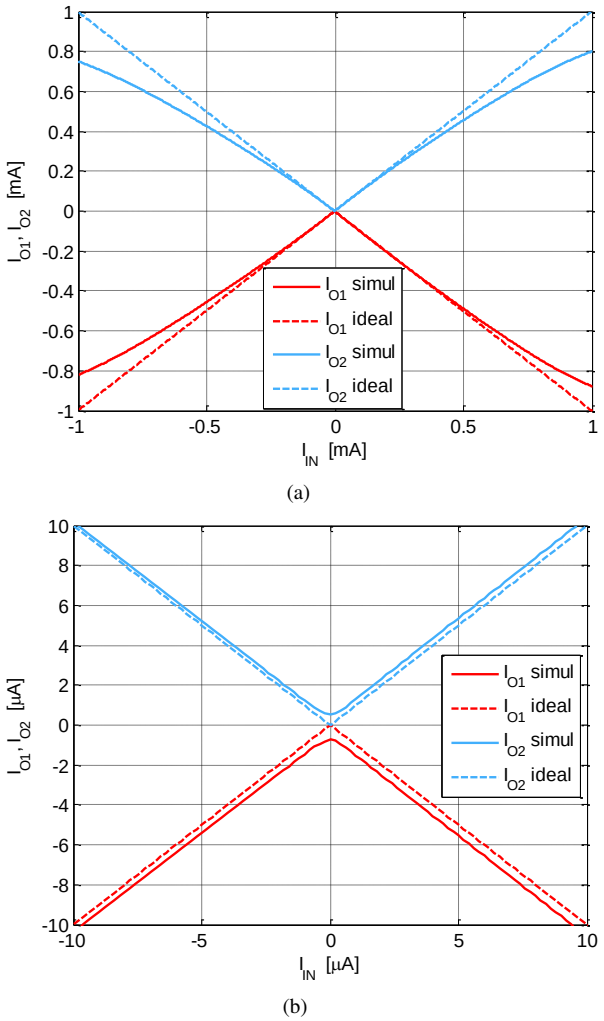

Fig. 3. Ideal and simulated (a) DC current transfers of the proposed current-mode rectifier, (b) zero crossing area, (I_{O1} red lines, I_{O2} blue lines).

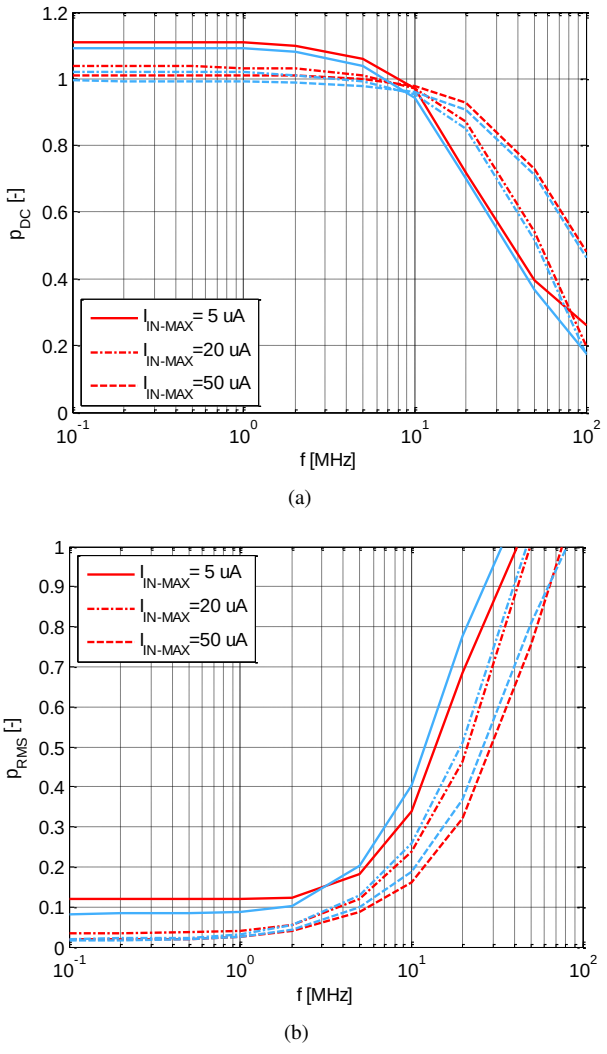

Fig. 4. (a) DC value transfers, (b) RMS errors for input signal amplitudes 5 μA, 20 μA, and 50 μA (I_{O1} red lines, I_{O2} blue lines).

Analyzing the DC transient value in Fig. 4a, for the input current signal of the magnitude 5 μA, 20 μA, and 50 μA correct DC values can be achieved up to the -3 dB cutoff frequency which is 15 MHz, 27 MHz, and 50 MHz, respectively. It is evident that for higher magnitudes of the input signal, the rectifier can be used at frequencies over 50 MHz, e.g. for input current with 100 μA magnitude the p_{DC} -3 dB cutoff frequency is 70 MHz. Note that because of the current offset for low frequencies the values of p_{DC} are higher than one.

The transient responses for frequencies 500 kHz, 1 MHz, and 5 MHz and input signal amplitude 20 μA are shown in Fig. 5. First at the frequency of 5 MHz a more significant distortion (mainly in the zero crossing area) can be observed, which is in agreement with the decreasing value of p_{DC} (Fig. 4a) and/or increasing value of p_{RMS} (Fig. 4b).

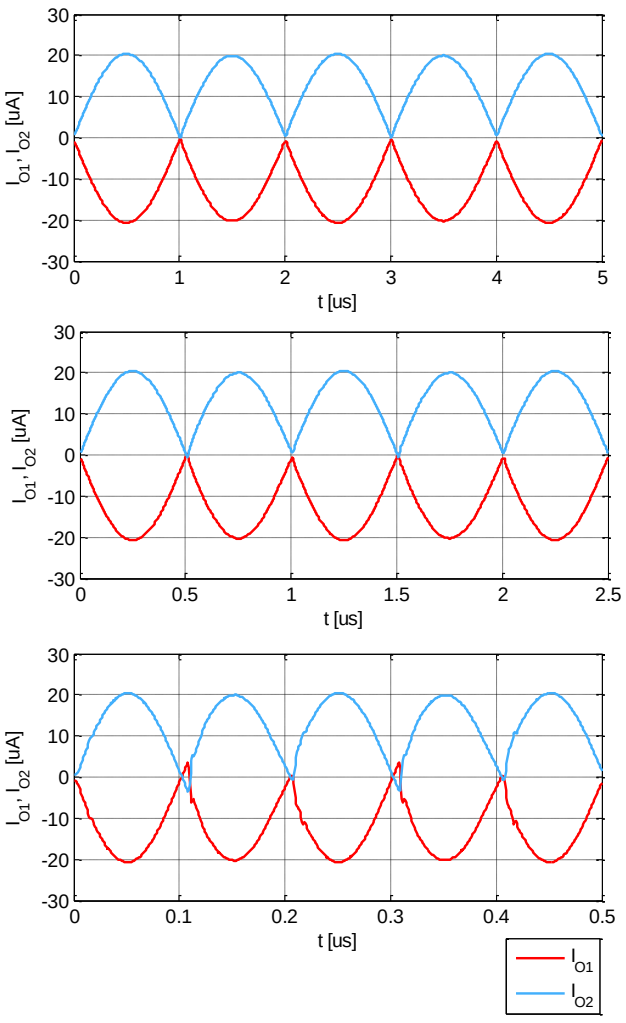

Fig. 5. Transient responses for frequencies 500 kHz, 1 MHz and 5 MHz and input signal amplitude 20 μA (I_{O1} red lines, I_{O2} blue lines).

4. Conclusion

In this paper we have presented current-mode precision rectifier using a two-cell winner-takes-all circuit. The input signal has still to be divided into both cells, however no 180° phase shift is required. A CMOS implementation of the precision rectifier has been proposed and using the the 0.35 μm TSMC CMOS technology further simulated. Based on the simulations the minimal amplitude of the input signal that can be rectified is 0.74 μA. Evaluating the DC value transfer p_{DC} and RMS error p_{RMS} the proposed circuit can be used to rectify signals of frequency up to 70 MHz if 5 % error in current gain of the rectifier is assumed, i.e. for input current magnitude of 100 μA. For higher input current magnitudes the error in gain increases, however, signals of frequency over 70 MHz can be rectified.

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