Supplementary First-Order All-Pass Filters with Two Grounded Passive Elements Using FDCCII

Bilgin METIN[1], *Norbert HERENCSAR*[2], *Kirat PAL*[3]

[1]Dept. of Management Information Systems, Bogazici University, Hisar Campus, 34342 Bebek-Istanbul, Turkey
[2]Dept. of Telecommunications, Brno University of Technology, Purkynova 118, 612 00 Brno, Czech Republic
[3]Dept. of Earthquake Engineering, Indian Institute of Technology, Roorkee, 247667, Uttaranchal, India

bilgin.metin@boun.edu.tr, herencsn@feec.vutbr.cz, kiratfeq@iitr.ernet.in

Abstract. *In this study, two novel first-order all-pass filters are proposed using only one grounded resistor and one grounded capacitor along with a fully differential current conveyor (FDCCII). There is no element-matching restriction. The presented all-pass filter circuits can be made electronically tunable due to the electronic resistors. Furthermore, the presented circuits enjoy high-input impedance for easy cascadability. The theoretical results are verified with SPICE simulations.*

Keywords

Analog filter, all-pass filter, cascadable filter, high-Q band-pass filter, grounded capacitor, FDCCII, MOSFET based resistors.

1. Introduction

In the literature different active elements [1] have been used in the design of voltage-mode (VM) all-pass filters [2]–[19] for different useful features, such as high input impedance, reduced number of active and passive elements or having grounded capacitors, etc. Some recent VM filter structures [13]–[19] emphasize the importance of the design with only grounded passive elements for easy integrated circuit (IC) implementation. Grounded IC capacitors have less parasitics compared to floating counterparts. Furthermore, the floating capacitors require an IC process with two poly layers. On the other hand, the grounded resistors can be replaced by MOS based electronic resistors [20] providing the advantages of less chip area and tunability. The electronically tunable circuits have been an important research area in the design of analog integrated circuits, because the tolerances of the electronic components in the IC realization can be very high and thus fine-tuning is necessary.

In [13], the VM all-pass section is designed by means of an operational transconductance amplifier (OTA), unity-gain differential amplifier, active voltage divider, and grounded capacitor. The VM circuits in [14] employ two resistors, two capacitors and two current conveyors. The VM circuits in [15], [16] use two differential difference current conveyors (DDCC) [21] and three grounded passive elements and they are cascadable. The circuit in [17] employs differential voltage conveyor (DVCC) [22] and two resistors. In [18], applications of the recently introduced analog building block (ABB) called voltage differencing differential input buffered amplifier (VD-DIBA) is presented. The proposed VM all-pass filter is composed of single VD-DIBA and one grounded capacitor. The circuits in [19] have a single fully differential current conveyor (FDCCII) [23] as active elements and two passive components.

In this study, in addition to the FDCCII based canonical and cascadable circuits of [19] in the literature, two supplementary cascadable VM first-order all-pass filters are presented. The proposed cascadable circuits employ only one grounded resistor and one capacitor and they have no element matching restriction compared to [14]–[16]. The introduced circuits consist of one fewer active element in comparison to [17]. Moreover, as an application example the proposed all-pass filters are used in the implementation of the high quality factor (high-Q) band-pass (BP) filter circuit [24]–[28] that is used frequently in the intermediate frequency stages of the receiver circuits [27]. Different from the circuits in [24]–[28], the presented high-Q band-pass filter example has a fine-tuning capability for its pole frequency and it consists of only grounded capacitors. The simulation results are used to verify the operation of the circuits.

2. FDCCII and Circuit Description

Fully differential current conveyor (FDCCII) is an eight-terminal ABB shown symbolically in Fig. 1. Conside-

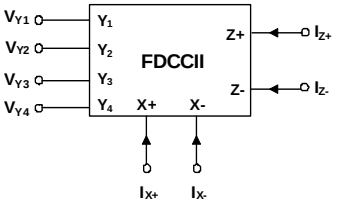


Fig. 1. The symbol of the FDCCII.

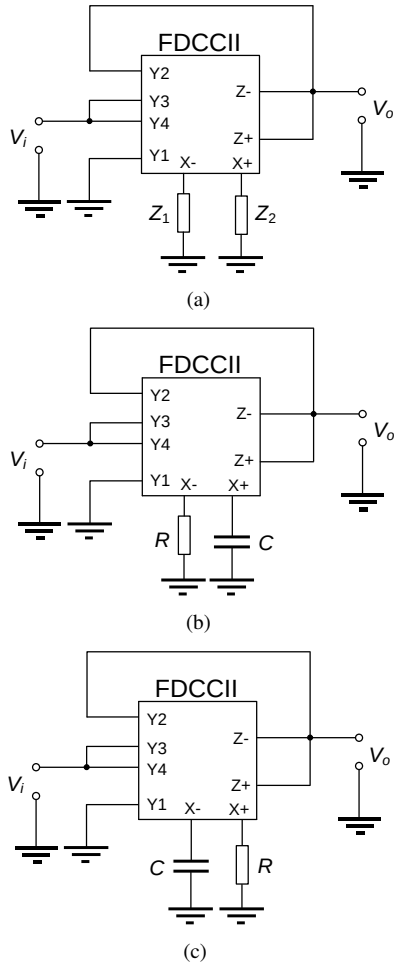


Fig. 2. (a) Presented general structure of VM all-pass filter, (b) first presented VM all-pass filter circuit, (c) second presented VM all-pass filter circuit.

ring the non-idealities caused by the physical implementation of the FDCCII [23], it is described with a matrix equation as follows:

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_1 & -\beta_2 & \beta_3 & 0 \\ 0 & 0 & -\beta_1 & \beta_2 & 0 & \beta_4 \\ \alpha_P & 0 & 0 & 0 & 0 & 0 \\ 0 & -\alpha_N & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \end{bmatrix} \tag{1}$$

where ideally $\beta_1 = \beta_2 = \beta_3 = \beta_4 = 1$ and $\alpha_P = \alpha_N = 1$ that represent the voltage and current transfer ratios of the FDCCII, respectively.

The transfer function of an all-pass filter can be given as follows:

$$\frac{V_o(s)}{V_i(s)} = K\frac{1-s\tau}{1+s\tau} \tag{2}$$

where K is the gain constant and its sign determines whether phase shifting is from 0 to π or from π to 0, and τ is the time constant. The proposed circuits are shown in Fig. 2. The general VM transfer function of the circuit in Fig. 2(a) is given for the ideal case ($\beta_1 = \beta_2 = \beta_3 = \beta_4 = 1$ and $\alpha_P = \alpha_N = 1$):

$$\frac{V_o}{V_i} = \frac{Z_1 - Z_2}{Z_1 + Z_2}. \tag{3}$$

Transfer function in (3) yields to two all-pass filter circuits under the specialization of Z_1 and Z_2 shown in Fig. 2(b) and 2(c). Their transfer function can be given as follows:

$$\frac{V_o}{V_i} = K\frac{-1+sCR}{1+sCR} \tag{4}$$

where $K = +1$ for $Z_1 = R$ and $Z_2 = 1/sC$ illustrated in Fig. 2(b) and where $K = -1$ for $Z_1 = 1/sC$ and $Z_2 = R$ illustrated in Fig. 2(c). Considering the active element non-idealities as given in (1), the transfer function for the circuit in Fig. 2(c) can be given as follows:

$$\frac{V_o}{V_i} = \frac{-\alpha_N\beta_4 + \alpha_P\beta_3 sCR}{(\alpha_N + \alpha_P sCR)\,\beta_2}. \tag{5}$$

The parasitic capacitances in the implementation of the active elements limit the high frequency operation. To evaluate high frequency performance, the frequency dependency of the current and voltage transfer ratios should be taken into account. Therefore, $\alpha(s)$ and $\beta(s)$ for FDCCII will be modeled with first-order functions for simplicity as:

$$\alpha_N(s) = \frac{\alpha_{N0}}{1+s\tau_N}, \quad \alpha_P(s) = \frac{\alpha_{P0}}{1+s\tau_P}, \quad \beta_k(s) = \frac{\beta_{k0}}{1+s\tau_{\beta k}}, \tag{6}$$

for $k = 1,2,3,4$ and where the α_{N0}, α_{P0}, and β_{k0} are the value of the current and voltage transfer ratios at low frequencies and $\omega_N = 1/\tau_N$, $\omega_P = 1/\tau_P$, and $\omega_\beta = 1/\tau_\beta$ represent their corresponding poles. Combining (5) and (6), the frequency dependent transfer function of the presented all-pass circuit in Fig. 2(c) can be obtained as follows:

$$\frac{V_o}{V_i} = \frac{(1+s\tau_{\beta2})\left[\begin{array}{c} -\alpha_{N0}\beta_{40}(1+s\tau_P)(1+s\tau_{\beta3}) + \\ +\alpha_{P0}\beta_{30}sCR(1+s\tau_N)(1+s\tau_{\beta4}) \end{array}\right]}{\beta_{20}\left[\begin{array}{c} \alpha_{N0}(1+s\tau_P) + \\ +\alpha_{P0}sCR(1+s\tau_N) \end{array}\right](1+s\tau_{\beta3})(1+s\tau_{\beta4})}. \tag{7}$$

Equation (7) shows that extra poles appear due to one-pole model additional to pole at $1/CR$. If the frequency of these additional poles are sufficiently higher than the pole of the presented all-pass filter such as $(CR)^{-1} \ll min\{\omega_{\beta3}, \omega_{\beta4}, \omega_{\alpha P}, \omega_{\alpha N}\}$, their effect on the frequency can be ignored.

3. Simulation Results

To verify theoretical results the proposed filter circuit shown in Fig. 2(c) is simulated by the SPICE simulation program. The FDCCII was realized based on the CMOS implementation in [23] (Fig. 3) and simulated using 0.35 μm, level 3 MOSFET parameters. The aspect ratios of the MOS transistors are given in Tab. 1. DC supply voltages of $\pm$1.3 V and V_{bp}, V_{bn} biasing voltages of 0 V are used. Biasing currents are chosen as 150 μA. The frequency response of the proposed circuit in Fig. 2(c) is given in Fig. 4(a) for

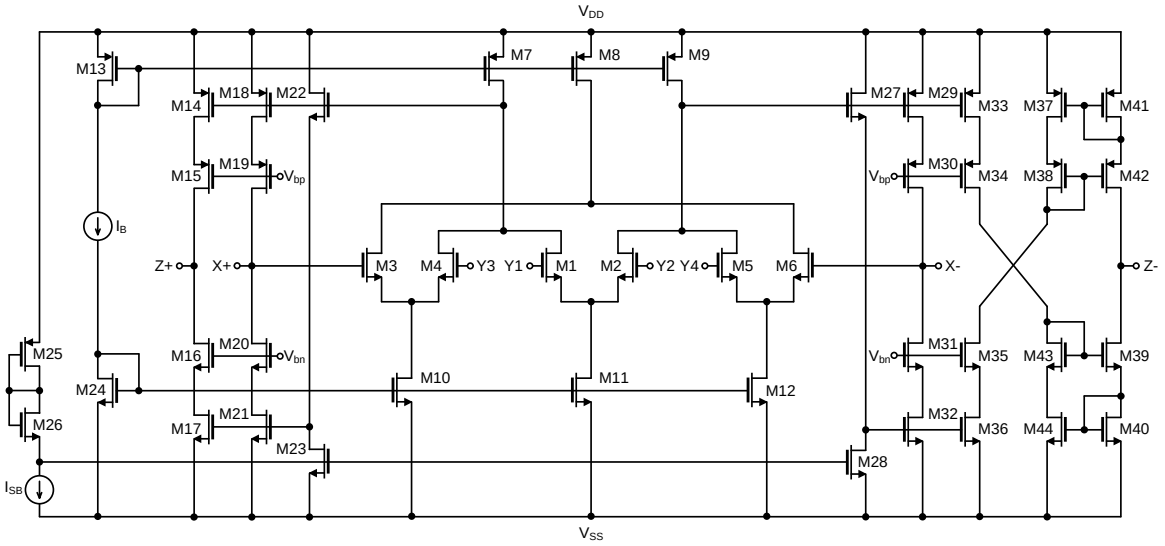


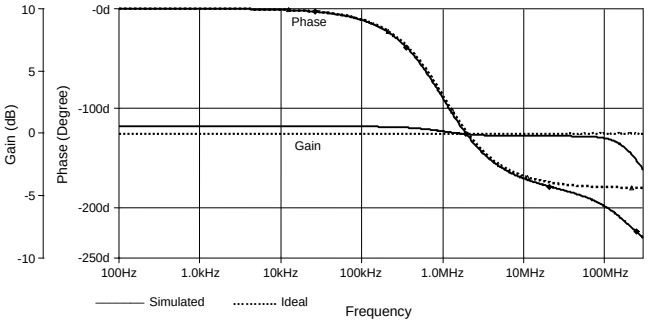
Fig. 3. CMOS FDCCII implementation based on [23].

$C = 100$ pF and $R = 1.5$ kΩ. The effects of the temperature on frequency response are examined for 10°C, 27°C, and 50°C in Fig. 4(b). The frequency response is slightly affected by the temperature. Time domain analysis of the proposed circuit in Fig. 2(c) for a 0.4 V peak-to-peak input signal at 100 kHz is given in Fig. 5 for passive element values of $C = 100$ pF and $R = 10$ kΩ. Total harmonic distortion at this frequency is found as 1.1 %. There is a 25 mV offset voltage at the output caused by the non-idealities of the FDCCII.

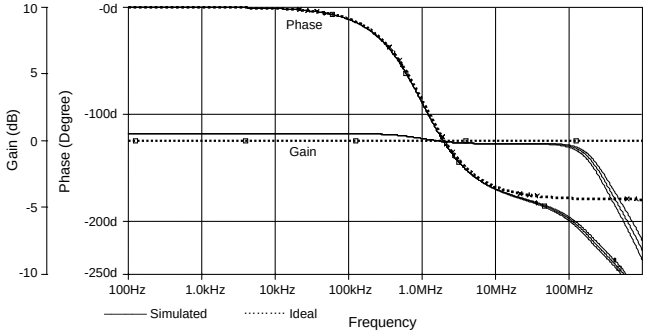
The presented all-pass filter is used to implement an electronically tunable high-Q band-pass (BP) filter application [24]–[28] as shown in Fig. 6. The quality factor of the band-pass filter is determined by R_A and R_B that is approximately equal to $Q \approx R_A/R_B$ [27]. In Fig. 6(a), the capacitor and resistor values are chosen as $C_1 = C_2 = 30$ pF, $R_1 = R_2 = 2$ kΩ, $R_A = 30$ kΩ, and $R_B = 1$ kΩ for a pole frequency of 2.65 MHz. Although the theoretical Q value is 30, in the simulations we have obtained $Q = 25$. The simulation results are given in Fig. 7. The center frequency of the BP filter circuit is found as 2.2 MHz in the simulation. Deviations from the ideal response result are caused by the non-idealities of the FDCCII used in the simulations. Fortunately, this deviation in the pole frequency can be corrected by fine tuning that can be achieved replacing grounded resistors with MOSFET based resistors [20] as shown in Fig. 6(b). The simulation results for the fine tuning of this circuit are illustrated in Fig. 8. The transistor aspect ratios for the MOSFET based electronic resistor in Fig. 6(b) are chosen as $(W/L)_{M1} = (W/L)_{M2} = 10.5\ \mu m/1.4\ \mu m$ and capacitor values are chosen as $C_1 = C_2 = 30$ pF. The pole frequency of the circuit is tuned between 3.14 MHz and 4.7 MHz by changing the control voltage V_C is changed between 0.8 V and 1.0 V. The parasitics and the non-idealities of the active elements cause change in the magnitude of the gains at the center frequency of the filter at high frequencies.

Transistors	W(μm)	L(μm)
M1-M6	4.4	0.35
M7-M9, M13-M15, M18, M19, M22, M23, M25, M27, M29, M30, M33, M34, M37, M38, M41, M42	35	0.35
M10-M12, M16, M17, M20, M21, M24, M26, M28, M31, M32, M35, M36, M39, M40, M43, M44	8.8	0.35

Tab. 1. Transistor aspect ratios.



(a)



(b)

Fig. 4. (a) Frequency response of the presented circuit, (b) the effect of the temperature change on the frequency response.

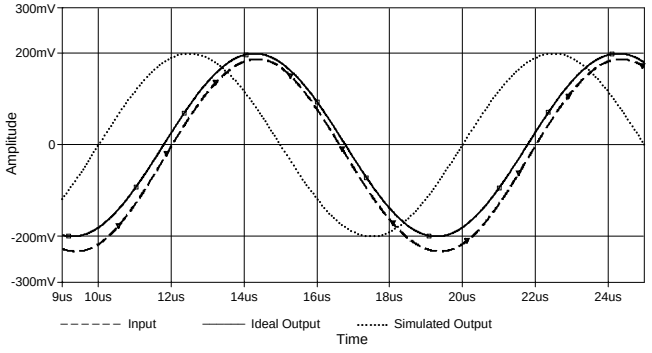


Fig. 5. Time domain analysis of the presented circuit.

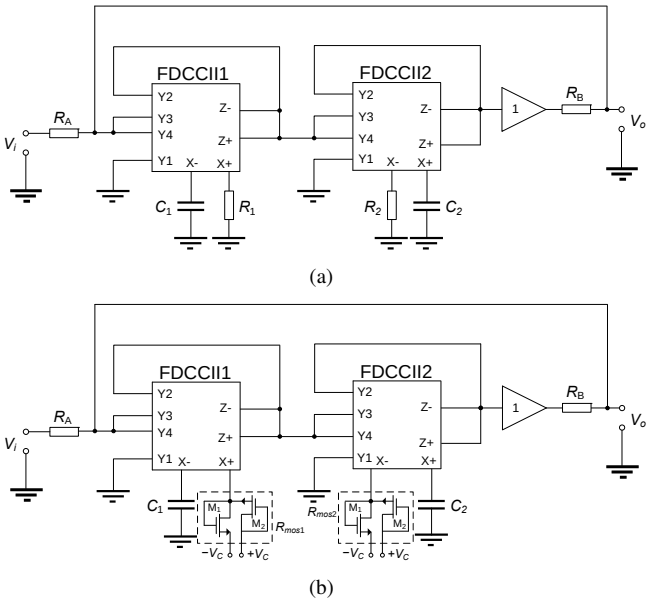


Fig. 6. (a) A high-Q band-pass filter example using presented all-pass filter, (b) electronically tunable form of the example band-pass filter.

4. Conclusion

In this study, two minimal first order all-pass filter realizations are given using only grounded passive elements. The proposed circuits have the advantage of having high input impedance for easy cascadability. The presented all-pass filter circuits are used in a tunable high-Q band-pass filter example. Simulations are performed to verify the theory.

Acknowledgements

This work was supported by Bogazici University Research Fund with the project code 08N304, Czech Ministry of Education under research program MSM 0021630513, and GACR projects under No. P102/11/P489 and P102/09/1681. Authors also wish to thank the reviewers for their useful and constructive comments.

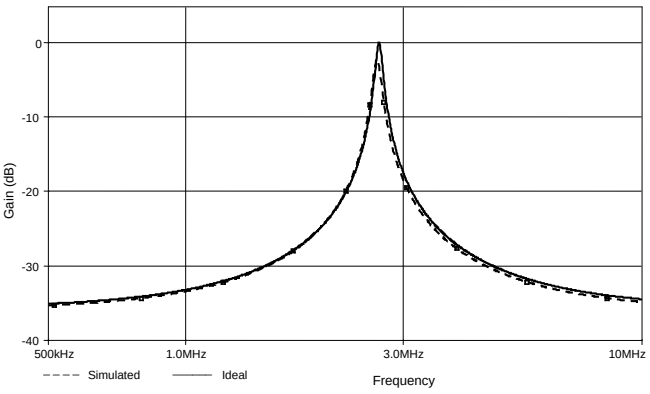


Fig. 7. Frequency response of the high-Q band-pass filter example.

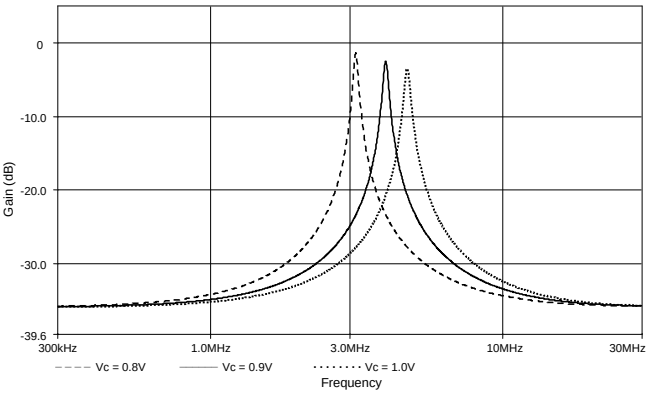


Fig. 8. Illustrating fine-tuning of the pole-frequency for the high-Q band-pass filter example.

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About Authors...

Bilgin METIN received the B.Sc. degree in Electronics and Communication Engineering from Istanbul Technical University, Istanbul, Turkey in 1996 and the M.Sc. and Ph.D. degrees in Electrical and Electronics Engineering from Bogazici University, Istanbul, Turkey in 2001 and 2007, respectively. He is currently an Assistant Professor in the Management Information Systems Department, Bogazici University. His research interests include continuous time filters, analog signal processing applications, current-mode circuits, computer networks, and network security. He was given the best student paper award of ELECO'2002 conference in Turkey. Dr. Metin has over 30 publications in scientific journals or conference proceedings.

Norbert HERENCSAR received the M.Sc. and Ph.D. degrees in Electronics & Communication and Teleinformatics from Brno University of Technology, Czech Republic, in 2006 and 2010, respectively. Currently, he is an Assistant Professor at the Dept. of Telecommunications, Brno University of Technology, Brno, Czech Republic. From September 2009 through February 2010 he was an Erasmus Exchange Student with the Dept. of Electrical and Electronic Engineering, Bogazici University, Istanbul, Turkey. His research interests include analog filters, current-mode circuits, tunable frequency filter design methods, and oscillators. He is an author or co-author of about 67 research articles published in international journals or conference proceedings. Since 2008, Dr. Herencsar serves in the organizing and technical committee of the Int. Conf. on Telecommunications and Signal Processing (TSP). In 2011 and 2012, he is guest co-editor of TSP 2010 and TSP 2011 Special Issues on Signal Processing, published in the Radioengineering journal. Dr. Herencsar is Senior Member of the IACSIT and Member of the IAENG and ACEEE.

Kirat PAL was born in Aligarh, India on 20th August 1950. He received the B.Sc & M.Sc degree from the Aligarh Muslim University in 1972 and 1977 respectively and the Ph.D. degree from the University of Roorkee (Presently Indian Institute of Technology, Roorkee) in 1982. He joined University of Roorkee as a scientific officer in 1979 and worked in various capacities as lecturer, reader and at present holds the post of Associate Professor in Earthquake Engineering Dept. of Indian Institute of Technology Roorkee. His main research interests are analog circuits and signal processing, transducers, seismological instrumentation and digital image processing. Dr. Pal has authored more than 100 research papers in the above areas in national, international journals and conferences.