Single ICCII Sinusoidal Oscillators Employing Grounded Capacitors

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Abstract. *Two inverting second-generation current conveyors (ICCII) based sinusoidal oscillators are presented. The first sinusoidal oscillator is composed of one ICCII, two grounded capacitors and two resistors. The oscillation condition and oscillation frequency can be orthogonally controllable. The second sinusoidal oscillator is composed of one ICCII, two grounded capacitors and three resistors. The oscillation condition and oscillation frequency can be independently controllable through different resistors.*

Keywords

Sinusoidal oscillator, current conveyor, active circuit.

1. Introduction

Over the past few years, a number of schemes based on second-generation current conveyors (CCIIs) have been developed to realize sinusoidal oscillators with grounded capacitors [1]-[7]. In 1986, Nandi proposed six sinusoidal oscillator circuits by using two plus-type CCIIs, two capacitors and two (or three) resistors [1]. In 1995, Abuelma'atti et al. proposed an oscillator configuration by using two minus-type CCII, three (or four) resistors and three (or four) capacitors [2]. In 1997, Horng et al. proposed four sinusoidal oscillator circuits by using one plus-type CCII, one minus-type CCII, two capacitors and two resistors [3]. In 2001, Horng proposed a sinusoidal oscillator circuit by using two plus-type CCIIs, two capacitors and two resistors [4]. In 2007, Horng et al. proposed two sinusoidal oscillator circuits by using two CCIIs, two capacitors and two (or three) resistors [5]. Soliman proposed several grounded capacitors oscillators using two (or three) CCIIs that were derived out from Wien-type oscillator or two-integrated loop oscillator [6], [7]. However, at least two active components are required in these circuit configurations.

Several single active building block sinusoidal oscillators were presented [8], [9]. However, these sinusoidal oscillators do not have all capacitors grounded. The oscillator circuit at Fig. 3 (c) of Toker at al. [10] uses one inverting second-generation current conveyor (ICCII), three resistors and three grounded capacitors. However, the capacitors it used are not minimum. The oscillator circuit at circuit 3 of Lahiri [11] uses one ICCII, two resistors and three grounded capacitors. However, the capacitor C_4 is connected to the x terminal of ICCII. Because the ICCII has a non-negligible output parasitic resistance on port x (R_x), when the x port of ICCII is loaded by a capacitor, it leads to an improper transfer functions. Due to the effect of this parasitic resistance R_x at the x port of ICCII, the oscillators with x port loaded by a capacitor do not exhibit good performance at high frequency. In 2007, Kumar and Senani proposed a sinusoidal oscillator by using one positive four terminal floating nullor (PFTFN), five resistors and two grounded capacitors [12]. However, the resistors it used are not minimum. In 2000, Gupta and Senani proposed a sinusoidal oscillator circuit by using one differential voltage current conveyor (DVCC), two grounded capacitors and three resistors [13].

ICCII was proposed by Awad and Soliman [14] and has been found useful in many applications [15]-[18]. In this paper, two sinusoidal oscillators based on ICCII are presented. The first proposed oscillator is composed of one ICCII, two grounded capacitors and two resistors. The oscillation condition and oscillation frequency can be orthogonally controllable. The second proposed oscillator is composed of one ICCII, two grounded capacitors and three resistors. The oscillation condition and oscillation frequency can be independently controllable through different resistors. Moreover, the proposed circuits use only grounded capacitor. The use of grounded capacitors is particularly attractive for integrated circuit implementation [19].

2. ICCIIs Based Oscillators

Using standard notation, the port relations of a ICCII can be characterized by $v_x = -v_y$, $i_z = \pm i_x$ and $i_y = 0$. The first proposed configuration is shown in Fig. 1. The characteristic equation of the circuit can be expressed as

$$s^2 C_1 C_2 R_1 R_2 + sR_1(2C_1 - C_2) + 2 = 0. \quad (1)$$

The oscillation condition and oscillation frequency can be obtained as

$$C_1 = 0.5C_2, \tag{2}$$

$$\omega_o = \sqrt{\frac{2}{C_1 C_2 R_1 R_2}}. \tag{3}$$

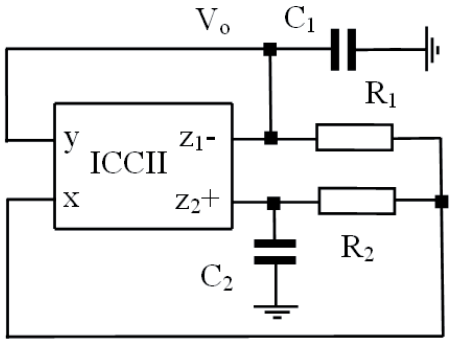

Fig. 1. The first proposed ICCII based sinusoidal oscillator.

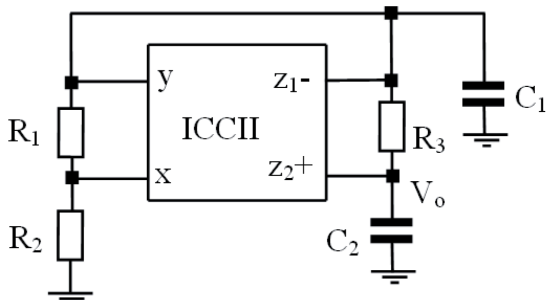

Fig. 2. The second proposed ICCII based sinusoidal oscillator.

The oscillation condition of Fig. 1 can be adjusted by grounded capacitor C_1 or/and C_2. The oscillation frequency can be adjusted by the resistor R_1 or R_2.

The second proposed configuration is shown in Fig. 2. The characteristic equation of the circuit can be expressed as

$$s^2 C_1 C_2 R_1 R_2 R_3 + sR_1(C_1 R_2 + C_2 R_2 - C_2 R_3) + 2R_2 = 0. \tag{4}$$

The oscillation condition and oscillation frequency can be obtained as

$$R_2 = \frac{C_2 R_3}{C_1 + C_2}, \tag{5}$$

$$\omega_o = \sqrt{\frac{2}{C_1 C_2 R_1 R_3}}. \tag{6}$$

The oscillation condition can be adjusted by the grounded resistor R_2. The oscillation frequency can be independently adjusted by the resistor R_1. Note that Fig. 1 and Fig. 2 employ only grounded capacitors. The use of grounded capacitors is particularly attractive for integrated circuit implementation [19]. It may be pointed out that the completely CMOS-based sinusoidal oscillators can be realized using the proposed circuits by replacing all resistors in Figs. 1 and 2 by CMOS floating resistors such as that given in [20]. Because the oscillation condition and oscillation frequency of Fig. 2 can be independently adjusted by different resistors, this circuit can be made voltage controllable by replacing the resistors by CMOS floating resistors.

Taking into account the non-ideal ICCII, namely, $i_z = \pm\alpha_i i_x$, $v_x = -\beta v_y$, where $\alpha_i = 1 - \varepsilon_{i1}$ and ε_{i1} ($|\varepsilon_{i1}| << 1$) denotes the current tracking error and $\beta = 1 - \varepsilon_2$ and ε_2 ($|\varepsilon_2| << 1$) denotes the voltage tracking error of a ICCII. The modified oscillation condition and oscillation frequency of Fig. 1 are

$$C_1 = \frac{C_2 R_1 \alpha_1 \beta + C_2 R_2 (\alpha_1 - 1)(1+\beta)}{R_1(1+\alpha_2)}, \tag{7}$$

$$\omega_o = \sqrt{\frac{\alpha_1 \alpha_2 (1+\beta) + (1-\alpha_1)(1+\alpha_2)(1+\beta)}{C_1 C_2 R_1 R_2}}. \tag{8}$$

The active and passive sensitivities of this sinusoidal oscillator are all low and obtained as

$$S^{\omega_o}_{C_1, C_2, R_1, R_2} = -\frac{1}{2};\ S^{\omega_o}_{\alpha_1} \cong -\frac{1}{2};\ S^{\omega_o}_{\alpha_2} \cong \frac{1}{2};\ S^{\omega_o}_{\beta} \cong \frac{1}{4}.$$

These values have been calculated using (8) by assuming that α_i and β are near to unity.

Taking into account the non-ideal ICCII in Fig. 2, the modified oscillation condition and oscillation frequency are

$$R_2 = \frac{C_2 R_1 R_3 \alpha_1 \beta}{C_1 R_1 + C_2 R_1 + C_2 R_3 (1-\alpha_1)(1+\beta)}, \tag{9}$$

$$\omega_o = \sqrt{\frac{R_2(1+\alpha_2-\alpha_1)(1+\beta) + R_1(\alpha_2-\alpha_1)\beta}{C_1 C_2 R_1 R_2 R_3}}. \tag{10}$$

The active and passive sensitivities are obtained as

$$S^{\omega_o}_{C_1, C_2, R_3} = -\frac{1}{2};\ S^{\omega_o}_{R_1} \cong -\frac{1}{2};\ S^{\omega_o}_{R_2} \cong 0;$$

$$S^{\omega_o}_{\alpha_1} \cong -\frac{1}{2} - \frac{R_1}{4R_2};\ S^{\omega_o}_{\alpha_2} \cong \frac{1}{2} + \frac{R_1}{4R_2};\ S^{\omega_o}_{\beta} \cong \frac{1}{4}$$

These values have been calculated using (10) by assuming that α_i and β are near to unity.

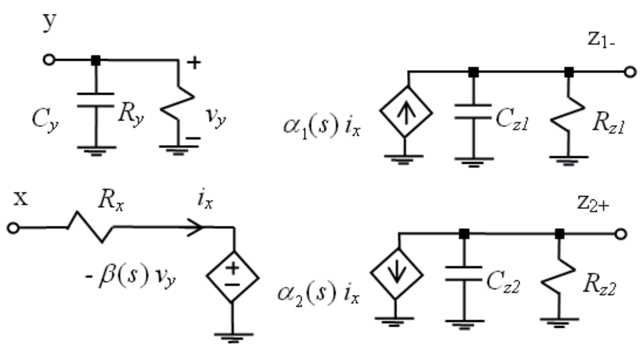

Fig. 3. The non-ideal ICCII model.

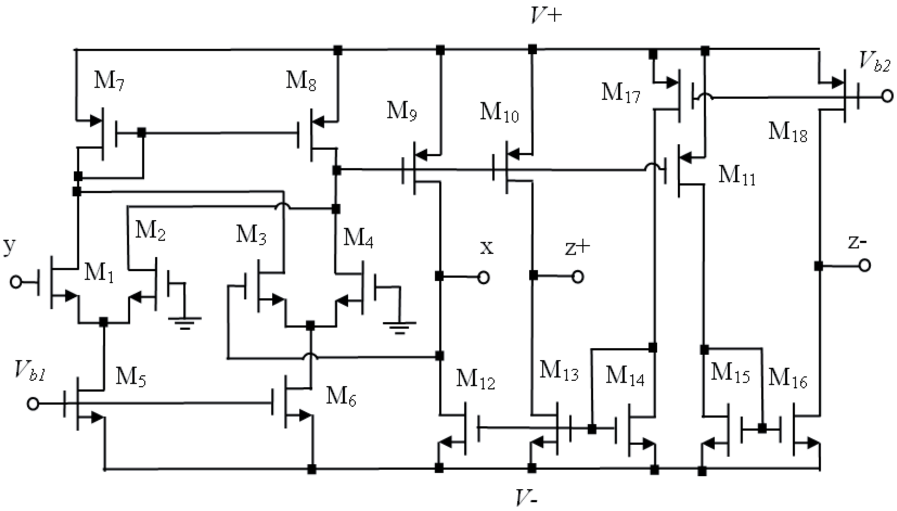

Fig. 4. CMOS realization of the ICCII [22].

3. Influence of the ICCII Parasitic Elements on the Proposed Circuits

A non-ideal ICCII model is shown in Fig. 3 [21]. It is shown that the real ICCII has parasitic resistors and capacitors from the y and z terminals to the ground, and also, a series resistor at the input terminal x. Taking into account the non-ideal ICCII in Fig. 1 and assuming the circuit is working at frequencies much lower than the corner frequencies of $\alpha_i(s)$ and $\beta(s)$, namely, $\alpha_i \cong \beta \cong 1$, the characteristic equation of Fig. 1 becomes

$$\begin{aligned}
&s^2 C_1'C_2'(G_1+G_2+G_x) \\
&+ s(2C_1'G_2G_x - C_2'G_2G_x + C_1'G_1G_2 + C_1'G_1G_{z2} + C_1'G_2G_{z2} \\
&+ C_1'G_{z2}G_x + C_2'G_1G_3 + C_2'G_1G_2 + C_2'G_2G_3 + C_2'G_3G_x) \\
&+ 2G_1G_2G_x + 2G_2G_3G_x + G_1G_2G_3 + G_1G_3G_{z2} \\
&+ G_1G_2G_{z2} + G_3G_{z2}G_x + G_2G_3G_{z2} - G_2G_{z2}G_x = 0
\end{aligned} \quad (11)$$

where

$C_1' = C_1 + C_y + C_{z1}$, $C_2' = C_2 + C_{z2}$, $G_3 = G_y + G_{z1}$.

Taking into account the non-ideal ICCII model of Fig. 3 in Fig. 2 and assuming the circuit is working at frequencies much lower than the corner frequencies of $\alpha_i(s)$ and $\beta(s)$, the characteristic equation of Fig. 2 becomes

$$\begin{aligned}
&s^2 C_1'C_2'(G_1+G_2+G_x) \\
&+ s(C_1'G_3G_x + C_2'G_3G_x - C_2'G_2G_x + C_1'G_1G_3 + C_1'G_2G_3 \\
&+ C_1'G_1G_{z2} + C_1'G_2G_{z2} + C_1'G_{z2}G_x + C_2'G_1G_2 + C_2'G_1G_3 \\
&+ C_2'G_2G_3 + C_2'G_1G_4 + C_2'G_2G_4 + C_2'G_4G_x) \\
&+ 2G_1G_3G_x + G_1G_2G_3 + G_1G_2G_{z2} + G_1G_3G_{z2} + G_2G_3G_{z2} \\
&+ G_3G_{z2}G_x + G_1G_3G_4 + G_2G_3G_4 + G_3G_4G_x + G_1G_4G_{z2} \\
&+ G_2G_4G_{z2} + G_4G_{z2}G_x - G_2G_{z2}G_x = 0
\end{aligned} \quad (12)$$

where

$C_1' = C_1 + C_y + C_{z1}$, $C_2' = C_2 + C_{z2}$, $G_4 = G_y + G_{z1}$.

From the characteristic equations (11) and (12), the oscillation conditions and oscillation frequencies of the proposed sinusoidal oscillators in Figs. 1 and 2 are coupled due to the parasitic impedances, especially because R_x is not zero. To minimize the effects of the ICCIIs' non-idealities, the ICCII realization with minimum parasitic R_x resistance will be welcome for the realization of the proposed sinusoidal oscillators.

4. Simulation Results

To verify the theoretical prediction of the proposed circuits, Fig. 1 and Fig. 2 were simulated using HSPICE. The ICCII was realized by the CMOS implementation in Fig. 4 [22] whereas the aspect ratios of the NMOS and PMOS transistors are given in Tab. 1 using 0.18μm, level 49 MOSFET from TSMC. The power supply was ±1.25 V. The bias voltages are V_{b1} = -0.4 V and V_{b2} = 0.3 V.

Fig. 5 shows a simulated output waveform of Fig. 1 with C_1 = 15 pF, C_2 = 35 pF, R_1 = 5 kΩ, R_2 = 20 kΩ. The results of the V_o total harmonic distortion analysis are summarized in Tab. 2. Fig. 6 shows the simulation results of the oscillation frequencies of Fig. 1 by varying the value of the resistor R_1 with C_1 = 15 pF, C_2 = 35 pF and R_2 = 20 kΩ.

MOS transistors	W/L
M1~M4	24.84/0.54
M5, M6	8.1/0.54
M7, M8	10.26/0.54
M9~M11, M17, M18	39.6/1.98
M12~M16	20.16/2.52

Tab. 1. Aspect ratios of the MOSs in Fig. 3.

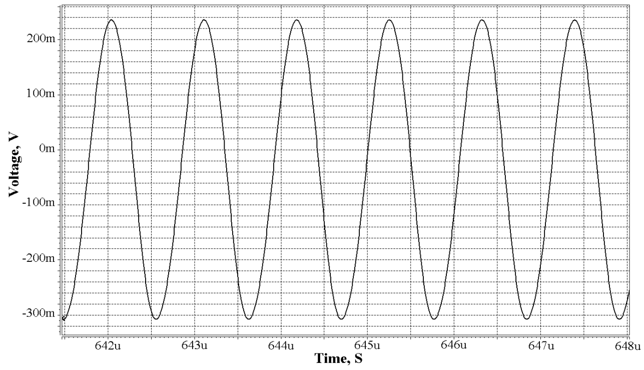

Fig. 5. Simulated output waveform of Fig. 1 with C_1 = 15 pF, C_2 = 35 pF, R_1 = 5 kΩ, R_2 = 20 kΩ.

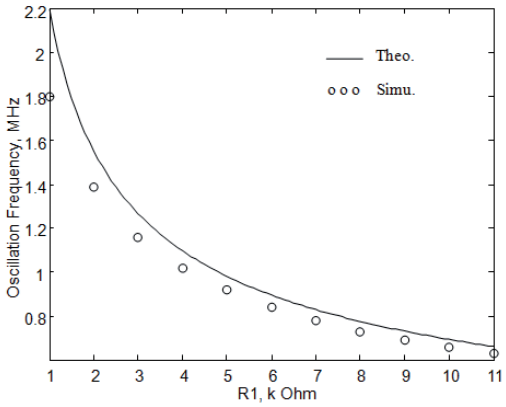

Fig. 6. Simulation results of the oscillation frequency of Fig. 1 by varying the value of the resistor R_1.

Harmonic no	Frequency(hz)	Fourier component	Phase(deg)
1	930.0000k	272.6247m	-150.62
2	1.8600x	6.3494m	-95.7539
3	2.7900x	1.5168m	-143.3834
4	3.7200x	504.8469u	60.5579
5	4.6500x	515.4810u	33.7076
6	5.5800x	333.5851u	9.7892
7	6.5100x	310.8758u	9.3744
8	7.4400x	280.7707u	10.6645
9	8.3700x	248.5830u	7.4949
dc component = -3.808D-02			
total harmonic distortion = 2.4188 percent			

Tab. 2. Total harmonic distortion analysis of V_o in Fig. 1 with C_1 = 15 pF, C_2 = 35 pF, R_1 = 5 kΩ, R_2 = 20 kΩ.

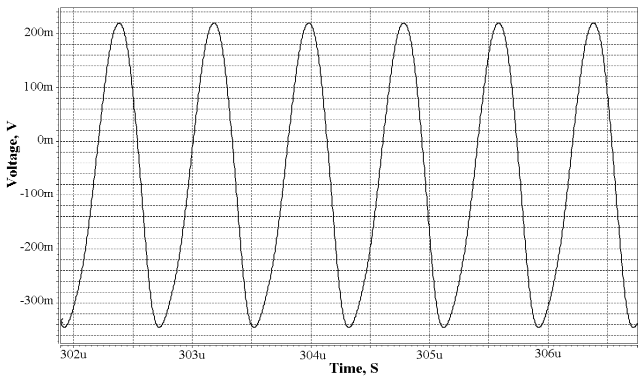

Fig. 7. Simulated output waveform of Fig. 1 with C_1 = 25 pF, C_2 = 55 pF, R_1 = 10 kΩ, R_2 = 5 kΩ.

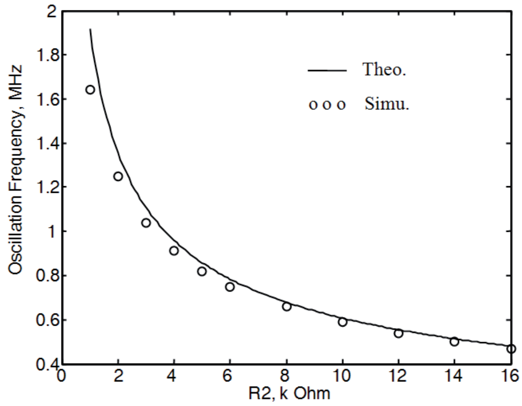

Fig. 8. Simulation results of the oscillation frequency of Fig. 1 by varying the value of the resistor R_2.

Fig. 7 shows a simulated output waveform of Fig. 1 with C_1 = 25 pF, C_2 = 55 pF, R_1 = 10 kΩ, R_2 = 5 kΩ. The results of the V_o total harmonic distortion analysis are summarized in Tab. 3. Fig. 8 shows the simulation results of the oscillation frequencies of Fig. 1 by varying the value of the resistor R_2 with C_1 = 25 pF, C_2 = 55 pF and R_1 = 10 kΩ.

Harmonic no	Frequency(hz)	Fourier component	Phase(deg)
1	820.0000k	250.2235m	16.5002
2	1.6400x	14.2835m	-126.6692
3	2.4600x	4.1816m	-6.4886
4	3.2800x	1.2418m	116.0461
5	4.1000x	345.6755u	-112.3604
6	4.9200x	131.6986u	117.4447
7	5.7400x	115.0711u	-146.7783
8	6.5600x	10.3602u	162.6544
9	7.3800x	48.6834u	-173.6039
dc component = -7.028D-02			
total harmonic distortion = 5.9706 percent			

Tab. 3. Total harmonic distortion analysis of V_o in Fig. 1 with C_1 = 25 pF, C_2 = 55 pF, R_1 = 10 kΩ, R_2 = 5 kΩ.

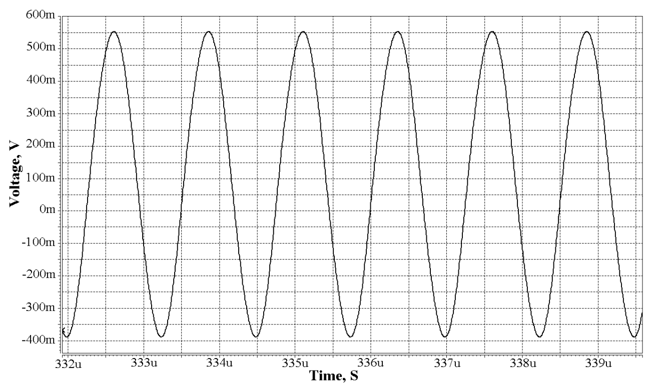

Fig. 9. Simulated output waveform of Fig. 2 with C_1 = 30 pF, C_2 = 40 pF, R_1 = 6 kΩ, R_2 = 5 kΩ and R_3 = 10 kΩ.

Fig. 9 shows a simulated output waveform of Fig. 2 with C_1 = 30 pF, C_2 = 40 pF, R_1 = 6 kΩ, R_2 = 5 kΩ and R_3 = 10 kΩ. The results of the V_o total harmonic distortion analysis are summarized in Tab. 4. Fig. 10 shows the simulation results of the oscillation frequencies of Fig. 2 by varying the value of the resistor R_1 with C_1 = 30 pF, C_2 = 40 pF, R_2 = 5 kΩ and R_3 = 10 kΩ. Comparisons of some recently reported grounded capacitors single active element oscillators are given in Tab. 5. Tab. 5 shows the features of the proposed circuits in the number of passive components used and operation frequency range reported.

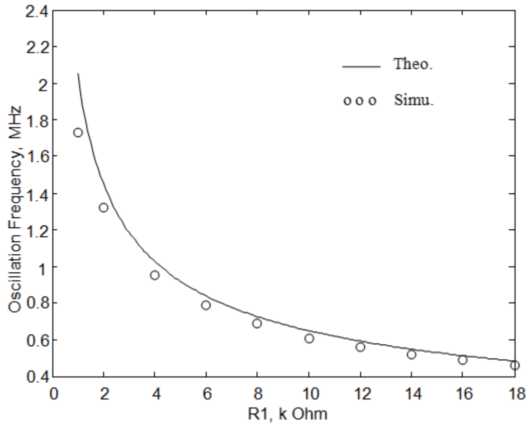

Fig. 10. Simulation results of the oscillation frequency of Fig. 2 by varying the value of the resistor R_1.

Harmonic no	Frequency(hz)	Fourier component	Phase(deg)
1	800.0000k	470.3956m	-100.9317
2	1.6000x	8.0197m	-119.3672
3	2.4000x	6.6175m	147.9938
4	3.2000x	703.3381u	57.5282
5	4.0000x	697.5248u	-78.5406
6	4.8000x	99.4012u	-80.8514
7	5.6000x	47.2812u	64.9175
8	6.4000x	65.1539u	45.9413
9	7.2000x	38.8709u	541.8767m
dc component = 8.968D-02			
total harmonic distortion = 2.2206 percent			

Tab. 4. Total harmonic distortion analysis of V_o in Fig. 2.

	Number of resistors	Number of capacitors	Frequency range reported	Process or experiment	THD (%)
[13]	3	2	0.4MHz	MOSIS 1.2 μ m	-
[10], Fig. 3(c)	3	3	Has not given	-	-
[12]	5	2	0.016MHz	Experiment	-
[11], circuit 3	2	3	0.16MHz	Has not given	-
Proposed Fig. 1	2	2	1.8MHz	TSMC 0.18 μ m	2.4188
Proposed Fig. 2	3	2	1.73MHz	TSMC 0.18 μ m	2.2206

Tab. 5. Comparisons of some reported grounded capacitors single active element oscillators.

5. Conclusion

In this paper, two new ICCII based sinusoidal oscillators have been presented. The first proposed circuit employs one ICCII, two grounded capacitors and two resistors. The oscillation condition and oscillation frequency can be orthogonally controllable. The second proposed employs one ICCII, two grounded capacitors and three resistors. The oscillation condition and oscillation frequency can be independently controllable. The proposed circuits use only grounded capacitors that are attractive for integrated circuit implementation. Each of the proposed circuits uses only one active device (one ICCII) that simplifies the circuit configuration.

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