CFOA-Based Lossless and Lossy Inductance Simulators

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Abstract. *Inductance simulator is a useful component in the circuit synthesis theory especially for analog signal processing applications such as filter, chaotic oscillator design, analog phase shifters and cancellation of parasitic element. In this study, new four inductance simulator topologies employing a single current feedback operational amplifier are presented. The presented topologies require few passive components. The first topology is intended for negative inductance simulation, the second topology is for lossy series inductance, the third one is for negative lossy parallel inductance (-R) (-L) and the fourth topology is for negative parallel (-R) (-L) (-C) simulation. The performance of the proposed CFOA based inductance simulators is demonstrated on both a second-order low-pass filter and inductance cancellation circuit. PSPICE simulations are given to verify the theoretical analysis.*

Keywords

CFOA, filters, inductance simulators.

1. Introduction

The current feedback operational amplifier and current-conveyor integrated circuits have been given great importance, because these circuits have several advantages like greater linearity and wider bandwidth over the conventional voltage mode operational amplifiers.

Actively simulated grounded inductors have been found in several applications ranging from filter to oscillator design to cancellation of parasitic inductances. There are several publications on the realization of inductance simulators using high performance active building blocks such as operational transconductance amplifiers (OTA), second generation current conveyors (CCII), current-feedback op-amps (CFOA), four terminal floating nullors (FTFN), differential voltage current conveyor (DVCC), current differencing buffer amplifer (CDBA), operational transresistance amplifier (OTRA), dual-X current conveyors (DXCCII), fully differential current conveyors (FDCCII), etc. [1] – [24]. In [16], two active elements, one dual-output second-generation current-controlled current conveyor (DO-CCCII) and one operational amplifier (Op-Amp) are used. The circuit of [17] uses six current conveyors and five passive elements. Three CCII+s and two external resistors are used in [18]. The circuit of [19] employs three current differencing buffered amplifiers (CDBAs) and three MOS resistors. The circuit of [20], [21] provides a negative inductance simulator.

In this paper four inductance simulator topologies employing a single CFOA and a various number of passive elements are presented. The first topology is intended for negative inductance simulation, the second topology is for lossy series inductance, the third one is for negative lossy parallel inductance (-R) (-L) and the fourth topology is for negative parallel (-R) (-L) (-C) simulation. Finally, a second-order low-pass filter and inductance cancellation circuit are constructed using the proposed series inductance and negative inductance simulator. Simulation results are included to verify the theory.

2. Proposed Circuits

The current feedback operational amplifier symbol is shown in Fig. 1. This element is constructed by using the second generation current conveyor and voltage buffer.

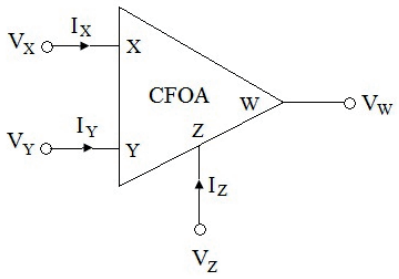

Fig. 1. Circuit symbol of current feedback operational amplifier.

The current-voltage terminal characteristic of an ideal CFOA can be modeled as

$$\begin{bmatrix} I_y \\ I_z \\ V_x \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix}. \tag{1}$$

Deviations from the ideal characteristics will affect the performance of the circuits realized with CFOA. Taking the current and voltage tracking errors into account, the current- voltage terminal characteristic of the non-ideal CFOA becomes

Circuit	Z_{eq}	L_{eq}	G_{eq}	C_{eq}	Type
Fig. 2(a)	$Z_{eq} = -\frac{sC}{2G_1G_2}$	$L_{eq} = -\frac{C}{2G_1G_2}$	–	–	Pure -L
Fig. 2(b)	$Z_{eq} = \frac{sC + G_1 + G_2}{G_1G_2}$	$L_{eq} = \frac{C}{G_1G_2}$	$G_{eq} = G_1 + G_2$	–	L with series R
Fig. 2(c)	$Z_{eq} = -\frac{sC}{sCG_2 + G_1G_2}$	$L_{eq} = -\frac{C}{G_1G_2}$	$G_{eq} = -G_2$	–	-L with parallel -R
Fig. 2(d)	$Z_{eq} = -\frac{sC_1}{G_1G_2 + s^2C_1C_2 + sC_1G_2 + sC_2G_1}$	$L_{eq} = -\frac{C_1}{G_1G_2}$	$G_{eq} = -\left(\frac{C_1G_2 + C_2G_1}{C_1}\right)$	$-C_2$	-L and -C parallel with -R

Tab. 1. Actively realizable inductance forms.

Circuit	Matching	Z_{eq}
Fig. 2 (a)	No	$Z_{eq} = -\frac{sC\alpha\beta\gamma}{G_1(1+\alpha)(G_2 + sC(1-\beta\gamma))}$
Fig. 2 (b)	No	$Z_{eq} = \frac{sC\alpha\gamma + G_1 + G_2}{G_1(G_2 + sC\alpha(-\beta + \gamma))}$
Fig. 2 (c)	No	$Z_{eq} = -\frac{sC}{sC(-1+\gamma)G_1 + sC\alpha\beta G_2 + \alpha\beta\gamma G_1G_2}$
Fig.2 (d)	No	$Z_{eq} = -\frac{sC_1}{G_1G_2\alpha\beta\gamma + s^2C_1C_2\alpha\beta + sC_1(G_2\alpha\beta + G_1(-1+\gamma)) + sC_2G_1\alpha\beta\gamma}$

Tab.2. CFOA-based grounded inductance circuits for the non-ideal case.

$$\begin{bmatrix} I_y \\ I_z \\ V_x \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \alpha & 0 & 0 \\ 0 & \beta & 0 \\ 0 & 0 & \gamma \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix} \tag{2}$$

where α, β and γ are the non-ideal current and voltage gains.

The proposed circuits are shown in Fig. 2. Routine analysis of these circuits yields the relations for the input impedances, equivalent inductances and equivalent resistances, illustrated in Tab. 1. The circuits illustrated in Fig. 2(b) can simulate series (+L) with (+R). The circuit of Fig. 2(c) simulates parallel (-L) with (-R). The last circuit in Fig. 2(d) simulates parallel (-L), (-C) and (-R). Besides the positive inductance simulator circuits, which can be considered as useful topologies for a circuit designer, the negative inductance simulators are also important. It can be found in many applications such as active filter design, oscillator design, and analog phase shifters, to minimize reflection at the input of antenna, to compensate bond wire inductance and cancellation of undesirable inductance. Impedance of the proposed circuits and conditions given for the ideal case in the previous table are modified if non-idealities are included. Non-ideality analysis considering current and voltage tracking errors taken into account are carried out for each circuit separately. Equations modeling non-ideal elements are given in Tab. 2.

3. CFOA Parasitic Effects

Using standard notation, the CFOA depicted in Fig. 1 can be defined as $I_Y = 0$, $I_Z = I_X$, $V_X = V_Y$ and $V_W = V_Z$. Likewise, a non-ideal CFOA can be represented in the *s*-domain by the following equations:

$$I_Y = (sC_Y + 1/R_Y)V_Y, \tag{3a}$$

$$I_Z = \alpha I_X + (sC_Z + 1/R_Z)V_Z, \tag{3b}$$

$$V_X = \beta V_Y + R_X I_X, \tag{3c}$$

$$V_W = \gamma V_Z + R_W I_W \tag{3d}$$

where R_X, R_Y , R_Z, R_W and C_Y , C_Z are parasitic resistances and capacitances at corresponding ports of the CFOA, respectively. Note that a plus-type CCII (CCII+) is represented by the equations (3a) through (3c). Thus, a CFOA is a buffered output CCII+. A CF can be obtained from the CCII by grounding the *Y* terminal of the CCII.

The parasitic resistances R_X and R_W appearing in series, respectively, at terminals *X* and *W* are ideally equal to zero. On the other hand, the parasitic resistances $R_Z = 1/G_Z$ and $R_Y = 1/G_Y$, respectively, in parallel with $1/(sC_Z)$ and $1/(sC_Y)$ are ideally infinite. These parasitic elements bring extra terms to the impedances of the inductor simulator circuit. Therefore, reduction methods can be used in simulator circuits to improve their frequency performance.

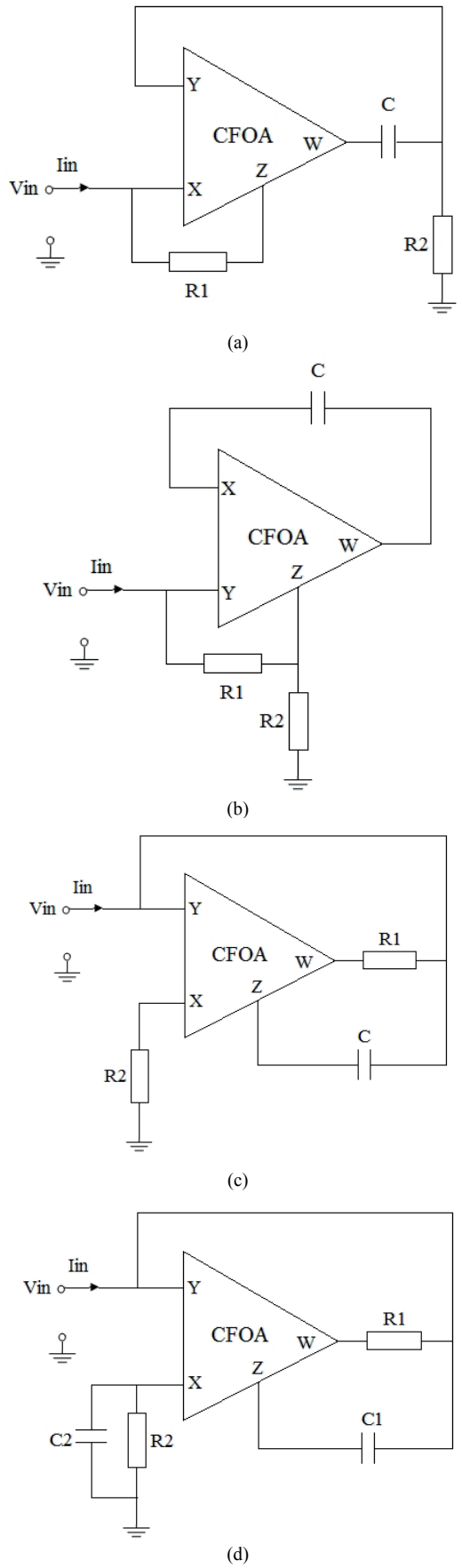

Fig. 2. Inductance simulators realized using single CFOA.

4. Applications and Simulation Results

All of the circuits illustrated in Fig. 2 are tested with SPICE simulations. The test circuits were constructed with AD844. The circuit in Fig. 2 (b) was supplied with symmetrical voltages of 10 V. The element values are chosen as $C_1 = 10$ nF, $R_1 = R_2 = 1$ kΩ to obtain an inductance of $L_{eq} = 10$ mH and a series resistance of $R_{eq} = 0.5$ kΩ. The frequency response of the topology in Fig. 2(b) is chosen as an example to demonstrate the performance of the derived inductance simulators. Fig. 3 shows that the magnitudes of the impedances of an ideal inductor and a lossy inductor that is a series RL circuit can be made very close for a set of selected values over many decades.

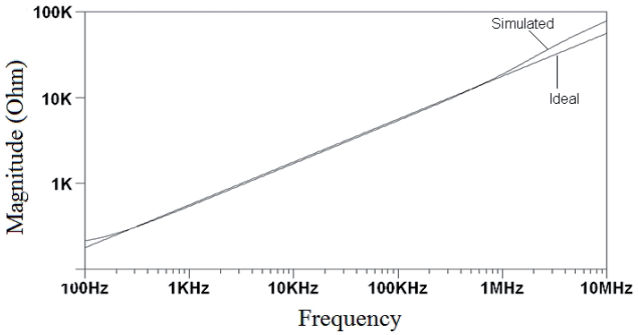

Fig. 3. Ideal and simulated frequency responses of the series (RL) inductor simulator.

Negative inductance is especially important if the parasitic effects have to be cancelled. The magnitude of the negative inductance increases with frequency in the same way as for positive inductances. However, a negative inductance provides a negative 90° phase shifting. Typical waveforms of the voltage and current through the proposed negative inductance simulator are shown in Fig. 4.

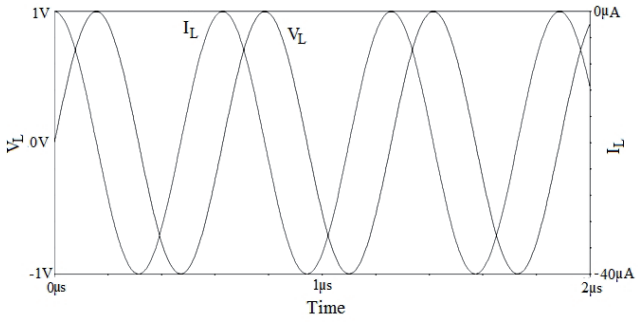

Fig. 4. Waveforms of voltage and current of the proposed negative inductance.

To illustrate an application of the negative inductance simulator, it is employed in an inductance cancellation circuit shown in Fig. 5 [20], where $V_{in} = 1$ V, $R = 100$ kΩ and $L = 5$ mH. Applying a sinusoidal input signal of 1.59 MHz with an amplitude of $V_{IN} = 1$ V, the transient responses of output current I_R and input voltage are obtained and illustrated in Fig. 6. It is shown that the inductance in the circuit has been cancelled by the negative inductance simulator.

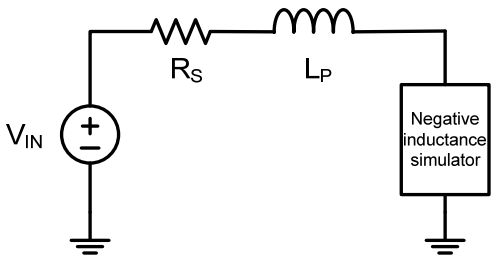

Fig. 5. Inductance cancellation circuit using negative inductance simulator.

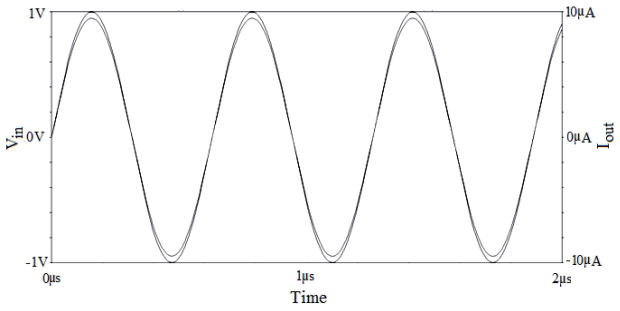

Fig. 6. Transient responses of the inductance cancellation circuit.

In order to demonstrate the performances of the proposed circuits, the second circuit with traditional CFOA is chosen as an example. Furthermore a low-pass filter circuit was realized as an application example by connecting a series capacitor to the circuit illustrated in Fig. 2(b). The proposed inductance simulator was used for constructing a second-order voltage mode low-pass filter shown in Fig. 7. The circuit is designed to simulate a series R-L combination consisting of an inductor with L_{eq} = 0.1 mH and a resistance R_{eq} = 0.5 kΩ. To obtain these values, the following values are chosen: $R_1 = R_2 = 1$ kΩ and C = 0.1 nF. Choosing the capacitor with C_L = 100 pF and driving the resulting RLC circuit with voltage of 1 V, the frequency responses of the ideal and simulated low-pass filter circuits are investigated. The circuit was supplied with symmetrical voltages of ±10 V. PSPICE simulations were performed using AD844.

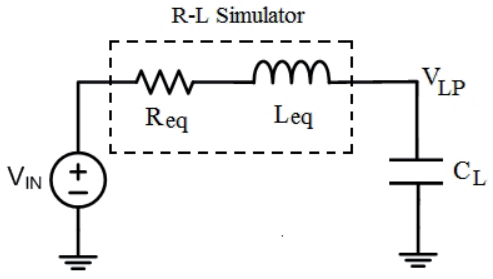

Fig. 7. Voltage-mode low-pass filter application of the series +L with +R lossy inductor simulators.

The frequency response of the actual circuit obtained from SPICE simulations is given with the response of the ideal circuit in Fig. 8. The simulation results show that filter characteristics are in good agreement with the predicted theoretical values. There is little difference between ideal and non-ideal responses in the high frequency region of the frequency response of this filter. Time domain analysis result is given in Fig. 9 for peak-to-peak 2 V, 1 MHz sine wave input for low-pass filter configuration for the circuit in Fig. 7.

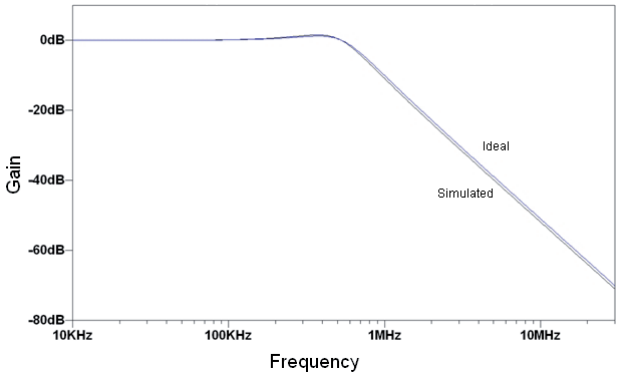

Fig. 8. Ideal and simulated frequency response of low-pass filter.

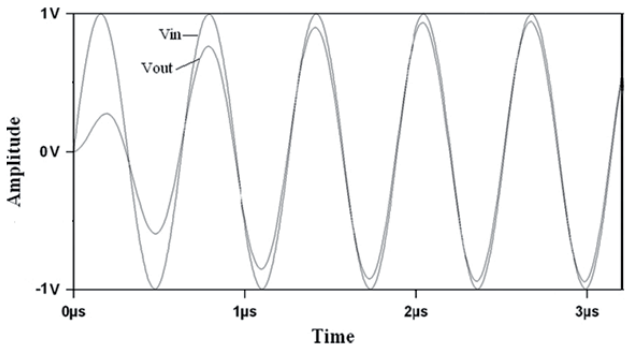

Fig. 9. Time domain response of circuit in Fig. 7 for 2 V peak-to-peak 1 MHz sine wave input for low-pass filter configuration.

5. Conclusion

In this paper four different inductance simulating topologies employing a current feedback operational amplifier are proposed. Each presented topology employs only one CFOA. Examples of applications are given in order to illustrate the practical use of the topologies. Simulation results are included to verify the theory. It is expected that the proposed series and parallel inductance simulators will be useful in analog signal processing applications such as filter and chaotic oscillator design.

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