New CMOS-based Resistor-less Current-mode First-order All-pass Filter Using only Ten Transistors and One External Capacitor

Abhirup LAHIRI

36-B, J and K Pocket, Dilshad Garden, Delhi, India

lahiriabhirup@yahoo.com

Abstract. *This paper proposes a new, compact CMOS realization of current-mode (CM) first-order all-pass filter (APF) using no external resistors. The circuit is created using only ten transistors and one external capacitor. The circuit uses lower number of transistors as compared to previously reported CM APFs using active building block (ABB) based approach. A comparison with previously reported CM APFs in terms of number of transistors and current consumption has been provided. As a design example, a 512 kHz pole-frequency (at typical process and 27ºC) CM APF is designed in 40nm CMOS technology and validated through SPICE simulations.*

Keywords

Analog circuits, current-mode (CM), first-order all-pass filter (APF), resistor-less.

1. Introduction

Recent criticism not withstanding [1], the current-mode (CM) techniques have given way to a number of important analog signal processing/signal generation circuits and which is evident from the vast amount of literature on such circuits published over the last three decades, see [2]-[3] and references therein. CM first-order all-pass filters have received a lot of attention in the last decade and numerous implementations using a variety of active building blocks (ABBs) have been proposed. The use of novel CM ABBs for implementing compact CM circuit solutions has received a lot of attention with authors claiming their solutions to be minimal in terms of the employed ABBs. Note that each of these ABBs, for an example, the very popular current differencing transconductance amplifier (CDTA) (proposed by D. Biolek in 2003, [4]) requires more than eighteen transistors for CMOS implementation [5], [6] and thus, unless the circuit solution is meant for bread-board type implementations using commercially available ICs, the claim of minimal circuit solution in terms of the number of ABBs (a "black-box") is misleading as really matters is the number of employed transistors for monolithic integration. The author admits to the fact that several of his works also include the so-labeled "minimal CM APF using one ABB and one capacitor" [7]. But although the focus since the last several years has been to realize minimum ABB circuit solutions, it is more meaningful to focus on minimum transistor circuit solutions for monolithic integration and which would save much of silicon area and consume lesser power. Further the advent of new ABBs and minimal circuit solutions using these new ABBs are also not very suitable for bread-board implementations as many of the newly reported ABBs are often conceptualized and not available as "off-the-shelf" components. Thus, even for discrete-component realizations on bread-board, the solutions are often not minimal and require the use of several op-amps and/or OTAs for their realization (e.g., creating a single DVCC requires three current-feedback operational-amplifiers (CFOA) ICs and two matched resistors [8]). The author of course does not rule out the advantage of ABB based design approach in creating new circuit solutions and devising additional useful approaches to create the circuit solutions, but believes that having realized a compact ABB based circuit solution, the focus should be on compact CMOS realization of the solution for monolithic integration. Before presenting the newly proposed CMOS CM APF, a comparative study of the most recent CM APFs have been provided in Tab. 1.

Rest of this communication is organized as follows: section 2 provides the CMOS implementation of the proposed APF, section 3 provides the simulation results of the designed 512 kHz pole frequency (at typical process and 27ºC) CM APF in 40nm CMOS technology and section 4 provides the concluding remarks.

2. Proposed Circuit

Based on the concept that an APF function can be realized with 1-2*LPF, where LPF is low-pass filtering function, the proposed CMOS CM APF is shown in Fig. 1. The circuit offers low input resistance- $1/(g_{m0}+g_{m1})$ and high output resistance – $r_{o5}||r_{o7}||r_{o9}$. As compared to other CM APFs pointed in Tab. 1 (excluding [23]), our circuit

Ref.	ABB type[#]	No. of ABBs	No. of transistors	No. of resistors	No. of external capacitors	Power consumption (mW)
[9]	CCII	1	-	4	2	-
[10]	CCII	1	-	4	2	-
[11]	CCIII	1	56[++]	3	1	-
[12]	CCIII	1	24*	1	1	-
[13]	MOCCII	2	46	1	1	-
[14]	FDCCII	1	36	3	1	-
[15]	CCCII	1	15	0	1	-
[16]	CCCII	2	32	0	1	6.5[+]
[17]	CDBA	1	20*	1	1	-
[6]	CDTA	1	18	2	1	0.37
[18]	CDTA	2	48*	0	1	10.2[+]
[7]	CDTA	1	34	0	1	2.4[+]
[19]	OTA	2	*D*	1	1	-
[20]	OTA	1	12*	2	1	-
[21]	DVCC	1	18	2	1	-
[22]	FTFN	1	*D*	2	1	-
[23]	-	-	5*	0	0	0.28
Proposed	-	-	10	0	1	0.98

Tab. 1. Comparative study with previous works:
[#] Refer Appendix for nomenclature of the ABBs,
- Not mentioned,
* Ideal current sources assumed,
[+] found using biasing current details,
D Discrete ICs used,
[++] Using reference [24].

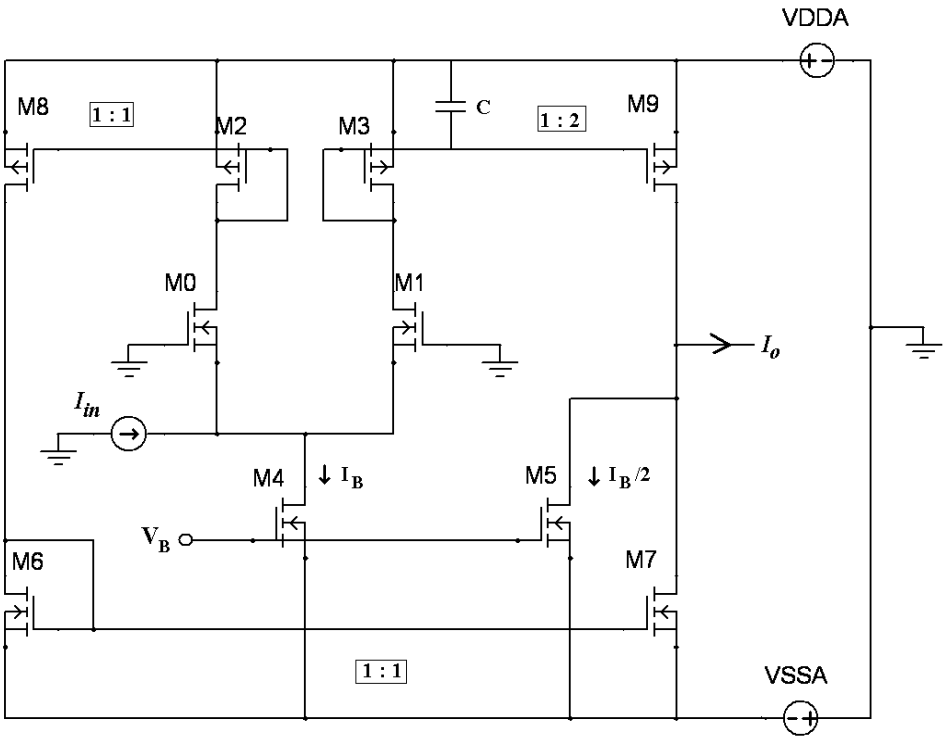

Fig. 1. CMOS current-mode all-pass filter.

does not use the ABB based approach and is a direct CMOS CM APF. The circuit in [23] uses five transistors but the current sources in the schematic are shown to be ideal. Considering a simple MOSFET as the required V-I convertor, the circuit in [23] would require only eight transistors. Note that the circuit in [23] utilizes internal MOS capacitances (e.g. C_{gs} and C_{gd}) of the current-mirrors to realize the APF. Since both C_{gs} and C_{gd} are voltage dependent capacitances (with a non-linear relationship) this technique would require appropriate node biasing of the

current mirrors (e.g. $V_G >> V_{TN}$), so that the average pole frequency does not vary much due to the variations in C_{gs} and C_{gd}, when processing the input signal. Also, the circuit in [23] requires one time constant of a current mirror to be much larger than the time constant of the other current-mirror to actually realize the APF transfer function (the ratio of time constants in [23] is 1:4). If this condition is not fulfilled, the circuit also degrades the output amplitude with increasing frequency while providing the required signal phase-shift. To alleviate the problems, our circuit employs external linear capacitor much larger than MOS parasitic capacitances (thereby providing voltage independence to one of the components deciding the pole frequency). Further, keeping the external linear capacitor much larger than the C_{gs} guarantees the transfer function of the circuit to be close to equation (6) of [23], rather than equation (3). Thus, in the operating frequency range much smaller than the pole frequencies of the mirrors, the proposed circuit provides 0º-180º phase shift without any amplitude degradation. Using routine circuit analysis of Fig. 1, we find the following transfer function

$$T(s) = \frac{I_o(s)}{I_{in}(s)} = \frac{1}{2}\frac{(sC - g_{mp})}{(sC + g_{mp})} \tag{1}$$

where g_{mp} represents the transconductance of matched PMOS transistors M2-M3. It is again emphasized that $C >> C_{gs}$ and the operating frequencies for which (1) is true (i.e. APF function is valid) is $\omega << g_m/(2C_{gs})$. The above equation is representative of the first-order all-pass filtering function with phase shift of the input signal by

$$\angle T(j\omega) = 180° - 2\tan^{-1}\left(\frac{\omega C}{g_{mp}}\right) \tag{2}$$

3. Simulation Results

To verify the workability of the proposed circuit, a 512 kHz pole frequency (at typical process and 27ºC) CM APF is designed in 40nm CMOS technology with ±1.25 V supply. The aspect ratios of the transistors are shown in Tab. 2.

Transistor	W/L (µm/µm)
M0-M1	10/0.3
M2, M3, M8	24/1
M6, M7	16/2
M4	64/4
M5	32/4
M9	48/1

Tab. 2. Aspect ratios of the transistors in CM APF.

Thick gate oxide (GO2) transistors (50A) are used for the analog design at this supply voltage and it should not be surprising that the transistors are not minimal length of the technology (i.e. 40nm). Precision analog circuits are preferably designed using long channel length transistors to reduce short-channel effects and deliver good performance (e.g. current mirrors are always designed with long channel length transistors to alleviate effects of channel-length modulation, provide good current mirroring and high output impedance) and also lower the effects of device mismatch on circuit parameters. Also, the details of minimal length of the GO2 transistors (used for analog circuits) to be used in design are always provided according to design for manufacturability rules and in this technology, it is preferred that GO2 transistors have more than 0.3u channel length. Transistors with 40nm channel length would typically be used for digital circuits like logic gates and flip-flops (these transistors are thin gate oxide and working at a reduced supply voltage not suitable for analog designs).

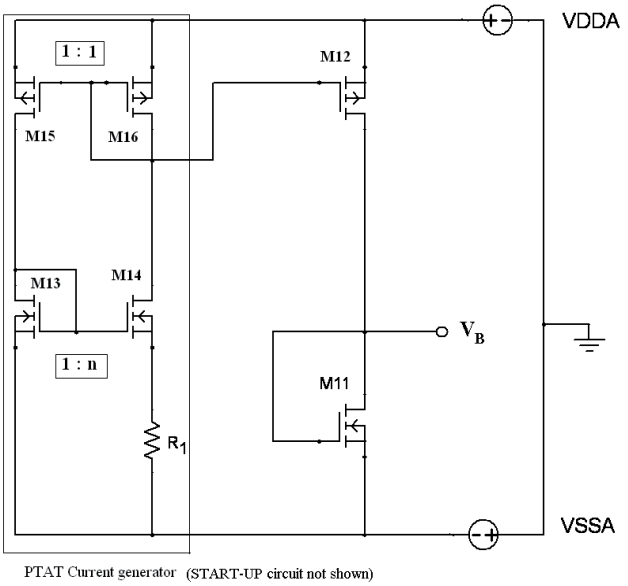

Fig. 2. Bias-voltage (V_B) creation using PTAT current generator.

The biasing voltage V_B is generated using the PTAT bias current generator circuit (Fig. 2) which acts as a common current/voltage biasing block for all other circuits present on the chip in addition to the CM APF. The transistors M13-M14 work in sub-threshold region to produce a PTAT current $I_B' = mV_T \ln(n)/R_1$, which flows into the diode-connected transistor M11 to generate V_B for the CM APF. The PTAT current not only helps in reducing the transconductance variation with temperature of MOSFETS in APF (thereby reducing the variation of pole frequency with temperature), but also is essential for ultra-low-power realization of the bias current generator and the CM APF. Constant-gm biasing circuit is not used since it leads to larger change of the bias current (and thus power consumption) with temperature ($\propto T^{1.5}$) as compared to the PTAT current ($\propto T$). However, constant-gm biasing can be useful if the main concern is to reduce the pole frequency variation of the APF; thus there is a design-tradeoff. Note that the transistor count of the bias current generator is not taken into account and only the transistors employed in the APF (Fig. 1) have been considered. Also,

although the bias voltage generator uses an external resistor, the CM APF is resistor-less and MOS transconductance is utilized to simulate resistance. The bias generator generates I_B' of the order of 220 nA to 280 nA at typical process corner and temperature range of -40ºC to 125ºC and tail current for the CM APF, I_B= 96 uA at 27ºC. Clearly, the current consumption of the bias generator block (considering M15-M16 arms) is negligible with respect to the CM APF. With capacitor value C = 100 pF (a value much larger than C_{gs3}, C_{gs9}), the magnitude and phase response of the circuits at different operating temperatures, namely -40ºC, 27ºC and 125ºC are shown in Fig. 3 and 4, respectively.

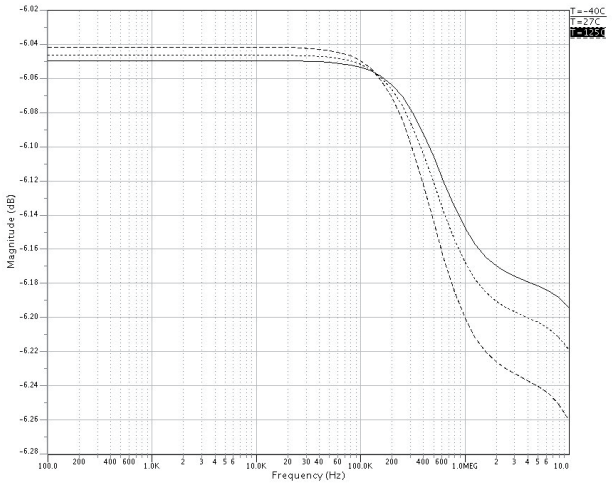

Fig. 3. Magnitude response of the CM APF at different operating temperatures.

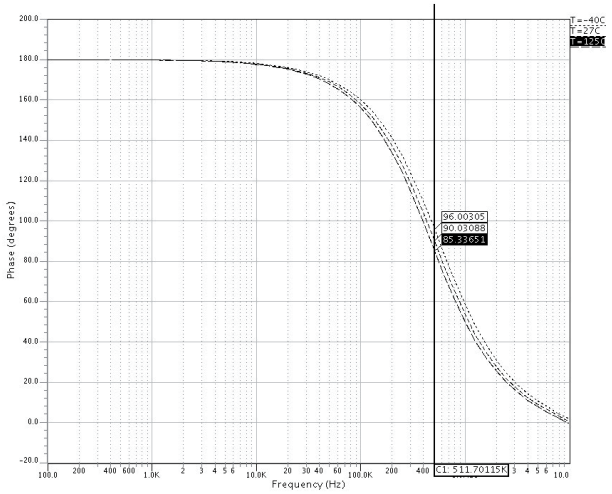

Fig. 4. Phase response of the CM APF at different operating temperatures.

The gain of the filter changes by 0.22 dB in the operating frequency range of 100 Hz-10 MHz and temperature range of -40ºC to 125ºC, while providing phase shift of 0º-180º. The pole frequencies (i.e. the frequency at which phase-shift is 90º), transconductance (g_{mp}) and current consumption values at these temperatures are provided in Tab. 3.

Temperature [°C]	Pole frequency [kHz]	Transconductance g_{mp} [μA/V]	Current consumption [μA]
-40	570.62	349.71	311.90
27	512.01	314.12	337.12
125	473.03	287.91	392.80

Tab. 3. Simulated parameters for CM APF at different temperatures.

The transistors are also sized appropriately to reduce the affect of device mismatches on the pole frequency. Monte-Carlo analysis with 500 runs at 27 ºC gives 1σ = 40.5 kHz, which is about 0.08%. Transient analysis of the circuit at 27ºC and input frequency of 512 kHz is shown in Fig. 5 and the output THD is less than 2%. The linear range of the circuit, as shown in Fig. 6, is obtained using DC simulation and can be extended further by increasing the tail bias current which leads to increased power consumption.

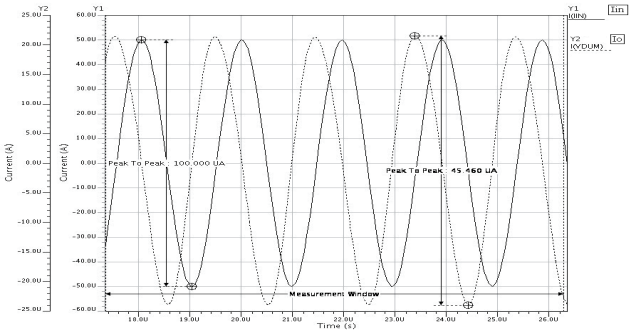

Fig. 5. Transient simulation with input signal of 100 μA pp. and 512 kHz frequency.

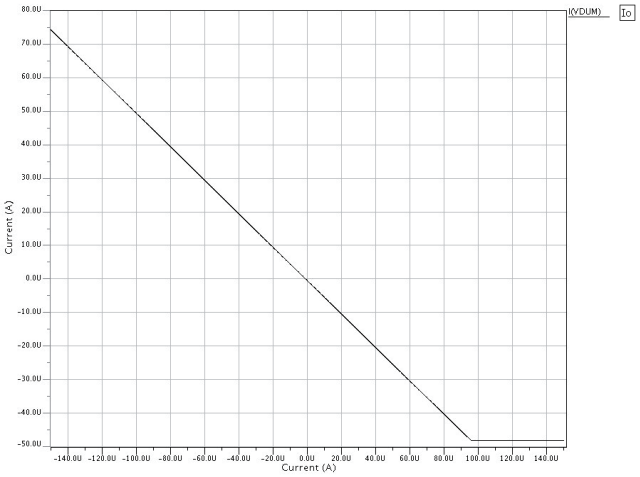

Fig. 6. Linear range of the designed CM APF.

4. Concluding Remarks

A new CMOS-based CM first-order APF using only ten transistors, no external resistors and one external capacitor is proposed. Unlike the ABB based approach, the solution provides direct and compact CMOS realization of

the circuit. A 512 kHz pole frequency (at typical process and 27ºC) CM APF is designed in 40nm CMOS technology with ±1.25 V supply and verified using SPICE simulations. It is believed that the circuit would be useful to both the workers and researchers in the field and more compact and low-power CMOS realizations of the CM APF are proposed in the near future.

5. Appendix

This section provides full nomenclature of the aforementioned ABBs.

CCII: Second-generation current conveyor
CCIII: Third-generation current conveyor
MOCCII: Multiple-output second-generation current conveyor
FDCCII: Fully-differential second-generation current conveyor
CCCII: Second-generation current-controlled conveyor
CDBA: Current-differencing buffered amplifier
CDTA: Current-differencing transconductance amplifier
OTA: Operational transconductance amplifier
DVCC: Differential voltage current conveyor
FTFN: Four-terminal floating nullor

References

[1] SCHMID, H. Why 'current-mode' does not guarantee good performance. *Analog Integrated Circuits and Signal Processing*, 2003, vol. 35, no. 1, p. 79–90.

[2] BIOLEK, D., SENANI, R., BIOLKOVA, V., KOLKA, Z. Active elements for analog signal processing: classification, review, and new proposals. *Radioengineering*, 2008, vol. 17, no. 4, p. 15-32.

[3] YUAN, F. *CMOS Current-Mode Circuits for Data Communications*. Springer, ISBN- 0-387-29758-8.

[4] BIOLEK, D. CDTA–building block for current-mode analog signal processing. In *Proceedings of European Conference on Circuit Theory and Design*, 2003, p. 397-400.

[5] BIOLEK, D., HANCIOGLU, E., KESKIN, A. U. High-performance current differencing transconductance amplifier and its application in precision current-mode rectification. *AEU-International Journal of Electronics and Communications*, 2008, vol. 62, p. 92-96.

[6] UGYUR, A., KUNTMAN, H. Low -voltage current differencing transconductance amplifier in a novel allpass configuration. In *Proceedings of IEEE MELCON*, 2006, p. 23-26.

[7] LAHIRI, A. Novel first-order current-mode all-pass filter using CDTA. *Radioengineering*, 2009, vol. 18, no. 3, p. 300-305.

[8] MAHESHWARI, S. Quadrature oscillator using grounded components with current and voltage outputs. *IET- Circuits Devices Systems*, 2009, vol. 3, no. 4, p. 153-160.

[9] UN, M., KACAR, F. New second generation current conveyor-based current-mode first order all-pass filter and quadrature oscillator. *Journal of Electrical & Electronics engineering-Istanbul University*, 2007, vol. 7, p. 119-127.

[10] NANDI, R. Novel current-mode all-pass phase shifter using a current conveyor. *IEEE Transactions on Instrumentation and Measurement*, 1992, vol. 41, no. 4, p. 553-555.

[11] UN, M., KACAR, F. Third generation current conveyor based current-mode first order all-pass filter and quadrature oscillator. *Journal of Electrical & Electronics Engineering*, 2008, vol. 8, no. 2, p. 529-535.

[12] MAHESHWARI, S. Novel first-order current-mode all-pass sections using CCIII. *Active and Passive Electronic Components*, 2004, vol. 27, p. 111-117.

[13] KHAN, I. A., BEG, P., AHMED, M. T. First order current mode filters and multiphase sinusoidal oscillators using CMOS MOCCIIs. *The Arabian Journal of Science and Engineering,* 2007, vol. 32, no. 2C, p, 119-126.

[14] MOHAN, J., MAHESHWARI, S., SINGH, S.V., CHAUHAN, D.S. Grounded capacitor first order all-pass filters using single active element. In *International Conference on Advances in Recent Technologies in Communication and Computing*, 2009 , p. 333-336. DOI 10.1109/ARTCom.2009.150

[15] KUMNGERN, M. Electronically tunable current-mode all-pass filter-based high-Q bandpass filter using minimum elements. In *Proceedings of IEEE TENCON 2009*, p. 1-4.

[16] KUMNGERN, M., SAMPATTAVANICH, P., PROMMEE, P., DEJHAN, K. A capacitor-grounded current-tunable current mode all-pass network. In *Proceedings of IEEE TENCON 2004*, pp. 384-386.

[17] TOKER, A., OZOGUZ, S., CICEKOGLU, O., ACAR, C. Current-mode all-pass filters using current differencing buffered amplifier and a new high- bandpass filter configuration. *IEEE Transactions on Circuits and Systems*, 2000, vol. 47, no. 9, p. 949-954.

[18] TANJAROEN, W., TANGSRIRAT, W. Resistorless current-mode first-order allpass filter using CDTAs. In *Proceedings of ECTI-CON 2008*, p. 721-724.

[19] PSYCHALINOS, C., PAL, K. A novel all-pass current-mode filter realized using a minimum number of single output OTAs. *Frequenz,* 2010, vol. 64, p. 30-32.

[20] PROMMEE, P., ANGKEAW, K., CHANWUTITUM, J., DEJHAN, K. Dual input all-pass networks using MO-OTA and its application. In *Proceedings of ECTI-CON 2007*, p. 129-132.

[21] MINAEI, S., IBRAHIM, M. A., KUNTMAN, H. DVCC based current-mode first-order all-pass filter and it's application. In *Proceedings of IEEE ICECS 2003*, p. 276-279.

[22] HIGASHIMURA, M. Current-mode allpass filter using FTFN with grounded capacitor. *Electronics Papers*, 1992, vol. 27, no. 13, p. 1182-1183.

[23] SRISUCHINWONG, B., LEELASANTITHAM, A. A 2V CMOS capacitorless current-tunable all-pass filter using current mirrors. *Thammasat International Journal of Science and Technology*, 2001, vol. 6, no. 1, p. 46-51.

[24] MINAEI, S., YILDIZ, M., KUNTMAN, H., TURKOZ, S. High performance CMOS realization of the third generation current conveyor (CCIII). In *Proceedings of IEEE MWSCAS*, 2003, p. 307-310.

About Author…

Abhirup LAHIRI received Bachelor of Engineering (B.E.) degree with the highest honors from the Division of Electronics and Communications, Netaji Subhas Institute of Technology (erstwhile, Delhi Institute of Technology), University of Delhi, India. His past research works include

design of compact analog circuit solutions using novel voltage-mode and current-mode active elements. His current research interests include low-power and low-voltage analog circuit design and precision voltage and current reference generation. He has authored/co-authored more than thirty international journal/conference papers (including fifteen SCI/SCI-E publications) and has acted as a reviewer (by editor's invitation) for numerous international journals and conferences of repute. He served as a program committee member for The 33rd International Conference on Telecommunications and Signal Processing (TSP). He is an editorial board member of Radioengineering Journal for the years 2011-2012. His biography is included in Marquis Who's Who in the World 2011- (28th Edition).

RADIOENGINEERING REVIEWERS

September 2011, Volume 20, Number 3

- ABUELMA'ATTI, M. T., King Fahd University of Petroleum & Minerals, Saudi Arabia
- ARCE-DIEGO, J. L., University of Cantabria, Santander, Spain
- ARTHABER, H., Vienna University of Technology, Austria
- BALTZIS, K., Aristotle University of Thessaloniki, Greece
- BEČVÁŘ, Z., Czech Technical University in Prague, Czechia
- BHASKAR, D., National Islamic University, New Delhi, India
- BIOLEK, D., University of Defense, Brno, Czechia
- BOBULA, M., RACOM company, Czechia
- BONEFAČIĆ, D., University of Zagreb, Croatia
- BURDA, K., Brno Univ. of Technology, Czechia
- CHAUDRY, A., Panjab University, India
- CHEN, H.-P., Ming Chi University of Technology, Taiwan
- ČERNÝ, P., Czech Technical University in Prague, Czechia
- ČÍKA, P., Brno Univ. of Technology, Czechia
- DEL-RIO, C., University of Navarra, Spain
- DJIGAN, V., R&D Center of Microelectronics, Russia
- DOBEŠ, J., Czech Technical University in Prague, Czechia
- DROTÁR, P., Honeywell International, Czechia
- EOIN, T., University College Cork, Ireland
- FANJUL-VÉLEZ, F., University of Cantabria, Spain
- FEDRA, Z., Brno Univ. of Technology, Czechia
- FILANOVSKY, V., University of Alberta, Canada
- FLIEGEL, K., Czech Technical University in Prague, Czechia
- FONTAN, P. F., University of Vigo, Spain
- FRANCHI, E., University of Bologna, Italy
- FRANEK, O., Aalborg University, Denmark
- FUCHS, M., Brno University of Technology, Czechia
- FUČÍK, O., Brno University of Technology, Czechia
- GAI, Y., University of Southern California, USA
- GAZDA, J., Technical University of Košice, Slovakia
- GEORGIADIS, A., Centre Tecnologic de Telecomunicacions de Catalunya, Barcelona, Spain
- GOŇA, S., Tomas Bata University in Zlin, Czechia
- GRGIĆ, S., University of Zagreb, Croatia
- HASSANI, M., Islamic Azad University, Iran
- HAZDRA, P., Czech Technical University in Prague, Czechia
- HENNIGER, H., German Aerospace Center, Germany
- HORNG, J.-W., Chung Yuan Christian University, Taiwan
- HORSKÝ, P., AMIS Czech, Ltd., Brno, Czechia
- JAIKLA, W., Suan Sunandha Rajabhat University, Thailand
- JELÍNEK, L., Czech Technical University in Prague, Czechia
- KESKIN, A. U., Yeditepe Univ., Istanbul, Turkey
- KOCUR, D., Technical Univ. of Košice, Slovakia