Design of the 12-bit Delta-Sigma Modulator using SC Technique for Vibration Sensor Output Processing

Michal PAVLIK, Vilem KLEDROWETZ, Jiri HAZE

Dept. of Microelectronics, Brno University of Technology, Faculty of Electronic Engineering and Communication, Technicka 10, 616 00 Brno, Czech Republic

pavlik@feec.vutbr.cz

Abstract. *The work deals with the design of the 12-bit Delta-Sigma (ΔΣ) modulator using switched capacitors (SC) technique. The modulator serves to vibration sensor output processing. The first part describes the ΔΣ modulator parameters definition. Results of the proposed topology ideal model were presented as well. Next, the ΔΣ modulator circuitry on the transistor level was done. The ONSemiconductor I2T100 0.7 μm CMOS technology was used for design. Then, the ΔΣ modulator nonidealities were simulated and implemented into the MATLAB ideal model of the modulator. The model of real ΔΣ modulator was derived. Consequently, modulator coefficients were optimized. Finally, the corner analysis of the ΔΣ modulator with the optimized coefficients was simulated. The value of SNDR = 82.2 dB (ENOB = 13.4 bits) was achieved.*

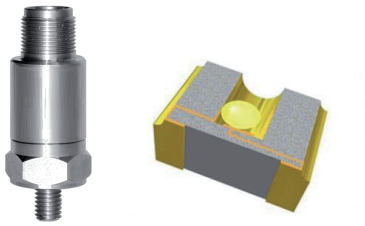
Keywords

Vibration sensor, Delta-Sigma modulator, Switched Capacitor technique, MATLAB model.

1. Introduction

Currently, the vibration sensors usually used in the industry are fabricated in steel body. The sensor is attached to analyzed source of vibration by metric thread (e.g. producers Viditech [1], Wilcoxon [2], Imi sensors [3], etc.). These sensors are usually based on the use of piezo-resistive material, CCLD (Constant Current Line Drive) sensors or motion sensors that use micro-balls in the capsule [4], [5]. Vibration sensor is composed of both the sensor itself and electronic circuits. Electronic circuits process the sensor output signal and occupy the most area.

Even though, the vibration sensor has relatively small dimensions, the evaluation electronics implemented on the PCB increases the sensor final size. The evaluation electronics usually consists of analog filter, Analog to Digital Converter (ADC), signal processing circuits (e.g. Digital Signal Processor - DSP) and communication interfaces. Implementation of the evaluation electronics in integrated circuit would allow significant miniaturization of the sensor.



a) b)

Fig. 1. Examples of the vibration sensors: a) industry sensor capsule, b) microball sensor.

Frequency band of the vibration sensor output is usually in the range from 10 Hz to 5 kHz. These parameters are not critical. Nevertheless, the industrially manufactured sensors usually have resolution of the AD conversion from 10 to 12-bit (e.g. Viditech [1] sensor type ATW08). Many converters based on different principles (integration, successive approximation, pipelined, ΔΣ modulator) could be used for processing the sensor output signal.

The paper discusses the design of ΔΣ modulator. The modulator together with digital filter (decimator) composes AD converter. It is one of the main components of the vibration sensor evaluation electronics.

Similarly to converters based on the other conversion principles there are a number of the ΔΣ modulator structures (e.g. cascaded, MASH or multi-bit [6-9]). The easiest way to implement ΔΣ modulator is probably a cascade structure (first to third order). Nevertheless, it is difficult to ensure modulator stability in the case of high-order modulators [6-10]. The cascaded structures can be generally divided into DIFF (Distributed Input and Forward Feedback) and DIDF (Distributed Input and Distributed Feedback) [6], [7].

The last step is the selection of technology and circuit techniques, which will implement the modulator. The selected technology determines the technological parameters of the components. Applicable compensation techniques primarily depend on used circuit technique (e.g. the overall noise reduction [11-15], operational amplifiers offset minimizing [14-16], etc.).

The article describes development procedure of the ΔΣ modulator using SC technique step by step (from

choosing an appropriate structure to implement into the transistor level).

2. The Design Background

The chip manufacturing technology, circuit technique, principle of the converter function and its structure are selected during the ADC design preparation.

2.1 Definition of Parameters of the Converter and Structure Selection

The first step is a proper definition of the converter's parameters, we want to achieve. The chip manufacturing technology usually influences many modulator parameters, e.g. supply voltage, voltage swing, maximal frequency, etc. In our case, the converter was designed in CMOS technology ON Semiconductor I2T100 0.7 μm (I2T100). The constraints resulted from the technology must be taken into account when the structure and principle of the converter is chosen. In case of I2T100 technology, the required parameters are reported in Tab. 1.

Parameter	Symbol	Value	Unit
Clock frequency	f_{vz}	2	MHz
Bandwidth	f_{BW}	5	kHz
Effective number of bits	*ENOB*	12	-
Signal to Noise Ratio	*SNR*	74	dB
Supply voltage	V_{SS}	5	V
Common mode voltage	V_{CM}	2,5	V
Signal amplitude	v_{INm}	2	V

Tab. 1. Defined converter parameters.

The implemented converter is based on the ΔΣ modulation principle. The second order of the modulator was chosen. The *OSR* of the proposed converter is

$$OSR = \frac{f_s}{2 f_{bw}} = \frac{2.10^6}{2.5.10^3} = 200 . \quad (1)$$

Theoretically, this modulator could achieve a Signal to Noise Ratio (*SNR*) [10]

$$SNR = \left(\frac{3\pi}{2}\right)(2N+1)\left(\frac{OSR}{\pi}\right)^{(2N+1)} \cong 104\ dB \quad (2)$$

where *N* is order of the modulator. Value of approximately 104 dB is only theoretical and can't be achieved in real application. However, this result verified the required parameters met for designed ΔΣ modulator.

2.2 The Selection of Transfer Coefficients of the Modulator

The achievable *SNR* is defined by the noise transfer function (*NTF*) and signal transfer function (*STF*) given by modulator structure. In our case, the chosen structure is CIDIDF, whose ideal model is shown in Fig. 2. The zero values of the coefficients b_2 and b_3 lead to increased stability of the modulator. However, it is balanced by reduction of achievable *SNR*.

Coefficient	Value
a_1	0.75
a_2	0.75
b_1	0.75
b_2	0
b_3	0
c_1	1
c_2	3

Tab. 2. The chosen values of the coefficients.

The remaining coefficients (Tab. 2) were chosen according to recommendations in [8]-[10].

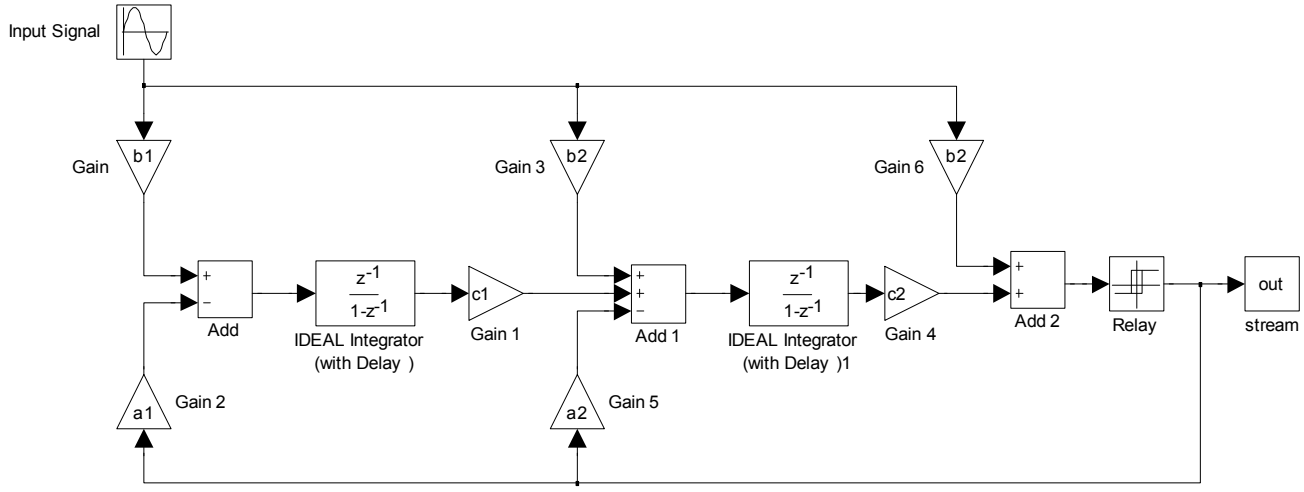


Fig. 2. Ideal model of the second order ΔΣ modulator in MATLAB SIMULINK.

2.3 The Ideal Modulator Simulations

Even if the *SNR* value is important, the most significant indicator of the converter quality is Signal to Noise and Distortion Ratio (*SNDR* or *SINAD*). Assuming the ideal modulator model the attainable *SNDR* value with selected coefficients is

$$SNDR = 99.3\,dB\,, \tag{3}$$

as can be observed in Fig. 3 that describes the power spectral density of the modulator output signal.

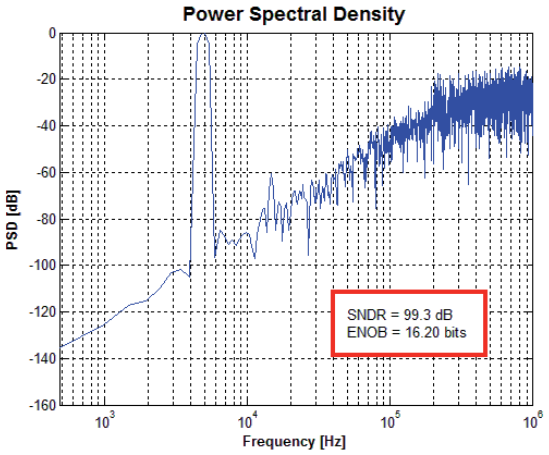


Fig. 3. Power spectral density output of the ideal modulator with coefficients according to Tab. 2.

It would seem that the lowest *SNDR* has to be measured at the f_{BW} due to modulator noise shaping feature. However this assumption is not correct. When the *SNDR* in the frequency band is examined, the 3rd harmonic of the input signal that produces the most amount of the distortion is out of the calculation. The degradation of *SNDR* is caused by intrinsic slew-rate limitation of ΔΣ modulator [9]. Fig. 4 describes the dependence of *SNDR* on the frequency of the modulator input signal. The graph shows that there is a significant decline in value of *SNDR* at the input signal frequency equal to one third of the frequency on border of the modulator bandwidth.

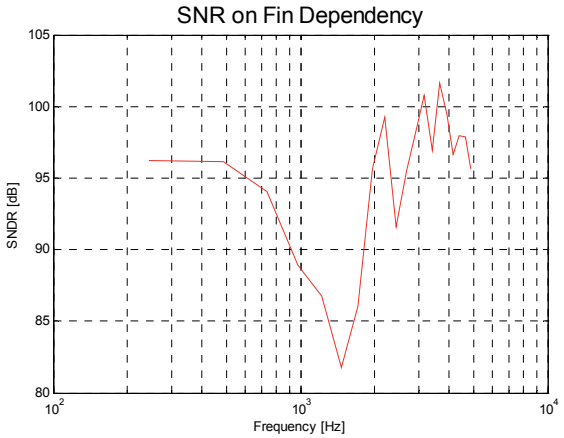


Fig. 4. Dependence of *SNDR* on the input signal frequency (non optimized transfer parameters).

To verify whether the modulator meets the required *SNDR* value it is necessary to determine its value dependence on the frequency

$$f_t = \frac{1}{3} f_{BW}\,. \tag{4}$$

The lowest *SNDR* of the ideal modulator throughout the frequency bandwidth was found *SNDR* = 82.8 dB.

3. Design and Modeling of the Modulator Fundamental Blocks

There is a possibility to mathematically modeling the ΔΣ modulator and its transfer functions by arbitrary parameters. It allows using more or less the noise modulating potential. But if the real behavior of circuits is taken into account, it could radically change the modulator parameters.

The next step during the modulator design is creation of the basic blocks in the CADENCE software and their model in MATLAB. Block diagram of the proposed modulator on hardware level is shown in Fig. 5.

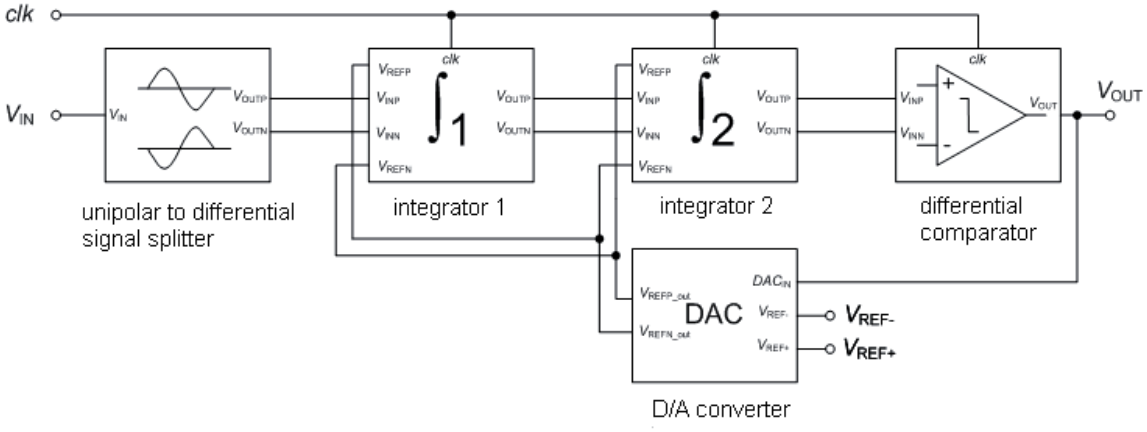


Fig. 5. Block scheme of the ΔΣ modulator.

Non-ideal properties of the basic blocks that should be taken into account in the modulator simulations are as follows: operational amplifier, switch, quantization circuit (comparator) and Digital to Analog Converter (DAC).

Block	Parameter	Initial value	Weight
1.Integrator	OpAmp gain	82 dB	1.9642
	OpAmp slew rate	18 V/μs	0.1043
	OpAmp bandwidth	22 MHz	0.8526
	OpAmp offset	8 μV	1.2732
2.Integrator	OpAmp gain	82 dB	0.7067
	OpAmp slew rate	18 V/μs	n.s.
	OpAmp bandwidth	22 MHz	n.s.
	OpAmp offset	8 μV	1.3514
ADC	Level error	1 mV	0.1941
	Hysteresis	1 mV	0.1040
DAC	Output level error (-5%/+10%)	2.5 V	5.0182

Tab. 3. Influence of the parameter change about -50 %/+100 % on modulator *SNR*.

The weights of the parameter change are written in Tab. 3. Data were obtained by equation

$$a = \frac{v_{+100\%} - v_{-50\%}}{v}.100 \quad [\%] \tag{5}$$

where a is a percentage weight of the property change and v represents value of the property. The DAC output level error has the highest influence on the modulator's *SNDR*. On the other hand, change of the slew rate and bandwidth of the second integrator operational amplifier has practically no influence on *SNDR*.

3.1 Operational Amplifier

The fully differential SC operational amplifier is used in the integrator. The simplified circuit diagram is shown in Fig. 6. Operational amplifier parameters were incorporated into the mathematical model implemented in MATLAB (see Fig. 7) after the proposal on the transistor level. Operational amplifier is characterized mainly by high-bandwidth (22 MHz), high slew rate (18 V/μs) and low input capacitance (800 fF).

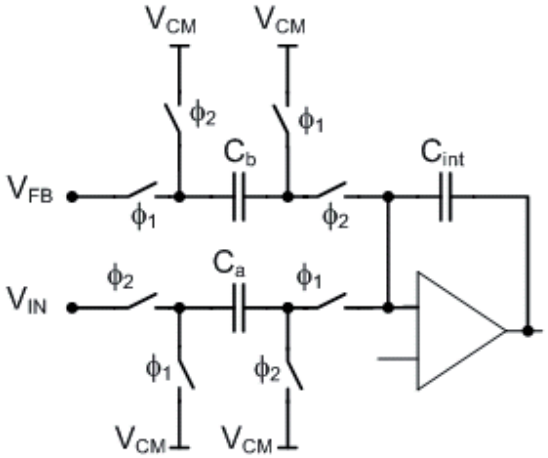


Fig. 6. Simplified circuitry of the used integrator.

3.2 Comparison of the Results

As should be expected, when the ideal model of the modulator was extended with operational amplifier and real switch properties, the achievable *SNR* was reduced to 86 dB at f_{BW} respectively to 79 dB at 1/3 f_{BW}. Graph comparing the ideal and achieved power spectral density is in Fig. 8.

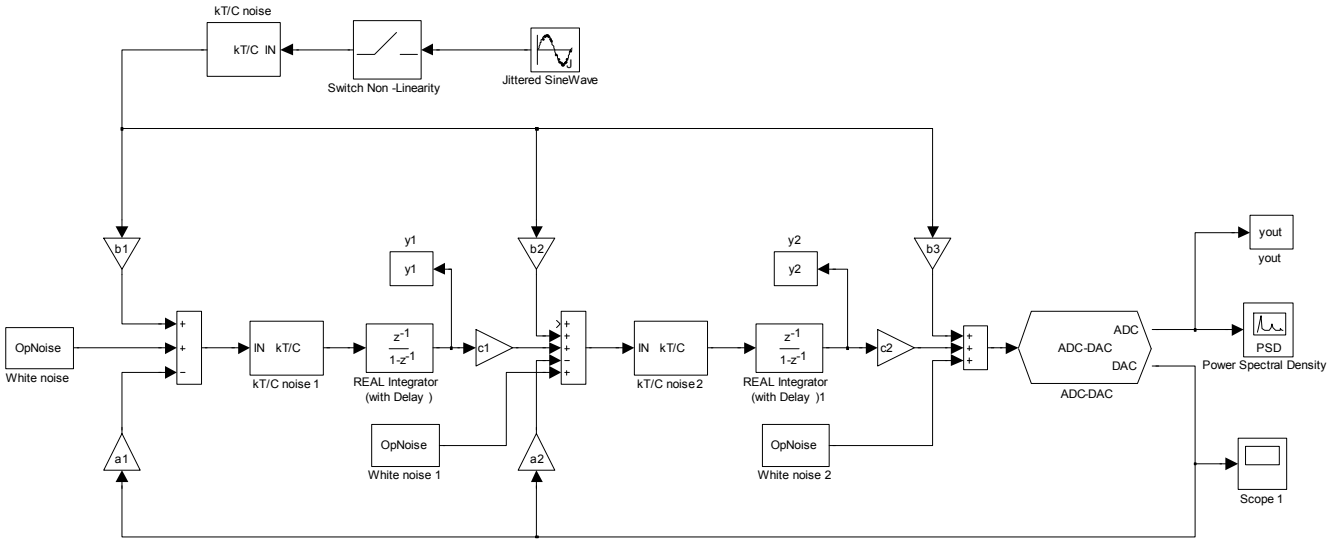


Fig. 7. Model of the second order ΔΣ modulator with component non-idealities in MATLAB SIMULINK.

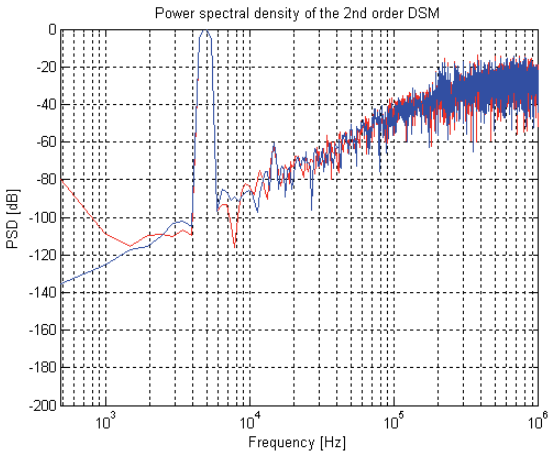


Fig. 8. Power spectral density of the second order ΣΔ modulator (ideal and designed).

4. Optimization of the Transfer Coefficients and Corner Analysis

Real properties of the ΔΣ modulator basic blocks change the modulator transfer function and final *SNDR*. However, thanks to knowledge of these properties the modulator transfer coefficients could be optimized.

Coefficient	Value
a_1	1
a_2	1
b_1	1
b_2	0
b_3	0
c_1	1.6
c_2	4

Tab. 4. Optimized values of the modulator coefficients.

It is possible to reach efficient noise modulation. However, it is sacrificed by maintaining of modulator stability. There are many ways to optimize the modulator transfer coefficients.

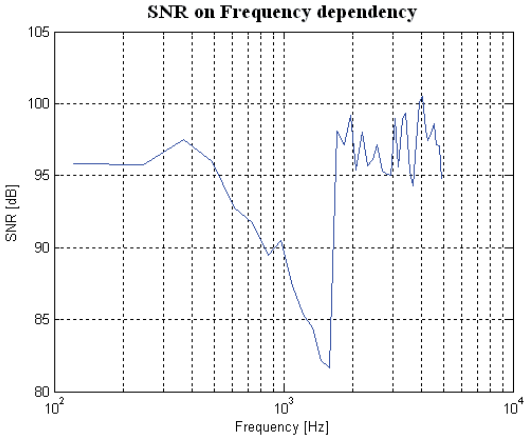


Fig. 9. *SNR* on signal frequency dependence (optimized coefficients values).

The neural network was used for transfer coefficients optimization. Values of the used transfer parameters are reported in Tab. 4. The previous figure shows that the modulator *SNDR* increased by 8.4 dB in comparison to real modulator with non-optimized transfer parameters.

4.1 Corner Analysis

When designing any type of circuit on the chip, especially analog, it's necessary to verify whether the resulting circuit implementation meets the requirements under all boundary conditions - temperature, substrate parameters, etc. The analysis result shows only difference at DC spectral line. First, it's appropriate to determine the worst case scenario for the chosen boundary conditions coefficients (see Tab. 1). We can determine the worst case configuration for further testing depending on the worst result of the corner analysis. This information saves a lot of time. It should be noted that at least 8 spectral lines in a band is required while spectral analysis is examined for adequate testing behavior throughout the modulator bandwidth. High value of the *OSR* leads to spectral analysis with high resolution necessity. It naturally leads to obtain large amounts of data and long time simulations.

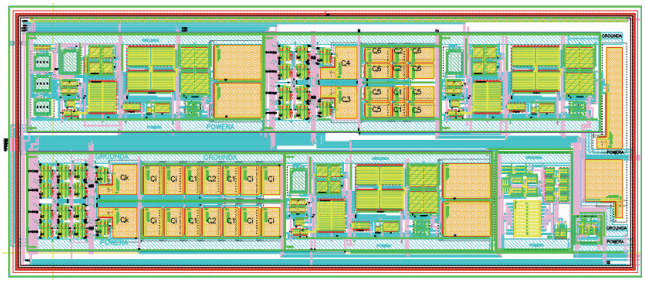


Fig. 10. Designed modulator topology.

Thanks to MATLAB model of the ΔΣ modulator accuracy the obtained value of the *SNDR* after post-simulation practically coincides with the simulation results from MATLAB.

5. Conclusion

The paper describes the design of the 12-bit ΔΣ modulator using switched capacitor technique. The ΔΣ modulator is utilized for vibration sensor output signal processing. The design is explained step by step from technology choice and modulator circumstance through simulation of the ideal modulator, design fundamental blocks on transistor level, design of the real modulator model to transfer coefficients optimization and final ΔΣ modulator parameter measurement. The ONSemiconductor I2T100 0.7 μm technology was used. Proposed ΔΣ modulator was simulated and simulation conditions were discussed as well. The final value of *SNDR* for the worst conditions reached 82.2 dB (ENOB = 13.4 bits). Die size of the modulator is 0.5 mm^2.

Acknowledgements

The research has been supported by the Czech Ministry of Education, Youth and Sports within the frame of the Research Plan MSM0021630503 MICROSYN, by the Czech Grant Agency as the project GA102/09/1628 Research and development of digitally controlled integrated mixed-mode circuits, as project Prospective applications of new sensor technologies and circuits for processing of sensor signals, No. FEKT-S-11-16 and by the Ministry of Industry and Trade of the Czech Republic under the MPO 2A-1TP1/143. Special thanks to CADENCE because CADENCE software was used with support through the CADENCE Academic Network.

References

[1] Viditech, http://www.viditech.cz

[2] Wilcoxon Research, accelerometers and vibration sensors http://www.wilcoxon.com/

[3] IMI SENSORS, http://www.imi-sensors.com/

[4] SKF, Vibration Sensors, http://www.skf.com/files/268580.pdf

[5] GORDON, D., SCHMIDTKE, H. R., BEIGL, M., ZENGEN, G. A novel micro-vibration sensor for activity recognition*:* Potential and limitations. In *International Symposium on Wearable Computers 2010*. Seoul (South Korea), 2010, p. 1 – 8.

[6] MALOBERTI, F., *Data Converters*. Dordrecht: Springer, 2007.

[7] PLASHE, R. *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*. Broadcom, Irvine, CA: Kluwer Academic Publishers, 2003.

[8] BOURDOPOULOS, G. I., PNEVMATIKAKIS, A., ANASTASSOPOULOS, V., DELIYANNIS, T. I. *Delta-Sigma Modulators (Modelling, Design and Applications)*. London: Imperial College Press, 2003.

[9] NORSWORTHY, S. R., SHREIER, R., TEMES, G. C. *Delta-Sigma Data Converters*. Piscataway (NJ): IEEE Press, 1997.

[10] GEERTS, Y., STEYAERT, M., SANSEN, W. M. C. *Design of Multi-Bit Delta-Sigma A/D Converters*. The Springer International Series in Engineering and Computer Science, vol. 686, 2002.

[11] STESSMAN, N. J., VINNAKOTA, B., HARJANI, R. System-level design for test of fully differential analog circuits. *IEEE Journal of Solid-State Circuits,* 1996, vol. 31, no. 10, p. 1526 to 1534.

[12] NICOLLINI, G., CONFALONIERI, P., SENDEROWICZ, D. A fully differential sample-and-hold circuit for high-speed applications. *IEEE Journal of Solid-State Circuits,* Oct 1989, vol. 24, no. 5, p. 1461- 1465.

[13] ALI, S., TANNER, S., FARINE, P.A. A novel 1V, 24µW, ΣΔ modulator using Amplifier & Comparator Based Switched Capacitor technique, with 10-kHz bandwidth and 64dB SNDR. In *17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2010).* Athens (Greece), Dec 2010, p. 1124-1127.

[14] TORKZADEH, P., JAVIDAN, J., ATARODI, M. A 640MHz CMOS switched-capacitor sigma-delta ADC with 12 bits of resolution by using double sampling technique. In *4th IEEE International Conference on Circuits and Systems for Communications (ICCSC 2008).* Shanghai, May 2008, p. 572-575.

[15] CHUN-KIT CHEUNG, SIEW-CHONG TAN, LAI, Y. M., TSE, C.K. A new visit to an old problem in switched-capacitor converters. In *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS).* Paris (France), 2010, p. 3192 to 3195.

[16] KUBAŘ, M., ŠUBRT, O., JAKOVENKO, J., MARTINEK, P. Versatile engine for virtual testing of ADC/DAC non-linearity. In *The International Workshop on Symbolic and Numerical Methods, Modelling and Applications to Circuit Design 2010*. Tunis: IEEE - Tunisia, 2010, ISBN 978-1-4244-6815-7.

[17] KUBAŘ, M., ŠUBRT, O., MARTINEK, P., JAKOVENKO, J. Experience in virtual testing of RSD cyclic A/D converters. In *Proc. of 12th IEEE Design and Diagnostics of Electronic Circuits and Systems Workshop 2009 (DDECS'09)*. Los Alamitos: IEEE Computer Society Press, 2009, p. 178-181. ISBN 978-1-4244-3339-1.

[18] BOUŘA, A., HUSÁK, M., KULHA, P. NMOS and PMOS translinear multiplying cell for current-mode signal processing. In *ASDAM 2008 Conference Proceedings*. Bratislava: Slovak University of Technology, 2008.

About Authors ...

Michal PAVLIK was born in Trebic. He received MSc., and Ph.D. degrees at the University of Technology, Faculty of Electrical Engineering and Communication, Department of Microelectronics, Brno, Czech Republic, in 2005 and 2009, respectively. Now he is working as senior lecturer at the same institution. His research is in the field of integrated circuit design, where his interests include analog and mixed-mode integrated circuits design and simulations, signal processing and system testing.

Vilem KLEDROWETZ passed bachelor study branch Microelectronics and technology and master degree branch Microelectronics at the Faculty of Electrical Engineering and Communication. The topic of his diploma thesis is *The influence of MDAC resolution on basic blocks of pipelined AD converter*. Nowadays he studies third year of doctoral degree branch Microelectronics, he is mainly focused on design of analog integrated circuits and AD/DA converters. He passed the profession internship in ON Design Czech s.r.o. during 2008 and 2009.

Jiri HAZE was born in Nachod. He received MSc., Ph.D. and Ass. Prof. degrees at the University of Technology, Faculty of Electrical Engineering and Communication, Department of Microelectronics, Brno, Czech Republic, in 2002, 2005 and 2009, respectively. Now he is working as associated professor at the same institution. His research is in the field of integrated circuit design, where his interests include analog and mixed-mode integrated circuits design, signal processing and sensor application.