High Input Impedance Voltage-Mode Universal Biquadratic Filters with Three Inputs Using Three CCs and Grounding Capacitors

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Abstract. Two current conveyors (CCs) based high input impedance voltage-mode universal biquadratic filters each with three input terminals and one output terminal are presented. The first circuit is composed of three differential voltage current conveyors (DVCCs), two grounded capacitors and four resistors. The second circuit is composed of two DVCCs, one differential difference current conveyor (DDCC), two grounded capacitors and four grounded resistors. The proposed circuits can realize all the standard filter functions, namely, lowpass, bandpass, highpass, notch and allpass filters by the selections of different input voltage terminals. The proposed circuits offer the features of high input impedance, using only grounded capacitors and low active and passive sensitivities. Moreover, the x ports of the DVCCs (or DDCC) in the proposed circuits are connected directly to resistors. This design offers the feature of a direct incorporation of the parasitic resistance at the x terminal of the DVCC (DDCC), $R_x$, as a part of the main resistance.

Keywords
Current conveyor, biquadratic filter, active circuit.

1. Introduction

The differential difference current conveyors (DDCC) [1] or differential voltage current conveyors (DVCC) [2] have received considerable attention due to they enjoy the advantages of second-generation current conveyor (CCII) and differential difference amplifier (DDA) such as larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry, low power-consumption, and arithmetic operation capability. Moreover, it has two or three high input impedance voltage terminals (y terminals) that make easy to synthesize circuits.

The circuit design uses only grounded capacitors is attractive, because grounded capacitor can be implemented on a smaller area than the floating counterpart and it can absorb equivalent shunt capacitive parasitic [3], [4]. High input impedance voltage-mode active filters are of great interest because several cells of this kind can be directly connected in cascade to implement higher order filters [5], [6]. Because the DVCC (or DDCC) has a non-negligible resistance on port x ($R_x$) [7], when the x port of DVCC is loaded by a capacitor, it leads to improper transfer functions. Due to the effect of this parasitic resistance $R_x$ at the x port of DVCC, the filters with x port loaded by a capacitor do not exhibit good performance at high frequency.

Several voltage-mode universal biquads each with three input terminals were presented in [8]-[19]. Five kinds of standard filter functions can be derived by the selections of different input voltage terminals in these circuits. However, these circuits suffer from one or more of the following drawbacks:

- use floating capacitors [8], [10], [11], [14]-[16], [18], [19],
- need more active components for the unity gain inverting inputs in some filter realizations [8], [10], [15], [18], [19],
- low input impedance [9], [10], [13]-[16], [18], [19],
- the resonance angular frequency and quality factor cannot be orthogonally controllable [8]-[12], [14]-[16], [18], [19],
- the x ports of the current conveyors are not connected directly to resistors [8], [10], [11], [15],
- use too many active and passive components [17].

In 2000, Minaei and Yuce [20] presented a DVCC based voltage-mode universal biquad with three input terminals. This circuit uses two grounded capacitors, three grounded resistors and three DVCCs.

In this paper, two new high input impedance voltage-mode universal biquadratic filters each with three input terminals using three DVCCs (or DDCC) is presented. Each of the proposed circuits uses four resistors and two grounded capacitors. The proposed circuits have the following features: (i) five standard filter functions, that is, highpass, bandpass, lowpass, notch, and allpass filters can
be obtained from the same circuit configuration, (ii) high input impedance, (iii) low active and passive sensitivities, and (iv) the x ports of the DVCCs (or DDCC) are connected directly to resistors.

2. The Proposed Biquadratic Filters

Using standard notation, the port relations of a DVCC can be described by the following matrix equation [2]:

\[
\begin{bmatrix}
i_{y1} \\
i_{y2} \\
v_y \\
i_z
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
1 & -1 & 0 & 0 \\
0 & 0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
v_{y1} \\
v_{y2} \\
0 \\
v_z
\end{bmatrix}.
\]

(1)

where the plus and minus signs indicate whether the DVCC is configured as a non-inverting or inverting circuit, termed DVCC⁺ or DVCC⁻.

Using standard notation, the port relations of a DDCC can be described by the following matrix equation [1]:

\[
\begin{bmatrix}
i_{y1} \\
i_{y2} \\
i_{y3} \\
v_y \\
i_z
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
1 & -1 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 & 0
\end{bmatrix}
\begin{bmatrix}
v_{y1} \\
v_{y2} \\
v_{y3} \\
i_y \\
v_z
\end{bmatrix}.
\]

(2)

where the plus and minus signs indicate whether the DDCC is configured as a non-inverting or inverting circuit, termed DDCC⁺ or DDCC⁻.

Considering the first proposed circuit in Fig. 1, the output voltage can be expressed as

\[
V_{out} = \frac{s^2C_1C_2G_1V_{in3} - sC_1G_2G_3V_{in2} + G_1G_3G_4V_{in1}}{s^2C_1C_2G_1 + sC_1G_2G_4 + G_1G_2G_3}.
\]

(3)

From (3), we can see that:

- If \(V_{in2} = V_{in3} = 0\) (grounded), then \(V_{out} = V_{in1}\), a lowpass filter can be obtained with \(V_{out}/V_{in1}\).
- If \(V_{in1} = 0\) (grounded), then \(V_{out} = V_{in3}\), a highpass filter can be obtained with \(V_{out}/V_{in3}\).
- If \(V_{in2} = 0\) (grounded), then \(V_{out} = V_{in1}\), a notch filter can be obtained with \(V_{out}/V_{in1}\).
- If \(V_{in1} = V_{in2} = V_{in3} = V_{in}\) = input voltage signal and let \(R_2 = R_3 = R_4\), an allpass filter can be obtained with \(V_{out}/V_{in}\).

The resonance angular frequency \(\omega_0\) and the quality factor \(Q\) are given by

\[
\omega_0 = \frac{G_1G_2G_3}{C_1C_2G_4}
\]

(4)

and

\[
Q = \frac{C_1G_2G_3}{C_1G_2G_4}.
\]

(5)

Thus, all the standard filter functions (highpass, bandpass, lowpass, notch, and allpass) can be obtained from the proposed circuit in Fig. 1. Due to the three input signals, \(V_{in1}, V_{in2}\) and \(V_{in3}\) are connected directly to the high input impedance input nodes of the three DVCCs (the y port of the DVCC), respectively, the circuit enjoys the feature of high input impedance. The proposed circuit uses only two grounded capacitors, which are attractive for integrated circuit implementation.

Considering the second proposed circuit in Fig. 2, the output voltage can be expressed as

\[
V_{out} = \frac{(s^2C_1C_2G_1 + G_1G_2G_3)V_{in3} - sC_1G_2G_3V_{in2}}{s^2C_1C_2G_1 + sC_1G_2G_4 + G_1G_2G_3}.
\]

(6)
From (6), we can see that:

- If $V_{in2} = V_{in3} = 0$ (grounded), then $V_{in1} =$ input voltage signal, a lowpass filter can be obtained with $V_{out}/V_{in1}$.

- If $V_{in1} = V_{in3} = 0$ (grounded), then $V_{in2} =$ input voltage signal, a bandpass filter can be obtained with $V_{out}/V_{in2}$.

- If $V_{in1} = V_{in2} = 0$ (grounded), then $V_{in3} =$ input voltage signal, a notch filter can be obtained with $V_{out}/V_{in3}$.

- If $V_{in2} = 0$ (grounded), then $V_{in1} = V_{in3} = V_{in} =$ input voltage signal, a highpass filter can be obtained with $V_{out}/V_{in}$.

- If $V_{in1} = 0$ (grounded), then $V_{in2} = V_{in3} = V_{in} =$ input voltage signal and let $R_1 = R_4$, an allpass filter can be obtained with $V_{out}/V_{in}$.

The resonance angular frequency $\omega_o$ and the quality factor $Q$ are given by

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}}, \quad (7)$$

and

$$Q = \frac{G_4}{G_3} \sqrt{\frac{C_1 G_1}{C_2 G_2}}. \quad (8)$$

Thus, all the standard filter functions (highpass, bandpass, lowpass, notch, and allpass) can be obtained from the proposed circuit in Fig. 2. Due to the three input signals, $V_{in1}$, $V_{in2}$ and $V_{in3}$ are connected directly to the high input impedance input nodes of the DVCCs or DDCC (the y port of the DVCCs or DDCC), respectively, the circuit enjoys the feature of high input impedance. This circuit uses only grounded capacitors and resistors, which are attractive for integrated circuit implementation. From (7), (8), the resonance angular frequency can be controlled by $R_1$ or $R_2$. The quality factor can be independently controlled by $R_3$ or $R_4$.

From Fig. 1 and Fig. 2, the three resistors $R_1$, $R_2$, $R_3$ are connected to the three x terminals of the three DVCCs (or DDCC), respectively. This design offers the feature of a direct incorporation of the parasitic resistance at the x terminal of the DVCC (DDCC), $R_x$, as a part of the main resistance. Since the output impedances of the proposed circuits are not small, voltage followers are needed while cascaded the proposed circuits to the next stages.

### 3. Sensitivities Analysis

Taking the non-idealities of the DVCC or DDCC into account, the relationship of the terminal voltages and currents of DVCC can be rewritten as

$$[i_{y1} \ i_{y2} \ v_y \ i_y] = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \ 0 & 0 & 0 & 0 & 0 \ \alpha_{i1}(s) - \alpha_{i2}(s) & 0 & 0 & 0 \ 0 & 0 & \pm \beta_i(s) & 0 \end{bmatrix} [v_{y1} \ v_{y2} \ v_y \ i_y] \quad (9)$$

The relationship of the terminal voltages and currents of DDCC can be rewritten as

$$[i_{y1} \ i_{y2} \ v_y \ i_y] = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \ 0 & 0 & 0 & 0 & 0 \ \alpha_{i1}(s) - \alpha_{i2}(s) & 0 & 0 & 0 \ 0 & 0 & \pm \beta_i(s) & 0 \end{bmatrix} [v_{y1} \ v_{y2} \ v_y \ i_y] \quad (10)$$

where $\alpha_{i1}(s)$, $\alpha_{i2}(s)$ and $\alpha_{i3}(s)$ represent the frequency transfer functions of the internal voltage followers and $\beta_i(s)$ represent the frequency transfer function of the internal current follower of the k-th DDCC (or DVCC). They can be approximated by first order lowpass functions, which can be considered to have a unity value for frequencies much lower than their corner frequencies [21]. If the circuit is working at frequencies much lower than the corner frequencies of $\alpha_{i1}(s)$, $\alpha_{i2}(s)$, $\alpha_{i3}(s)$ and $\beta_i(s)$, then $\alpha_{i1}(s) = \alpha_{i1} = 1 - \alpha_{i1}$, and $\alpha_{i3}(s) = \alpha_{i3}$ (so $\alpha_{i3} = 0$) denotes the voltage tracking error from $y_1$ terminal to x terminal of the k-th DDCC (or DVCC), $\alpha_{i2}(s) = \alpha_{i2} = 1 - \alpha_{i2}$ and $\alpha_{i3}(s) = \alpha_{i3} = 0$ (so $\alpha_{i3} = 0$) denotes the voltage tracking error from $y_2$ terminal to x terminal of the k-th DDCC (or DVCC), $\alpha_{i3}(s) = \alpha_{i3} = 1 - \alpha_{i3}$, and $\alpha_{i3}(s) = \alpha_{i3} = 1$ (so $\alpha_{i3} = 1$) denotes the voltage tracking error from $y_3$ terminal to x terminal of the k-th DDCC (or DVCC). The denominator of the non-ideal voltage transfer function for Fig. 1 becomes

$$D(s) = s^2 C_1 C_2 G_4 + s C_1 G_4 G_5 + G_1 G_4 G_5 G_6 G_7 G_8 \alpha_{i1} \alpha_{i2} \beta_i \beta_i \beta_i \beta_i \beta_i. \quad (11)$$

The resonance angular frequency $\omega_o$ and quality factor $Q$ become

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2} \frac{C_1 G_1}{C_2 G_2}}, \quad (12)$$

$$Q = \sqrt{\frac{C_1 G_1}{C_2 G_2}}, \quad (13)$$

The active and passive sensitivities of $\omega_o$ and $Q$ are shown as

$$S_{\omega_o}^a G_{i1} G_{i2} G_{i3} G_{i4} G_{i5} G_{i6} G_{i7} G_{i8} = -S_{\omega_o}^a G_{i1} G_{i2} G_{i3} = \frac{1}{2};$$

$$S_Q^a G_{i1} G_{i2} G_{i3} G_{i4} G_{i5} G_{i6} G_{i7} G_{i8} = -S_Q^a G_{i1} G_{i2} G_{i3} = \frac{1}{2}. \quad (14)$$

The denominator of the non-ideal voltage transfer function for Fig. 2 becomes

$$D(s) = s^2 C_1 C_2 G_4 + s C_1 G_4 G_5 \alpha_{i1} \alpha_{i2} \beta_i \beta_i \beta_i + G_1 G_4 G_5 G_6 G_7 G_8 \alpha_{i1} \alpha_{i2} \beta_i \beta_i \beta_i \beta_i \beta_i \beta_i \beta_i \beta_i \beta_i \beta_i. \quad (14)$$

The resonance angular frequency $\omega_o$ and quality factor $Q$ become

$$\omega_o = \dots$$

$$Q = \dots$$

where $Q$ is the quality factor and $\omega_o$ is the resonance angular frequency.
\( \omega_0 = \sqrt{ \frac{G_1 G_2 \alpha_1 \alpha_2 \beta_1 \beta_2}{C_1 C_2} }, \) \hfill (15)

\( Q = \frac{G_4}{G_3 \alpha_2 \alpha_2 \beta_1} \sqrt{\frac{C_1 C_2 \alpha_2 \alpha_2 \beta_1}{C_1 C_2 \beta_2}}. \) \hfill (16)

The active and passive sensitivities of \( \omega_0 \) and \( Q \) are shown as

\[ S_{\omega_0} = S_{\beta_1}^{-1} = \frac{1}{2}; \]

\[ S_{\beta_2} = S_{\beta_2}^{-1} = \frac{1}{2}; \]

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All the active and passive sensitivities of Fig. 1 and Fig. 2 are small.

4. Simulation Results

HSPICE simulations were carried out to demonstrate the feasibility of the proposed circuits in Fig. 1 and Fig. 2. The DDCC was realized by the CMOS implementation of Elwan and Soliman [21] (by ungrounding the gate of MOSFET M2 and treating this as the third \(-y\)-input \( y_3 \)) and is redrawn in Fig. 3.

![Fig. 3. The CMOS realization of the DDCC.](image)

The DVCC was realized from Fig. 3 by grounding the gate of MOSFET M2. The simulations use 0.18 \( \mu \)m, level 49 MOSFET from TSMC (Taiwan Semiconductor Manufacturing Company, Ltd.). The supply voltages are \( V_+ = +1.25 \text{ V}, \ V_- = -1.25 \text{ V} \) and \( V_{b1} = -0.45 \text{ V} \). The dimensions of the NMOS transistors in the DDCC are set to be \( W = 4.5 \text{ \( \mu \)m} \) and \( L = 0.9 \text{ \( \mu \)m} \). The dimensions of the PMOS transistors in the DDCC are set to be \( W = 9 \text{ \( \mu \)m} \) and \( L = 0.9 \text{ \( \mu \)m} \).

Fig. 4 represents the simulated frequency responses for the lowpass filter of Fig. 1 designed with \( V_{a1} = V_{a2} = 0 \) (grounded), \( V_{a3} = V_{a3} \) = input voltage signal, \( Q = 1 \) and \( f_o = 1.5915 \text{ MHz} \): \( C_1 = C_2 = 10 \text{ pF} \) and \( R_1 = R_2 = R_3 = R_4 = 10 \text{ k\( \Omega \)} \). Fig. 5 represents the simulated frequency responses for the bandpass filter of Fig. 1 designed with \( V_{a1} = V_{a2} = 0 \) (grounded), \( V_{a3} = V_{a3} \) = input voltage signal, \( Q = 1 \) and \( f_o = 1.5915 \text{ MHz} \): \( C_1 = C_2 = 10 \text{ pF} \) and \( R_1 = R_2 = R_3 = R_4 = 10 \text{ k\( \Omega \)} \). Fig. 6 represents the simulated frequency responses for the highpass filter of Fig. 1 designed with \( V_{a1} = V_{a2} = 0 \) (grounded), \( V_{a3} = V_{a3} \) = input voltage signal, \( Q = 1 \) and \( f_o = 1.5915 \text{ MHz} \): \( C_1 = C_2 = 10 \text{ pF} \) and \( R_1 = R_2 = R_3 = R_4 = 10 \text{ k\( \Omega \)} \). The power dissipation of this allpass filter is 4.266 mW.

Fig. 9 represents the simulated frequency responses for the notch filter of Fig. 2 designed with \( V_{a1} = V_{a2} = 0 \) (grounded), \( V_{a3} = V_{a3} \) = input voltage signal, \( Q = 1 \) and \( f_o = 1.5915 \text{ MHz} \): \( C_1 = C_2 = 10 \text{ pF} \) and \( R_1 = R_2 = R_3 = R_4 = 10 \text{ k\( \Omega \)} \).
Fig. 4. Simulation results for the lowpass filter of Fig. 1 with $V_{in1} = V_{in3} = 0$ (grounded), $V_{in2} = V_{in}$.

Fig. 5. Simulation results for the bandpass filter of Fig. 1 with $V_{in1} = V_{in3} = 0$ (grounded), $V_{in2} = V_{in}$.

Fig. 6. Simulation results for the highpass filter of Fig. 1 with $V_{in1} = V_{in2} = 0$ (grounded), $V_{in3} = V_{in}$.

Fig. 7. Simulation results for the notch filter of Fig. 1 with $V_{in2} = 0$ (grounded), $V_{in1} = V_{in3} = V_{in}$.

Fig. 8. Simulation results for the allpass filter of Fig. 1 with $V_{in1} = V_{in2} = V_{in3} = V_{in}$.

Fig. 9. Simulation results for the notch filter of Fig. 2 with $V_{in1} = V_{in2} = 0$ (grounded), $V_{in3} = V_{in}$.
Fig. 10. Simulation results for the bandpass filter of Fig. 2 with $V_{in1} = V_{in3} = 0$ (grounded), $V_{in2} = V_{in}$. 10 kΩ. Fig. 11 represents the simulated frequency responses for the lowpass filter of Fig. 2 designed with $V_{in2} = V_{in3} = 0$ (grounded), $V_{in1} = V_{in} = V_{in}$ input voltage signal, $Q = 1$ and $f_o = 1.5915$ MHz; $C_1 = C_2 = 10$ pF and $R_1 = R_2 = R_3 = R_4 = 10$ kΩ. Fig. 12 represents the simulated frequency responses for the highpass filter of Fig. 2 designed with $V_{in2} = 0$ (grounded), $V_{in1} = V_{in3} = V_{in} = V_{in}$ input voltage signal, $Q = 1$ and $f_o = 1.5915$ MHz; $C_1 = C_2 = 10$ pF and $R_1 = R_2 = R_3 = R_4 = 10$ kΩ. Fig. 13 represents the simulated frequency responses for the allpass filter of Fig. 2 designed with $V_{in2} = 0$ (grounded), $V_{in1} = V_{in3} = V_{in} = V_{in}$ input voltage signal, $Q = 1$ and $f_o = 1.5915$ MHz; $C_1 = C_2 = 10$ pF and $R_1 = R_2 = R_3 = R_4 = 10$ kΩ. The power dissipation of this allpass filter is 4.2617 mW. Fig. 14 represents the simulated frequency responses for the bandpass filter of Fig. 2 as the resistor $R_3$ in $Q$ is varied with $V_{in1} = V_{in3} = 0$ (grounded), $V_{in2} = V_{in} = V_{in}$ input voltage signal, $C_1 = C_2 = 10$ pF, $R_1 = R_2 = 10$ kΩ and $R_4 = 25$ kΩ. All the simulation results are coherent and support the theoretical analyses.
5. Conclusion

In this paper, two new high input impedance voltage-mode universal biquadratic filters each with three input terminals are presented. The proposed circuits use three DVCCs (or DDCC), four resistors and two grounded capacitors and offers the following advantages: high input impedance, the use of only grounded capacitors, the versatility to synthesize lowpass, bandpass, highpass, notch, and allpass responses, does not need voltage inverter to realize the allpass response, low active and passive sensitivities, and direct incorporation of the parasitic resistance at the x terminal of the CC as a part of the main resistance.

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References


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