Voltage-Mode Highpass, Bandpass, Lowpass and Notch Biquadratic Filters Using Single DDCC

Wei-Yuan CHIU, Jiun-Wei HORNG

Dept. of Electronic Engineering, Chung Yuan Christian University, Chung-Li, 32023, Taiwan

jwhorng@cycu.edu.tw

Abstract. *A new voltage-mode multifunction biquadratic filter using one differential difference current conveyor (DDCC), two grounded capacitors and three resistors is presented. The proposed circuit offers the following attractive advantages: realizing highpass, bandpass, lowpass and notch filter functions, simultaneously, from the same circuit configuration; employing grounded capacitors, which is ideal for integration and simpler circuit configuration.*

Keywords

Active filters, current conveyors, analog signal processing.

1. Introduction

The operational amplifier (OP AMP) has traditionally played an important role in the design of active filters. However, the OP AMP-based circuit often suffers from the limited bandwidth and slew-rate. Recently, the current conveyors have received great attention due to higher signal bandwidth, wider dynamic range, greater linearity, lower power consumption, and simpler circuitry with respect to the voltage-mode OP AMP [1], [2].

To obtain various filter functions simultaneously in the same circuit topology will increase the usability and reduce the cost of the circuit. For this reason, a large number of multifunction biquadratic filters were proposed based on current conveyors. Some multifunction biquadratic filters with single input and three outputs that can realize highpass, bandpass and lowpass filters, simultaneously, were proposed in [3]–[7]. However the circuit configurations in [3], [4] required at least three active components. Some two active components highpass, bandpass and lowpass filters were proposed in [5]–[7]. However, the active components they used were not minimum. From the point of view of power dissipation, it is beneficial to keep the number of the active elements as small as possible. Several voltage-mode biquadratic filters using one active component were proposed in [8]-[14]. However, only three standard filter functions at most can be simultaneously obtained in each circuit realization.

A voltage-mode biquadratic filter with single input and four outputs using single fully differential current conveyor (FDCCII) was presented in Chen [15]. However, the active component (FDCCII) used in this circuit is a very complicate device. On each FDCCII there are almost twice as many MOSs as the differential difference current conveyor (DDCC) needs. Moreover, a FDCCII is equivalent to two DDCCs arithmetically in fact.

Several current-mode biquadratic filters were proposed in [16], [17]. The current-mode filters can be transferred to voltage-mode by adding voltage to current and current to voltage converters. The current-mode biquad in [16] can realize four kinds of standard filter functions, simultaneously, with one input and four outputs using four operational transconductance amplifiers (OTAs) and two grounded capacitors. The current-mode biquad in [17] can realize five kinds of standard filter functions with three inputs and one output using one current controlled current differencing transconductance amplifier (CCCDTA) and two grounded capacitors. For those applications that voltage-mode filters are required, because current-mode filters need other active devices to change the current-mode signals into voltage-mode, the use of additional active devices will add parasitic capacitors and resistors into the main circuit, which will degrade the performance of these circuits.

In this paper, a new voltage-mode multifunction biquadratic filter using one DDCC, two grounded capacitors and three resistors is presented. The proposed circuit can realize voltage-mode highpass, bandpass, lowpass and notch filter transfer functions, simultaneously. With respect to the previous multifunction biquadratic filters in [3]–[14], at least one more standard filter function can be simultaneously obtained from the proposed circuit. The proposed circuit uses grounded capacitors that are attractive for integrated circuit implementation [18].

2. Proposed Circuits

The DDCC was proposed in 1996, and it enjoys the advantages of second-generation current conveyor (CCII) and differential difference amplifier (DDA) such as larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry, high input impedance and arithmetic

operation capability [19]. Using standard notation, the port relations of an ideal DDCC can be characterized by

$$\begin{bmatrix} V_x \\ I_{y_1} \\ I_{y_2} \\ I_{y_3} \\ I_{z1} \\ \dots \\ I_{zk} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 \\ \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \pm 1 \end{bmatrix} \begin{bmatrix} V_{y_1} \\ V_{y_2} \\ V_{y_3} \\ I_x \end{bmatrix} \quad (1)$$

where the plus and minus signs indicate whether the z terminal is configured as a non-inverting or inverting type.

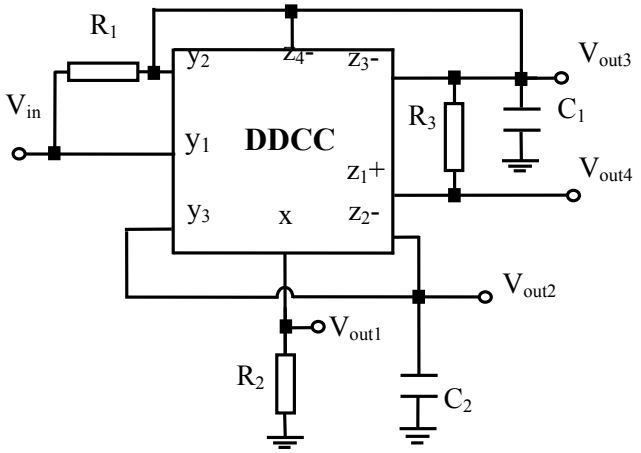


Fig. 1. The proposed voltage-mode highpass, bandpass, lowpass and notch biquadratic filter using single DDCC.

The proposed circuit configuration is shown in Fig. 1. The transfer functions can be expressed as:

$$\frac{V_{out1}}{V_{in}} = \frac{s^2 C_1 C_2}{s^2 C_1 C_2 + s\left[C_2(G_1 - G_2) + C_1 G_2\right] + G_1 G_2}, \quad (2)$$

$$\frac{V_{out2}}{V_{in}} = \frac{-sC_1 G_2}{s^2 C_1 C_2 + s\left[C_2(G_1 - G_2) + C_1 G_2\right] + G_1 G_2}, \quad (3)$$

$$\frac{V_{out3}}{V_{in}} = \frac{sC_2(G_1 - G_2) + G_1 G_2}{s^2 C_1 C_2 + s\left[C_2(G_1 - G_2) + C_1 G_2\right] + G_1 G_2}, \quad (4)$$

$$\frac{V_{out4}}{V_{in}} = \frac{s^2 C_1 C_2 \frac{G_2}{G_3} + sC_2(G_1 - G_2) + G_1 G_2}{s^2 C_1 C_2 + s\left[C_2(G_1 - G_2) + C_1 G_2\right] + G_1 G_2}. \quad (5)$$

From (2)–(3), it can be seen that a highpass response is obtained from V_{out1}, and a bandpass response is obtained from V_{out2}. From (4), a lowpass response is obtained from V_{out3} when $G_1 = G_2$. From (5), a notch response is obtained from V_{out4} when $G_1 = G_2$.

The resonance angular frequency ω_o and the quality factor Q are obtained by

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \quad (6)$$

and

$$Q = \frac{\sqrt{C_1 C_2 G_1 G_2}}{C_2(G_1 - G_2) + C_1 G_2}. \quad (7)$$

Thus, the proposed circuit can realize voltage-mode highpass, bandpass, lowpass and notch filter transfer functions, simultaneously, by employing only a single DDCC, two grounded capacitors and three resistors. The use of only grounded capacitors makes the proposed circuit ideal for integrated circuit implementation [18]. The proposed circuit is simpler than the previous one input and three outputs filters in [3]-[7] due to the use of only single active component. With respect to the previous multifunction biquadratic filters in [3]–[14], at least one more standard filter function can be simultaneously obtained from the proposed circuit. Voltage followers may be needed at output terminals of the proposed circuit to buffer the outputs and avoid the effects of load capacitances or resistances changing the responses of the filters. The lowpass and notch filters in the proposed circuit need components matching condition, one possible design equations for specified ω_o and Q can be obtained by:

$$\begin{cases} C_2 = Q^2 C_1 \\ R_1 = R_2 = \dfrac{1}{C_1 \omega_o Q} \end{cases} \quad (8)$$

3. Sensitivities Analysis

Taking the non-idealities of the DDCC into account, the relationship of the terminal voltages and currents can be rewritten as

$$\begin{bmatrix} V_x \\ I_{y_1} \\ I_{y_2} \\ I_{y_3} \\ I_{z1} \\ \dots \\ I_{zk} \end{bmatrix} = \begin{bmatrix} \alpha_1 & -\alpha_2 & \alpha_3 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm\beta_1 \\ \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \pm\beta_k \end{bmatrix} \begin{bmatrix} V_{y_1} \\ V_{y_2} \\ V_{y_3} \\ I_x \end{bmatrix} \quad (9)$$

where $\alpha_1 = 1 - \varepsilon_{1v}$ and ε_{1v} ($|\varepsilon_{1v}| << 1$) denotes the voltage tracking error from V_{y1} terminal to V_x terminal, $\alpha_2 = 1 - \varepsilon_{2v}$ and ε_{2v} ($|\varepsilon_{2v}| << 1$) denotes the voltage tracking error from V_{y2} terminal to V_x terminal, $\alpha_3 = 1 - \varepsilon_{3v}$ and ε_{3v} ($|\varepsilon_{3v}| << 1$) denotes the voltage tracking error from V_{y3} terminal to V_x terminal and $\beta_k = 1 - \varepsilon_i$ and ε_i ($|\varepsilon_i| << 1$) denotes the current tracking error from V_x terminal to the I_{zk} terminal of the DDCC. The denominator of non-ideal voltage transfer function in Fig. 1 becomes

$$D(s) = s^2 C_1 C_2 + sC_2\left[G_1 + G_2\alpha_2(\beta_1 - \beta_3 - \beta_4)\right] + sC_1 G_2 \alpha_3 \beta_2 + G_1 G_2 \alpha_3 \beta_2 \quad (10)$$

The resonance angular frequency ω_o and quality factor Q are obtained by

$$\omega_o = \sqrt{\frac{G_1 G_2 \alpha_3 \beta_2}{C_1 C_2}}, \tag{11}$$

$$Q = \frac{\sqrt{C_1 C_2 G_1 G_2 \alpha_3 \beta_2}}{C_2\left[G_1 + G_2\alpha_2\left(\beta_1 - \beta_3 - \beta_4\right)\right] + C_1 G_2 \alpha_3 \beta_2}. \tag{12}$$

The passive and active sensitivities of ω_o and Q are shown as

$$S_{\alpha_3,\beta_2}^{\omega_o} = \frac{1}{2},\quad S_{G_1,G_2}^{\omega_o} = -S_{C_1,C_2}^{\omega_o} = \frac{1}{2},$$

$$S_{C_1}^{Q} = S_{\alpha_3,\beta_2}^{Q} = \frac{1}{2} - \frac{C_1 G_2 \alpha_3 \beta_2}{\Delta},$$

$$S_{C_2}^{Q} = \frac{1}{2} - \frac{C_2\left[G_1 + G_2\alpha_2\left(\beta_1 - \beta_3 - \beta_4\right)\right]}{\Delta},$$

$$S_{G_1}^{Q} = \frac{1}{2} - \frac{C_2 G_1}{\Delta},$$

$$S_{G_2}^{Q} = \frac{1}{2} - \frac{C_2 G_2 \alpha_2\left(\beta_1 - \beta_3 - \beta_4\right) + C_1 G_2 \alpha_3 \beta_2}{\Delta},$$

$$S_{\alpha_2}^{Q} = -\frac{C_2 G_2 \alpha_2\left(\beta_1 - \beta_3 - \beta_4\right)}{\Delta},$$

$$S_{\beta_1}^{Q} = -\frac{C_2 G_2 \alpha_2 \beta_1}{\Delta},\quad S_{\beta_3}^{Q} = \frac{C_2 G_2 \alpha_2 \beta_3}{\Delta},$$

$$S_{\beta_4}^{Q} = \frac{C_2 G_2 \alpha_2 \beta_4}{\Delta},$$

$$\Delta = C_2\left[G_1 + G_2\alpha_2\left(\beta_1 - \beta_3 - \beta_4\right)\right] + C_1 G_2 \alpha_3 \beta_2.$$

All the active and passive sensitivities are less than unity when $G_1 = G_2$ and $C_2 \leq C_1$.

4. Effects of DDCC Parasitic

A non-ideal DDCC model is shown in Fig. 2 [20].

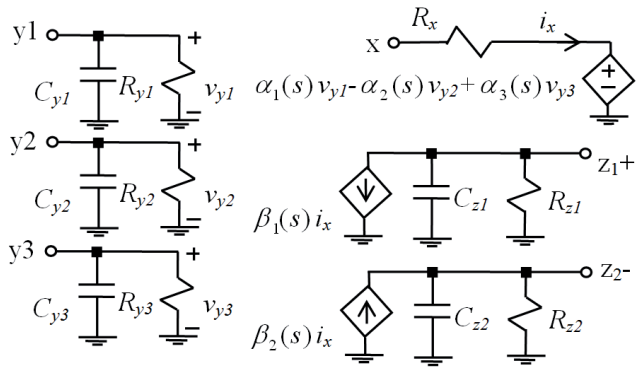


Fig. 2. The non-ideal DDCC model.

Taking into account the non-ideal DDCC and assuming the circuits are working at frequencies much less than the corner frequencies of $\alpha_i(s)$ and $\beta_j(s)$, namely, $\alpha_i \cong \beta_j \cong 1$. The transfer functions of Fig. 1 become

$$V_{out1} = (V_{in} - V_{out3} + V_{out2}) * \frac{R_2}{R_2 + R_x}, \tag{13}$$

$$\frac{V_{out2}}{V_{in}} = \frac{-s^2 C_1' C_{z1} G_2' + s a_{21} + a_{20}}{s^3 b_3 + s^2 b_2 + s b_1 + b_0}, \tag{14}$$

$$\frac{V_{out3}}{V_{in}} = \frac{s^2 C_2' C_{z1}(G_1 - 2G_2') + s a_{31} + a_{30}}{s^3 b_3 + s^2 b_2 + s b_1 + b_0}, \tag{15}$$

$$\frac{V_{out4}}{V_{in}} = \frac{s^2 C_1' C_2' G_2' + s a_{41} + a_{40}}{s^3 b_3 + s^2 b_2 + s b_1 + b_0} \tag{16}$$

where

$$C_1' = C_1 + C_{y2} + C_{z3} + C_{z4},$$

$$C_2' = C_2 + C_{y3} + C_{z2},$$

$$R_2' = R_2 + R_x,$$

$$G_{z2}' = G_{z2} + G_{y3},$$

$$G_{z3}' = G_{z3} + G_{z4} + G_{y2},$$

$$\begin{aligned} b_0 = {} & G_1 G_2'(G_3 + G_{z1}) + G_1 G_3 G_{z2}' \\ & + G_2' G_3(G_{z1} - G_{z2}' + G_{z3}') + G_1 G_{z1} G_{z2}' \\ & + G_2' G_{z1}(G_{z3}' - 2G_{z2}') + G_3 G_{z2}'(G_{z1} + G_{z3}') \\ & + G_{z1} G_{z2}' G_{z3}', \end{aligned}$$

$$\begin{aligned} b_1 = {} & C_1' G_2'(G_3 + G_{z1}) + C_1'(G_3 + G_{z1}) G_{z2}' \\ & + C_2' G_1(G_3 + G_{z1}) - C_2' G_2'(G_3 + 2G_{z1}) \\ & + C_2' G_3(G_{z1} + G_{z3}') + C_2' G_{z1} G_{z3}' \\ & + C_{z1} G_1(G_2' + G_{z2}') + C_{z1} G_2'(G_3 + G_{z3}' - 2G_{z2}') \\ & + C_{z1}(G_3 G_{z2}' + G_{z2}' G_{z3}'), \end{aligned}$$

$$\begin{aligned} b_2 = {} & C_1' C_2'(G_3 + G_{z1}) + C_1' C_{z1}(G_2' + G_{z2}') \\ & + C_2' C_{z1}(G_1 - 2G_2' + G_3 + G_{z3}'), \end{aligned}$$

$$b_3 = C_1' C_2' C_{z1},$$

$$a_{20} = -G_2' G_3(G_{z1} + G_{z3}') - G_2' G_{z1} G_{z3}',$$

$$a_{21} = -C_1' G_2'(G_3 + G_{z1}) - C_{z1} G_2'(G_3 + G_{z3}'),$$

$$\begin{aligned} a_{30} = {} & G_1 G_2'(G_3 + G_{z1}) + G_1 G_3 G_{z2}' - G_2' G_3 G_{z2}' \\ & + (G_1 - 2G_2') G_{z1} G_{z2}', \end{aligned}$$

$$\begin{aligned} a_{31} = {} & C_2' G_1(G_3 + G_{z1}) - C_2' G_2'(G_3 + 2G_{z1}) \\ & + C_{z1} G_1(G_2' + G_{z2}') - 2C_{z1} G_2' G_{z2}', \end{aligned}$$

$$a_{40} = G_1 G_2' G_3 + G_1 G_3 G_{z2}' - G_2' G_3 G_{z2}' + G_2' G_{z2}' G_{z3}',$$

$$a_{41} = C_2' G_3(G_1 - G_2') + C_2' G_2' G_{z3}' + C_1' G_2' G_{z2}'.$$

When the non-ideal equivalent circuit model of DDCC is used instead of the idea one in Fig. 1, the non-idealities of DDCC appear as the undesirable factors in (13)-(16), which lead to incorrect transfer functions. To minimize this error, more precise DDCC realization [21] would be more appropriate as it has lower parasitic. From (16), the non-idealities of DDCC appear as the undesirable factors in a_{41}. To minimize the effects of the DDCC's non-idealities at the notch filter, the conductance G_1 can be designed a litter smaller than the theoretical value.

In practical DDCC, the external resistors can be chosen very much smaller than the parasitic resistors at the y and z terminals of DDCC and very much greater than the parasitic resistors at the x terminals of DDCC, i.e. R_y, $R_z >> R_k >> R_x$. Moreover, the external capacitances C_1 and C_2 can be chosen very much greater than the parasitic capacitances at the y and z terminals of DDCC, i.e. C_y, $C_z << C_1$, C_2. Furthermore, assuming that the parasitic capacitances at the y terminals and z terminals of the DDCC are equal, i.e. $C_y \cong C_z$. Assuming that the parasitic resistances at the y terminals and z terminals of the DDCC are equal, i.e. $R_y \cong R_z$. Under these conditions, equations (13) to (16) become

$$\frac{V_{out1}}{V_{in}} \cong \frac{s^3 C_1'C_2'C_z + s^2 C_1'C_2'G_3}{D(s)} * \frac{-2G_2'G_3G_z}{D(s)} * \frac{R_2}{R_2+R_x}, \quad (17)$$

$$\frac{V_{out2}}{V_{in}} \cong \frac{-s^2 C_1'C_zG_2' - sC_1'G_2'G_3}{D(s)} * \frac{-2G_2'G_3G_z}{D(s)}, \quad (18)$$

$$\frac{V_{out3}}{V_{in}} \cong \frac{s^2 C_2'C_z(G_1-2G_2')}{D(s)} * \frac{+sC_2'(G_1-G_2')G_3 + G_1G_2'G_3}{D(s)}, \quad (19)$$

$$\frac{V_{out4}}{V_{in}} \cong \frac{s^2 C_1'C_2'G_2'}{D(s)} * \frac{+sC_2'(G_1-G_2')G_3 + G_1G_2'G_3}{D(s)} \quad (20)$$

where

$$D(s) \cong s^3 C_1'C_2'C_z + s^2 C_1'C_2'G_3 + s[C_2'(G_1-G_2') + C_1'G_2']G_3 + G_1G_2'G_3. \quad (21)$$

In equations (17) to (21), undesirable factors are yielded by the non-idealities of the DDCC. The capacitance C_z becomes effective at very high frequency; the conductance G_z becomes effective at low frequency. To minimize the effects of the DDCC's non-idealities, the operation angular frequency should restricted to the following conditions

$$\omega << \min \{\frac{G_3}{C_z}, \sqrt{\frac{[C_2'(G_1-G_2')+C_1'G_2']G_3}{C_1'C_2'C_z}}, \sqrt{\frac{G_1G_2'G_3}{C_2'C_z|2G_2'-G_1|}}\}, \quad (22)$$

$$\omega >> \max \{\sqrt{\frac{2G_2'G_z}{C_1'C_2'}}, \frac{2G_z}{C_1'}\}. \quad (23)$$

Moreover, application of the Routh-Hurwitz test to (21) shows that C_z may cause instability. According to this test, the transfer functions is stable if

$$(C_1'G_2' + C_2'G_1)G_3 > (C_2'G_3 + C_zG_1)G_2'. \quad (24)$$

It is not difficult to satisfy this condition, since the external capacitances C_1 and C_2 can be chosen very much greater than C_z.

5. Simulation Results

To verify the theoretical analysis, the proposed circuit was simulated using HSPICE with TSMC (Taiwan Semiconductor Manufacturing Company, Ltd.) 0.18μm, level 49 CMOS technology process parameters. The DDCC was realized by the CMOS implementation in Fig. 3 [22] with the NMOS and PMOS transistor aspect ratios W/L = 1.8u/0.18u and W/L = 7.2u/0.18u, respectively. The power supply voltages are V_+ = +1.25 V, V_- = -1.25 V and V_b = -0.5 V.

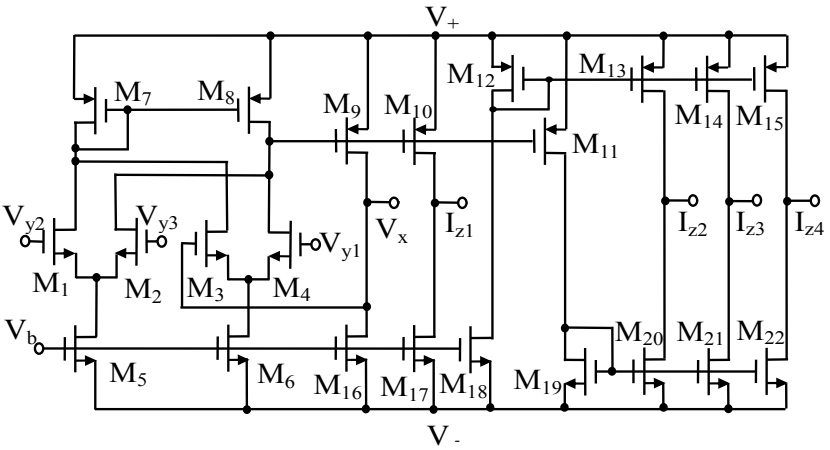
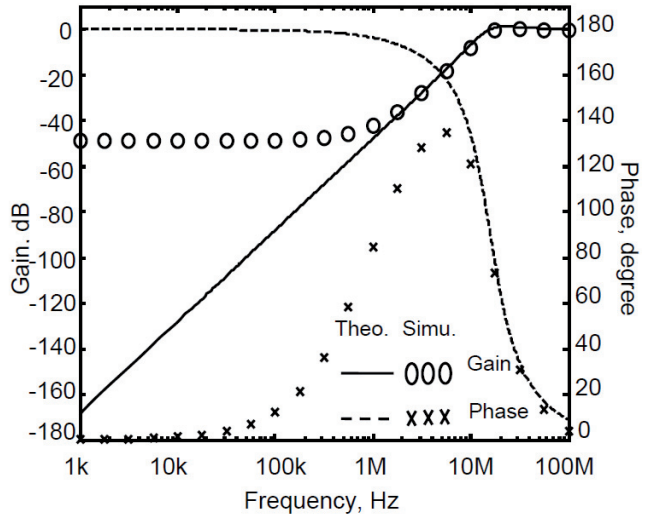
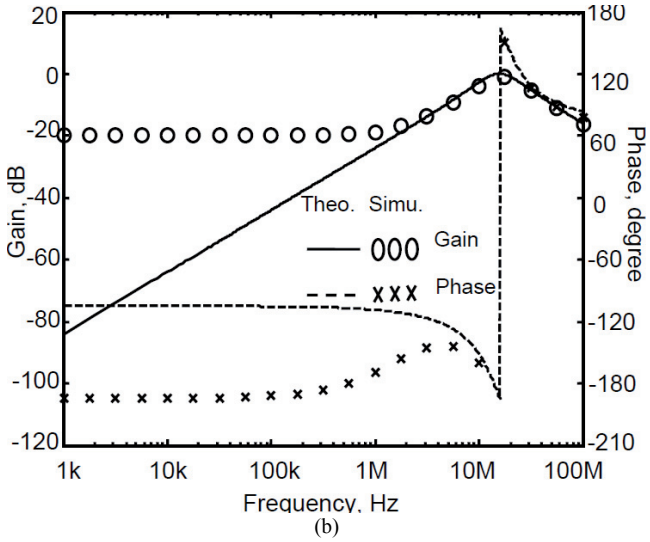


Fig. 3. The implementation of DDCC [22].

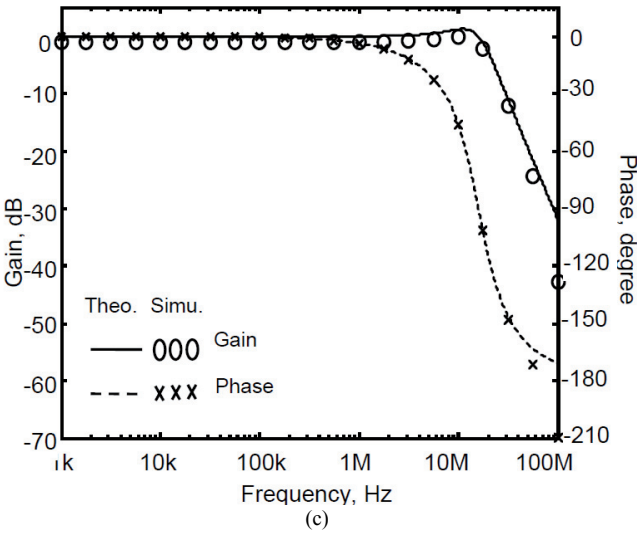
Fig. 4(a), (b), (c) and (d) represents the simulated frequency responses for the highpass (V_{out1}), bandpass (V_{out2}), lowpass (V_{out3}) and notch (V_{out4}) filters in Fig. 1, respectively, designed with f_o = 15.9 MHz, $C_1 = C_2 = 10$ pF, $R_1 = R_2 = R_3 = 1$ kΩ. From (17) and (18), the conductance G_z becomes effective at low frequency. This can explain why Fig. 4(a) and (b) have non-ideal frequency responses at low frequencies. In Fig. 4(d), the maximum attenuation of notch filter is -19.8 dB. Fig. 5 shows the square wave response of the filter of Fig. 1 with 150 mV input and V_{out2} output which confirms the stability of the implemented filter. Fig. 6 shows the input and output signals of bandpass response of the proposed filter. It is observed that 15.9 MHz with 360 mV_{p-p} input voltage signal levels are possible without significant distortion. In Fig. 7, THD (total harmonic distortion) of the bandpass filter is given for output voltages at 15.9 MHz operation frequency. These simulation results are coherent with the theoretical analyses.



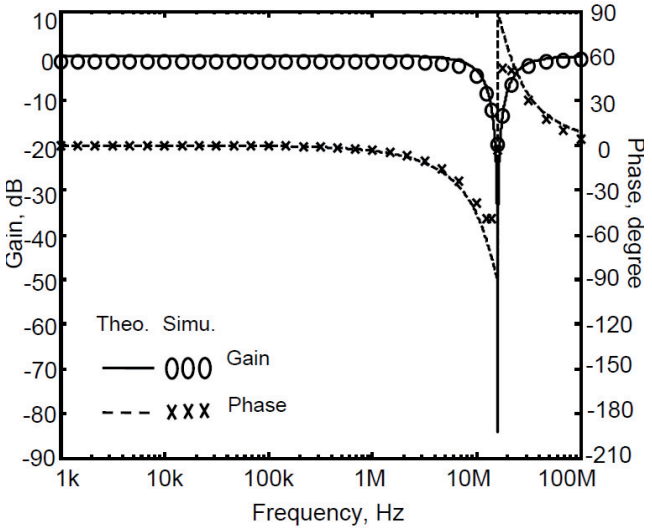
(a)



(b)



(c)



(d)

Fig. 4. Simulated frequency responses:
(a) for the highpass filter (V_{out1}) of Fig. 1,
(b) for the bandpass filter (V_{out2}) of Fig. 1,
(c) for the lowpass filter (V_{out3}) of Fig. 1,
(d) for the notch filter (V_{out4}) of Fig. 1.

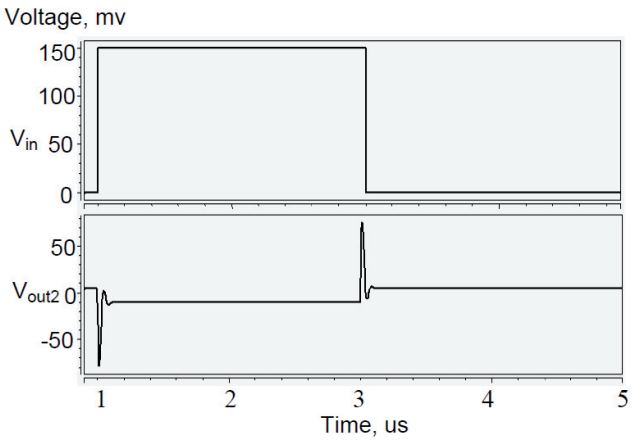


Fig. 5. Stability tests of the proposed filter.

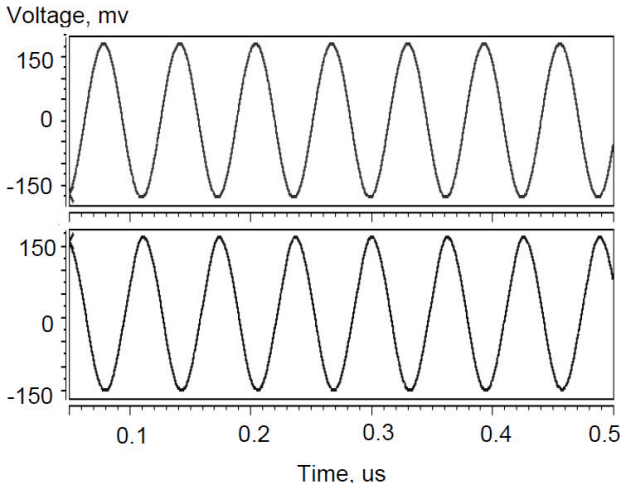


Fig. 6. Time-domain input (upper signal) and output signal waveforms to demonstrate the ac dynamic range of the proposed filter.

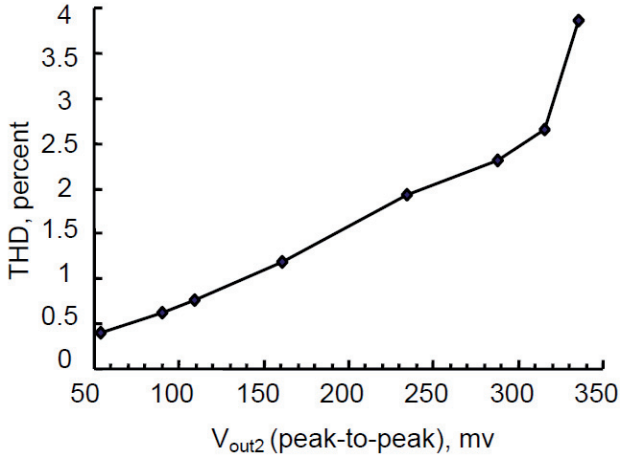


Fig. 7. THD analysis results of the proposed bandpass filter.

6. Conclusions

In this paper, a new voltage-mode multifunction biquadratic filter using one DDCC, two grounded capacitors and three resistors is proposed. The proposed circuit has the following features: (i) providing four standard filter functions, that is, highpass, bandpass, lowpass and notch filters, simultaneously, from the same circuit configuration, (ii) using only grounded capacitors and (iii) using only one active element. Because the output impedances of the proposed circuit are not low, voltage followers may be needed at output terminals to buffer the outputs and avoid the effects of load capacitances or resistances changing the responses of the filters.

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About Authors ...

Wei-Yuan CHIU received the M.S. degree in Electronic Engineering from Chung Yuan Christian University, Chung-Li, in 2005. Presently, he is working toward the Ph.D. degree in Electronic Engineering at Chung Yuan Christian University, Chung-Li. His research interests are in the area of active filter design.

Jiun-Wei HORNG was born in Tainan, Taiwan, Republic of China, in 1971. He received the B.S. degree in Electronic Engineering from Chung Yuan Christian University, Chung-Li, Taiwan, in 1993, and the Ph.D. degree from National Taiwan University, Taipei, Taiwan, in 1997. From 1997 to 1999, he served as a Second-Lieutenant in China Army Force. From 1999 to 2000, he joined CHROMA ATE INC. where he worked in the area of video pattern generator technologies. Since 2000, he was with the Department of Electronic Engineering, Chung Yuan Christian University, Chung-Li, Taiwan as an Assistant Professor. He is now an Associate Professor. Dr. Horng joins the Editorial Board of Active and Passive Electronic Components from 2010 and the Editorial Board of Radioengineering from 2011. His teaching and research interests are in the areas of Circuits and Systems, Analog Electronics, Active Filter Design and Current-Mode Signal Processing.