A 0.8 V T Network-Based 2.6 GHz Downconverter RFIC

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Abstract. *A 2.6 GHz downconverter RFIC is designed and implemented using a 0.18 μm CMOS standard process. An important goal of the design is to achieve the high linearity that is required in WiMAX systems with a low supply voltage. A passive T phase-shift network is used as an RF input stage in a Gilbert cell to reduce supply voltage. A single supply voltage of 0.8 V is used with a power consumption of 5.87 mW. The T network-based downconverter achieves a conversion gain (CG) of 5 dB, a single-sideband noise figure (NF) of 16.16 dB, an RF-to-IF isolation of greater than 20 dB, and an input-referred third-order intercept point (IIP_3) of 1 dBm when the LO power of -13 dBm is applied.*

Keywords

Downconverter, mixer, low voltage.

1. Introduction

Beyond 3G (B3G) systems, including the worldwide interoperability for microwave access (WiMAX) and the long term evolution (LTE) systems, feature with high data rates, high mobility, and large coverage areas. An RF transceiver in B3G systems must have a low power consumption to support long standby times of mobile devices. In a receiver, a downconverter is primarily responsible for converting frequencies. Operating a downconverter at a low supply voltage can greatly reduce the power consumed by B3G receivers. Proposed techniques to design a downconverter with a supply voltage below 1 V include: 1) current reuse [1]-[4], 2) the body-input scheme [5]-[7], and 3) use of a transformer [8]-[11]. The current reuse technique provides high conversion gain (CG) but at the cost of a poor noise figure (NF). The body-input technique supports transistor bias voltages that are lower than the threshold voltage but a high LO power (P_{LO}) is required to drive the transistors. The transformer technique provides a relatively high isolation but a large chip area is needed.

The goal of this work is to design and implement a low supply-voltage downconverter with a low input LO power using the TSMC 0.18 μm CMOS standard process for WiMAX applications. A passive T-type 180° phase shifter that consists of two series inductors and one parallel capacitor is used as a single-ended-to-differential converter of an input RF signal. The transistors in an active transconductance stage of a commonly used Gilbert mixer are absent, so the supply voltage of the downconverter can be reduced. A downconverter in a WiMAX receiver is often required to meet the high linearity specification for strictly high dynamic range. Therefore, the linearity performance of the T network-based downconverter with an inductor load and a π-resonator load are also compared with each other in this paper.

2. Circuit Design

Fig. 1 schematically depicts the circuit of the proposed downconverter with a T-type 180° phase-shift network. The T phase-shift network comprises two series inductances (L_T) and one shunt capacitance (C_T). The passive T network acts as a single-ended-to-differential converter. At first, the single-ended RF input signal that is applied to this T phase-shift network generates the differential RF signal. The transistors M_1 and M_2 form the two current sources, which have high output impedances to prevent the differential RF signal from leaking to ground. The transistors M_3, M_4, M_5, and M_6 comprise the multiplication core that is driven by the local oscillator. Since this multiplication core provides most of the conversion gain of the T network-based downconverter, the transistors from M_3 to M_6 must be biased at a point in the saturation region. The direct current (dc) bias design of the transistors from M_3 to M_6 is based on the principles of a multiplier, so the transistors are not pushed to the cutoff state. Therefore, the applied LO power can be kept small in the downconverter. Then, the RF and LO signals are mixed to generate the output differential IF signal. To reduce further the supply voltage, the inductor (L_D) is used as an output load because no dc voltage drop exists across it. Finally, the output voltage swing of the differential IF signal drops on the inductive load.

As indicated above, the single-ended-to-differential converter is a T phase-shift network. The amplitude and phase differences between nodes RF^+ and RF^-, presented in Fig. 1, are aimed to 0 dB and 180°, respectively. Notably, a capacitance value is much easier to implement in a CMOS standard process than an inductance value. There-

fore, the use of L_T to determine the C_T in a T network design is preferred. RF, LO, and IF frequencies of 2600, 2226, and 374 MHz, respectively, are used in the downconverter. The applied LO power is -13 dBm. Fig. 2 plots the simulated amplitude and phase errors between nodes RF^+ and RF^- within the range of C_T values from 1 to 1.6 pF for a selected L_T value of 1.3 nH. Notice that the amplitude and phase errors are the deviation of the amplitude and phase differences from 0 dB and 180°, respectively. They are extracted from the simulated phasor voltage at nodes RF^+ and RF^-. The simulation results are generated using an Agilent Advanced Design System (ADS). The C_T value is set to 1.32 pF to obtain 0 dB amplitude error and 0° phase error. The NMOS transistor, octagonal spiral inductor, and metal-insulator-metal (MIM) capacitor with particular specifications are used in the 0.18 μm CMOS standard process.

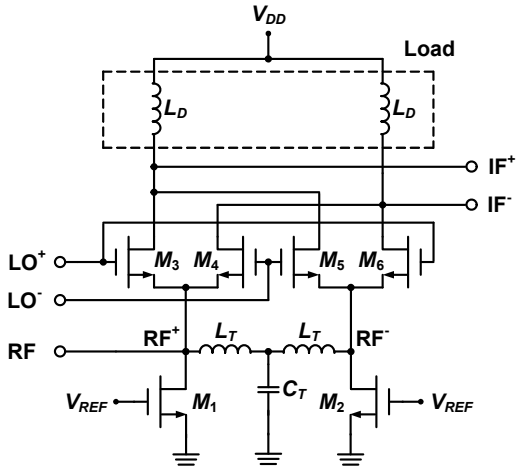

Fig. 1. Circuit schematic of proposed downconverter with a T phase-shift network.

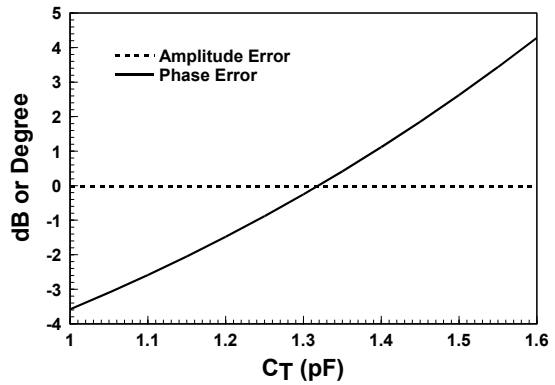

Fig. 2. Simulated amplitude and phase errors between nodes RF^+ and RF^- in T network-based downconverter within range of C_T values from 1 to 1.6 pF for L_T value of 1.3 nH.

Fig. 3 shows the amplitude and phase errors between nodes RF^+ and RF^- in the multi-point microwave distribution system (MMDS) band that covers frequencies from 2.5 to 2.69 GHz At the center design frequency of 2.6 GHz, the simulated amplitude and phase errors are 0 dB and -0.24°, respectively. Within the MMDS band, the simulated amplitude error is maintained at 0 dB. The simulated phase error which deviates from 2.6 GHz is higher than that at 2.6 GHz, but is still under 9°.

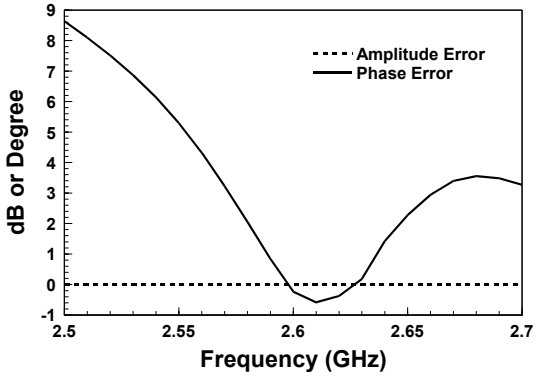

Fig. 3. Simulated amplitude and phase errors between nodes RF^+ and RF^- in T network-based downconverter within MMDS band.

3. Load Impedance Analysis

A downconverter that is responsible for the frequency conversion process in a WiMAX receiver is commonly required to meet the high linearity specifications of a high dynamic range. In designing downconverters, designers generally have to trade off conversion gain for high linearity. In fact, the trade-off between conversion gain and linearity determines the load at the IF output port of the downconverter, which is indicated in Fig. 1 by a broken-line rectangle. The impedances of two loads, an inductor and a π resonator, are analyzed below.

3.1 Inductor Load

Fig. 4 shows that two inductances (L_i) is used as the load of the T network-based downconverter. Notice that the supply voltage V_{DD} is regarded as alternating current (ac) grounded in the ac analysis. The load impedance looking into node IF^+ is denoted by $Z_{L,I}$. $Z_{L,I}$ can be obtained by connecting two series L_i, and is given by

$$Z_{L,I} = 2(j\omega L_i) \tag{1}$$

where ω is the angular frequency.

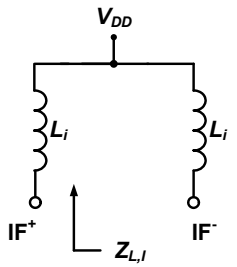

Fig. 4. Inductor load in T network-based downconverter.

3.2 π-Resonator Load

Fig. 5 shows that a π resonant circuit that is composed of one resistance (R_r), one inductance (L_r), and two capacitances (C_r) is used as the load of the T network-based downconverter. In the circuit shown in Fig. 5, $Z_{L,R}$ is the load impedance looking into node IF^+. The *RFC* denotes an RF choke. The center node between nodes IF^+ and IF^- is virtually grounded due to the balance of the circuit. The π resonator can be analyzed using its differential half-circuit. Fig. 6 shows the equivalent differential half-circuit with an impedance of half $Z_{L,R}$. Half of $Z_{L,R}$ is obtained by considering the connection of $R_r/2$, $L_r/2$, and C_r in parallel:

$$\frac{Z_{L,R}}{2} = \left(\frac{1}{R_r/2} + \frac{1}{j\omega L_r/2} + j\omega C_r\right)^{-1} = \left[\frac{1}{R_r/2} + j\left(\omega C_r - \frac{1}{\omega L_r/2}\right)\right]^{-1}. \quad (2)$$

Resonance occurs when the imaginary part of $Z_{L,R}/2$ is zero. The resonant angular frequency ω_0 can be derived as

$$\omega_0 = \frac{1}{\sqrt{\frac{L_r}{2} C_r}}. \quad (3)$$

Then, $Z_{L,R}/2$ at ω_0 is $R_r/2$, which is a purely real impedance. Hence $Z_{L,R}$ at resonance can be found as

$$Z_{L,R} = R_r. \quad (4)$$

R_r can be used to determine the impedance of the π-resonator load at resonance.

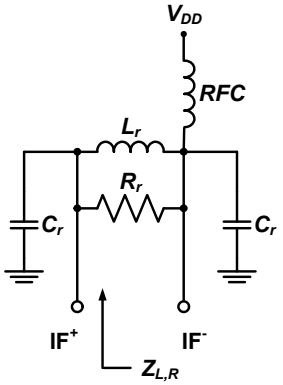

Fig. 5. π-resonator load in T network-based downconverter.

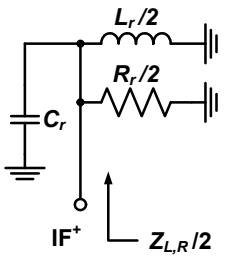

Fig. 6. Equivalent differential half-circuit of π-resonator load.

3.3 Comparison of Results and Discussions

The IF frequency that is used in the T network-based downconverter is 374 MHz. For an inductor load, the L_i in Fig. 4 is set to 330 nH. Substituting this value into (1) yields a magnitude of $Z_{L,I}$ of approximately 1.55 kΩ. For a π-resonator load, R_r, L_r, and C_r in Fig. 5 are set to 20 kΩ, 30 nH, and 12.085 pF, respectively. Substituting these values into (3) and (4) yields a resonant frequency of 374 MHz and a magnitude of $Z_{L,R}$ at resonance of 20 kΩ. Notably, L_r of the π-resonator load is much less than L_i of the inductor load, which, in this case, is 1/11.

Fig. 7 compares the magnitudes of $Z_{L,I}$ and $Z_{L,R}$ versus frequency. As shown in Fig. 7, the magnitude of $Z_{L,I}$ increases with frequency and its value is 1.55 kΩ at an IF frequency of 374 MHz. Fig. 7 also demonstrates that the magnitude of $Z_{L,R}$ as a function of frequency is like a spike. The maximum $Z_{L,R}$ magnitude is 20 kΩ, which is reached at a resonant frequency of 374 MHz, which is the IF frequency. A comparison of $Z_{L,I}$ and $Z_{L,R}$ magnitudes at 374 MHz shows that the magnitude of $Z_{L,R}$ is much higher than that of $Z_{L,I}$, by, in this instance, a factor of almost 13. This result implies that a small inductance can yield a large load impedance when a π resonant circuit is used. The conversion gain for a downconverter is usually proportional to its load impedance. The π-resonator load with high load impedance can then ensure that the conversion gain of the downconverter is high. In contrast, an inductor load with a low load impedance yields a low conversion gain of the downconverter.

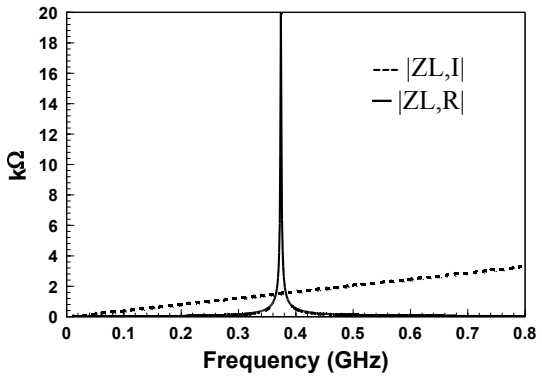

Fig. 7. Comparison of simulated magnitudes of $Z_{L,I}$ and $Z_{L,R}$.

Fig. 8 plots the dynamic load line superimposed on the drain-source current (I_{DS}) versus the drain-source voltage (V_{DS}) curves of transistors M_3 and M_5 that are displayed in Fig. 1. The input RF power is set to -20 dBm, which is less than the input-referred 1 dB compression point (IP_{1dB}) of the T network-based downconverter using an inductor load or a π-resonator load. Fig. 8 shows that the locus of the dynamic load line for an inductor load is an ellipse, whereas that of dynamic load line for a π-resonator load is a distorted ellipse. The main reason for the distortion is that high conversion gain that is provided by the π-resonator load easily causes saturation owing to gain compression. The method given by [12] for measuring the linearity per-

formance is to estimate the locus of a dynamic load line. An elliptic locus corresponds to good linearity. Therefore, the T network-based downconverter with an inductor load can provide higher linearity than that with a π-resonator load.

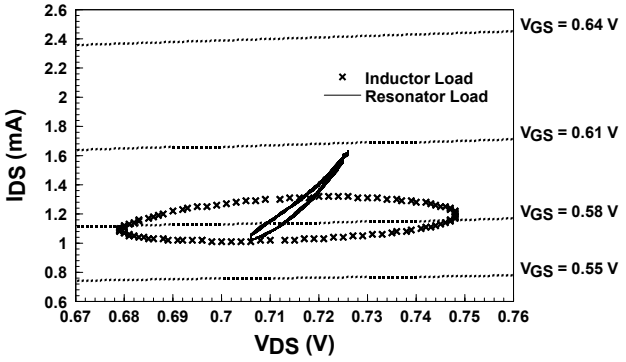

Fig. 8. Comparison between the simulated dynamic load lines superimposed on I_{DS}-V_{DS} curves for inductor and π-resonator loads.

Fig. 9 compares the simulated results for the gain compression of the T network-based downconverter with inductor and π-resonator loads. The downconverter with an inductor load yields a conversion gain of 5 dB and an IP_{1dB} of -10 dBm. The conversion gain and IP_{1dB} are 7.7 dB and -15 dBm, respectively, for the downconverter using a π-resonator load. Clearly, a π-resonator load with the larger load impedance provides a 2.7 dB higher conversion gain for a T network-based downconverter but at the cost of a 5 dB lower linearity than that of an inductor load with the smaller load impedance.

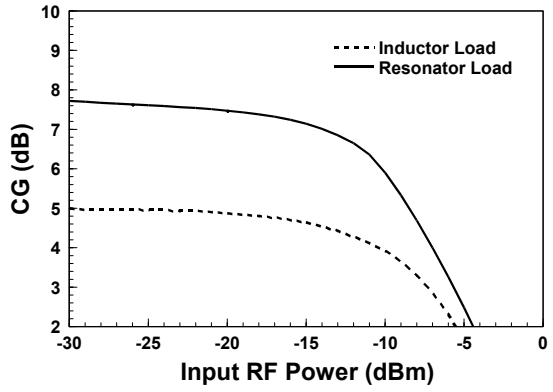

Fig. 9. Comparison of simulated gain compression in T network-based downconverter with inductor and π-resonator loads.

4. Implementation and Experiment

The linearity of a downconverter is essential in WiMAX applications. Therefore, an inductor load is used as an output interface network in the implemented T network-based downconverter. Notably, the 330 nH inductor is arranged off-chip to reduce the chip area. The microphotograph in Fig. 10 shows that the T network-based downconverter RFIC that is implemented using a TSMC 0.18 μm CMOS foundry process has an area of 0.93 mm × 0.93 mm. The downconverter RFIC was mounted and bounded on an FR4 printed circuit board for testing. The downconverter requires a three-port measurement setup to provide the RF signal and LO carrier with power and frequency sweeps as input signals, and to generate the output IF signal to evaluate all RF parameters. The single-ended RF input impedance is matched to 50 Ω by an external matching network. A microstrip ring hybrid is used as a passive balun to convert an incoming single-ended LO signal into a differential one with the input impedance matched to 50 Ω. Similarly, an output IF differential signal is transformed into a signal-ended one with the output impedance matched to 50 Ω using a Mini-Circuits TC1-1-13M+ passive balun. The power consumption (P_{DC}) from the single supply voltage of 0.8 V is 5.87 mW. The applied LO power is -13 dBm. The measured RF, LO, and IF return losses exceed 16 dB, 14 dB, and 12 dB, respectively.

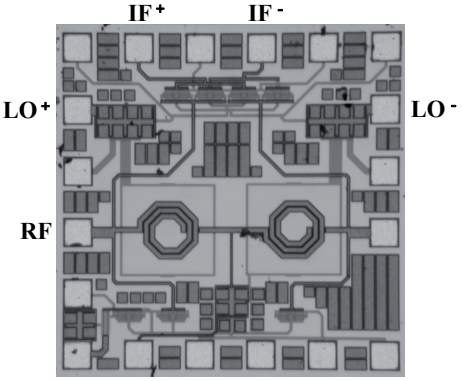

Fig. 10. Chip micrograph of the implemented downconverter RFIC.

Fig. 11 plots the measured conversion gain and noise figure in the WiMAX MMDS band that covers frequencies from 2.5 to 2.69 GHz. Notice that the measured conversion gain is obtained using an R&S ZVA 40 vector network analyzer and an R&S SMF 100A signal generator. The noise figure is measured with a Mini-Circuits NC346C noise source, an R&S SMBV100A vector signal generator, and an R&S FSV signal analyzer. The maximum conversion gain is 5.2 dB at 2.58 GHz. As indicated in Fig. 11, the 3 dB bandwidth covers the entire applied frequency range. Although the input stage of the T network-based downconverter is a passive network, by a multiplication stage that comprises four transistors can provide its conversion gain. Fig. 11 also shows that the measured noise figure is higher than 14 dB due to parasitic loss of the 1.3 nH octagonal spiral inductor in the T network, but still under 17.6 dB from 2.5 to 2.69 GHz.

Fig. 12 plots the measured the LO-to-IF, LO-to-RF, and RF-to-IF isolations of the T network-based downconverter. Within the LO frequency from 2.126 to 2.316 GHz, both LO-to-IF and LO-to-RF isolations are greater than 17 dB, but below 20 dB. This shortcoming can be overcome by keeping the incoming LO power to the downcon-

verter low. The RF-to-IF isolation exceeds 20 dB in the RF frequency range that covers from 2.5 to 2.69 GHz.

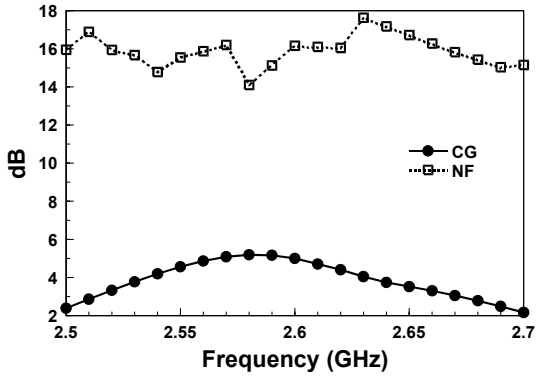

Fig. 11. Measured conversion gain and noise figure in T network-based downconverter.

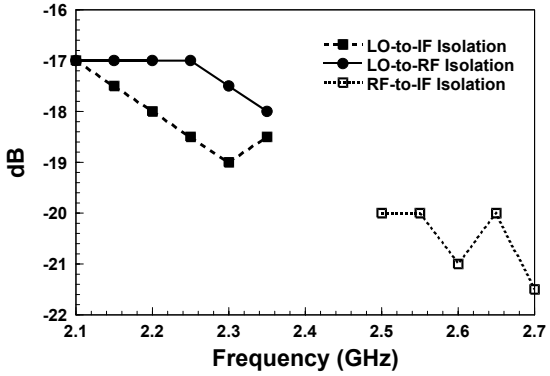

Fig. 12. Measured isolation in T network-based downconverter.

In a two-tone test, the RF, LO, and IF frequencies in the downconverter are set to 2600, 2226, and 374 MHz, respectively. The frequency spacing is set to 20 MHz, which is the channel bandwidth in WiMAX systems. Fig. 13 shows the simulated and measured output powers of fundamental and third-order intermodulation (IM_3) products in the T network-based downconverter. The agreement is quite good. The conversion gain and the IP_{1dB} of the downconverter are 5 dB and -10 dBm, respectively. Fig. 13 also indicates that the T network-based downconverter has an input-referred third-order intercept point (IIP_3) of 1 dBm, revealing that it has good linearity. This is because a passive T-type *LC* network that is used as a single-ended-to-differential converter replaces the active differential-pair transconductance stage of a Gilbert mixer, increasing the voltage drop and reducing the voltage swing.

Tab. 1 summarizes the performance merits of this work and compares it with previous proposed designs of low supply-voltage downconverters in [2], [3], [5], [6], [9]. The applied LO power level that is generated by a frequency synthesizer must be considered to determine the power consumption in an overall WiMAX system, especially in the low-voltage downconversion mixer design. In Tab. 1, a figure of merit (FOM) in terms of LO power is defined as

$$\mathbf{FOM} = 10\log\left(\frac{\mathbf{CG}}{\mathbf{NF}}\frac{\mathbf{IIP_3}}{\mathbf{P_{DC}}}\frac{1}{\mathbf{P_{LO}}}\right)\left(\frac{1}{\mathbf{W}}\right). \quad (5)$$

Numerical values of CG and NF are substituted into (5). The IIP_3, P_{DC}, and P_{LO} are expressed in watt (W). The comparison shows that the proposed downconverter has the highest FOM among all the works listed in Tab. 1.

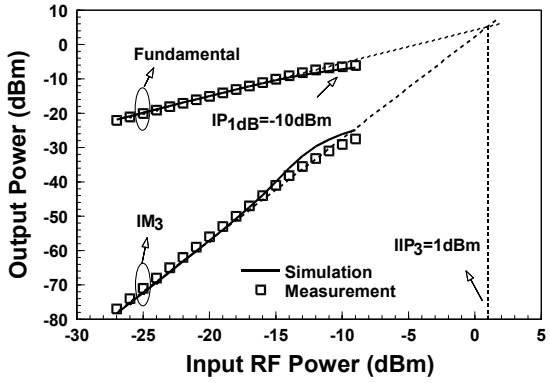

Fig. 13. Simulated and measured output powers for the fundamental and IM_3 products in T network-based downconverter.

	[2]	[3]	[5][a]	[6]	[9]	This Work
RF Freq. (GHz)	5.25	5.25	1.9	2.4	2.5	2.6
Supply Voltage (V)	0.9	0.9	0.8	0.77	0.6	0.8
P_{DC} (mW)	6.57	4.95	0.4	0.48	1.6	5.87
P_{LO} (dBm)	-3.6	5.5	0	5	-1	-13
CG (dB)	8.89	8.3	3	5.7	5.4	5
NF (dB)	24	24.5	10	15	14.8	16.16
IIP_3 (dBm)	-11.555	0.03	-11	-5.7	-2.8	1
FOM (1/W)	-1.24	1.38	15.98	13.19	16.76	25.15

a: Simulated results

Tab. 1. Comparison of performance of the proposed downconverter with those of downconverters presented elsewhere.

5. Conclusions

A low-voltage 2.6 GHz downconverter RFIC design with a T phase-shift network and an inductive load was implemented using a 0.18 μm CMOS standard process. Its main advantage is its lower input LO power and higher IIP_3 than those of other available techniques.

Acknowledgements

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References

[1] DEBONO, C. J., MALOBERTI, F., MICALLER, J. A 900 MHz, 0.9 V low-power CMOS downconversion mixer. In *Proceedings of the 2001 IEEE Conference on Custom Integrated Circuits*. San Diego (U.S.), 2001, p. 527 - 530.

[2] HUANG, M.-F., LEE, S.-Y., KUO, C. J. A 5.25 GHz even harmonic mixer for low voltage direct conversion receivers. In *Proceedings of the 2005 Asian Solid-State Circuits Conference*. Hsinchu (Taiwan), 2005, p. 321 - 324.

[3] HUANG, M.-F., KUO, C. J., LEE, S.-Y. A 5.25-GHz CMOS folded-cascode even-harmonic mixer for low-voltage applications. *IEEE Transactions on Microwave Theory and Techniques,* 2006, vol. 54, no. 2, p. 660 - 669.

[4] DEGUCHI, J., MIYASHITA, D., HAMADA, M. A 0.6V 380μW −14dBm LO-input 2.4GHz double-balanced current-reusing single-gate CMOS mixer with cyclic passive combiner. In *Digest of the 2009 IEEE International Solid-State Circuits Conference*. San Francisco (U.S.), 2009, p. 224 - 225,225a.

[5] JAFFERALI, N., DEEN, M. J. Low-voltage and low-power 1.9GHz body-input downconversion mixer. In *Proc. of the 2004 Canadian Conference on Electrical and Computer Engineering*. Niagara Falls (Canada), 2004, p. 1413 - 1416.

[6] LIANG, K.-H., CHANG, H.-Y., CHAN, Y.-J. A 0.5–7.5 GHz ultra low-voltage low-power mixer using bulk-injection method by 0.18-μm CMOS technology. *IEEE Microwave and Wireless Components Letters,* 2007, vol. 17, no. 7, p. 531 - 533.

[7] LIANG, K.-H., CHANG, H.-Y. 0.5-6 GHz low-voltage low-power mixer using a modified cascode topology in 0.18 μm CMOS technology. *IET Microwaves, Antennas & Propagation,* 2011, vol. 5, no. 2, p. 167 - 174.

[8] HERMANN, C., TIEBOUT, M., KLAR, H. A 0.6V 1.6mW transformer based 2.5GHz downconversion mixer with +5.4dB gain and -2.8dBm IIP3 in 0.13μm CMOS. In *Digest of the 2004 IEEE Radio Frequency Integrated Circuits Symposium*. Fort Worth (U.S.), 2004, p. 35 - 38.

[9] HERMANN, C., TIEBOUT, M., KLAR, H. A 0.6-V 1.6-mW transformer-based 2.5-GHz downconversion mixer with +5.4-dB gain and -2.8-dBm IIP3 in 0.13-μm CMOS. *IEEE Trans. on Microwave Theory and Techniques,* 2005, vol. 53, no. 2, p. 488 - 495.

[10] YANG, T.-Y., TU, H.-L., CHIOU, H.-K. Low-voltage high-linear and isolation transformer based mixer for direct conversion receiver. In *Proc. of the 2006 IEEE International Symp. on Circuits and Systems*. Island of Kos (Greece), 2006, p. 3754 - 3757.

[11] LAI, J.-T., LIN, Y.-S., LU, C.-L., CHUANG, H.-R. A 3-5-GHz low-voltage high-isolation transformer-based CMOS mixer for UWB applications. In *Proc. of the 3rd Int. Conf. on Innovative Computing Information and Control*. Dalian (China), 2008, p. 238.

[12] OHARA, S., NAKASHA, Y., IWAI, T., JOSHIN, K. Measurement of dynamic load lines of power heterojunction bipolar transistor. In *Digest of the 1997 IEEE MTT-S International Microwave Symposium*. Denver (U.S.), 1997, p. 909 - 912.

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