High Dynamic Range RF Front End with Noise Cancellation and Linearization for WiMAX Receivers

Jian-Ming WU, Chun-Hung YEH, Ching-Jui CHUANG

Dept. of Electronic Engineering, National Kaohsiung Normal University, Kaohsiung 824, Taiwan

jianmingwu@nknucc.nknu.edu.tw

Abstract. *This research deals with verification of the high dynamic range for a heterodyne radio frequency (RF) front end. A 2.6 GHz RF front end is designed and implemented in a hybrid microwave integrated circuit (HMIC) for worldwide interoperability for microwave access (WiMAX) receivers. The heterodyne RF front end consists of a low-noise amplifier (LNA) with noise cancellation, an RF band-pass filter (BPF), a downconverter with linearization, and an intermediate frequency (IF) BPF. A noise canceling technique used in the low-noise amplifier eliminates a thermal noise and then reduces the noise figure (NF) of the RF front end by 0.9 dB. Use of a downconverter with diode linearizer also compensates for gain compression, which increases the input-referred third-order intercept point (IIP_3) of the RF front end by 4.3 dB. The proposed method substantially increases the spurious-free dynamic range (DR_f) of the RF front end by 3.5 dB.*

Keywords

Front end, low-noise amplifier (LNA), mixer, downconverter, heterodyne, receiver, radio frequency (RF).

1. Introduction

Wireless systems are now a major communication mode in urban areas. Wireless systems can be classified into two categories based on data rate, mobility, and coverage area: 1) wireless local area network (WLAN) and 2) cellular mobile network. Whereas WLANs have a high data rate but poor mobility and low coverage area [1], cellular mobile networks have high mobility, large coverage areas, but low data rates during high speed movement [2]. Current WLAN and cellular mobile networks are unsuitable for next-generation wireless systems, which require high data rates, high mobility, and large coverage areas. One solution is worldwide interoperability for microwave access (WiMAX) system with orthogonal frequency division multiplexing (OFDM) techniques. The WiMAX standard IEEE 802.16e achieves the maximum data rate of 75 Mbps, a mobile speed up to 120 km/h, and a maximum coverage area of 48 km [3]. However, achieving these performance features requires a receiver with a high dynamic range.

A heterodyne architecture is commonly used in receivers because of its high sensitivity and good selectivity [4]. Wireless systems based on heterodyne architectures that have been proposed in the literature include: 1) IEEE 802.11 a/b/g [5]-[7] and Buletooth [8], [9] in WLANs; 2) global system for mobile communications (GSM) [10], [11] and wideband code division multiple access (W-CDMA) systems [12], [13] in cellular mobile networks; and 3) IEEE 802.16e [14] in WiMAX systems. An RF front end in a heterodyne receiver has two primary functions, amplifying weak signals from an antenna and converting frequencies. A WiMAX receiver often requires an RF front end to meet the low-noise and high-linearity specifications needed to achieve a high dynamic range.

This study aims to increase the dynamic range of a WiMAX heterodyne receiver front end. The presented RF front end was implemented in a hybrid microwave integrated circuit (HMIC) with Agilent discrete GaAs enhancement-mode high electron mobility transistor (HEMT) and WIN GaAs HEMT foundry process of f_T up to 85 GHz. Through the careful comparison between simulation and measurement, we find that a low noise amplifier in the first stage of an RF front end with noise cancellation and a downconverter in the latter stage of an RF front end with linearization substantially improve the dynamic range of a heterodyne RF front end.

2. Dynamic Range

An RF front end of a receiver can be any distance from a base station in a wireless system. A dynamic range is specified to ensure that an RF front end maintains good communication quality regardless of distance to a base station. Therefore, the dynamic range of an RF front end is the range of power of received signals that can be demodulated accurately. A noise level determines the lower limit of dynamic range, which relates to noise figure (*NF*) of an RF front end. Linearity determines the upper limit of the dynamic range, which is related to distortion of an RF front end.

The spurious-free dynamic range (DR_f) is defined as

a power range limited at the low end by the third-order intermodulation (IM_3) product equal to the noise level and at high end by the corresponding output signal power [15]. By referring to the derivation in [15], DR_f can be expressed in terms of the output-referred third-order intercept point (OIP_3) and the output noise power (N_o) of an RF front end as

$$DR_f = \frac{2}{3}(OIP_3 - N_o) \text{ (dB)}. \quad (1)$$

Note that N_o is the sum of the input noise power (N_i), the gain (G) and NF of an RF front end. According to the definition of input noise power given in [15], $N_i = kT_0B$, where $k = 1.380 \times 10^{-23}$ J/K is the Boltzmann's constant; T_0= 290 K is the noise temperature at room temperature; and B is the system bandwidth. Therefore, DR_f can be rewritten as

$$DR_f = \frac{2}{3}[OIP_3 - G - NF - 10\log(kT_0B/1mW)] \text{ (dB)}. \quad (2)$$

After subtracting G from OIP_3 to obtain an input-referred third-order intercept point (IIP_3), (2) can be simplified as

$$DR_f = \frac{2}{3}[IIP_3 - NF - 10\log(kT_0B/1mW)] \text{ (dB)}. \quad (3)$$

This clearly shows that the spurious-free dynamic range can be enhanced by increasing the input-referred third-order intercept point or by reducing the noise figure within the same system bandwidth.

3. Building Blocks

Fig. 1 shows the proposed heterodyne RF front end for WiMAX applications, which consists of a low-noise amplifier (LNA) with noise cancellation, an RF bandpass filter (BPF), a downconverter with linearization, and an IF BPF. A low-noise amplifier is used to amplify an input RF signal. An RF BPF selects the multipoint microwave distribution system (MMDS) band that covers from 2.5 to 2.69 GHz in WiMAX systems. Another important function is rejecting image signals. A downconverter takes charge of the frequency conversion process in a WiMAX RF receiver front end. The RF signals from 2.5 to 2.69 GHz and local oscillator (LO) signals from 2.126 to 2.316 GHz are mixed to generate the output IF signal at 374 MHz. The IF BPF in the next stage of a downconverter not only chooses the desired IF signal of 374 MHz but also filters out spurious signals.

The four components comprising the RF front end, as shown in Fig. 1, have noise factors F_1, F_2, F_3, F_4, and gains G_1, G_2, G_3, G_4. Notice that the noise factor F is the numerical value of the noise figure NF that is expressed in dB. By referring to [15], the noise factor of the entire RF front end can be expressed as

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} + \frac{F_4 - 1}{G_1G_2G_3}. \quad (4)$$

According to (4), the noise characteristic of the low-noise amplifier that is in the first stage of an RF front end dominates the noise factor of the overall RF front end. Therefore, the low-noise amplifier having a low noise figure and at least moderate gain can achieve the best noise performance of the entire RF front end.

A downconverter in the latter stage of an RF front end dominates the IIP_3 of the whole RF front end. As mentioned in Section 2, the spurious-free dynamic range increases as the noise figure decreases or as IIP_3 rises. The proposed method of increasing the spurious-free dynamic range for an RF front end is to use a low-noise amplifier with a noise cancellation technique to decrease thermal noise and a downconverter incorporating a diode linearizer to enhance linearity.

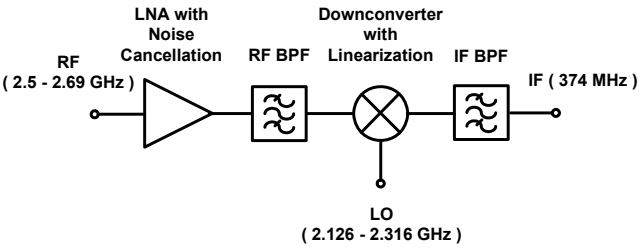


Fig. 1. Block diagram of the heterodyne RF front end for WiMAX receivers.

The theorems of noise canceling in a low-noise amplifier and linearization in a downconverter can be analyzed as follows.

3.1 Low-Noise Amplifier with Noise Canceling

Fig. 2 shows the circuit schematic of the proposed low-noise amplifier with noise canceling [16], [17]. In the circuit shown in Fig. 2, a signal source voltage is denoted by v_S. The R_S and R_L represent signal source resistance and load resistance, respectively. The RFC is an RF choke. The C_B denotes a direct current (dc) block capacitor. A common-gate transistor M_1 is cascaded with a common-source transistor M_2, which forms the basic structure of the low-noise amplifier. Since transistor M_1 is the first transistor, it dominates the noise performance of this low-noise amplifier [18]. Therefore, a common-source transistor M_3 is used to cancel the thermal noise generated from transistor M_1.

Fig. 2 also illustrates the noise canceling principle. The $i_{n,M1}$ represents the noise current produced in transistor M_1. Since noise current flow through resistors R_G and R_D is in opposite directions, the noise voltages at the gates of transistors M_2 and M_3 are out of phase. These two out-of-phase noises are amplified by transistors M_2 and M_3, respectively, and then added to obtain a total noise of zero at the output of low-noise amplifier. Applying Ohm's law as described in [17] shows that the output noise current is equal to zero only when

$$G_{m,\mathrm{M2}} \times R_D = G_{m,\mathrm{M3}} \times (R_S \,//\, R_G) \tag{5}$$

where the transconductance of transistors M_2 and M_3 are denoted by $G_{m,M2}$ and $G_{m,M3}$, respectively.

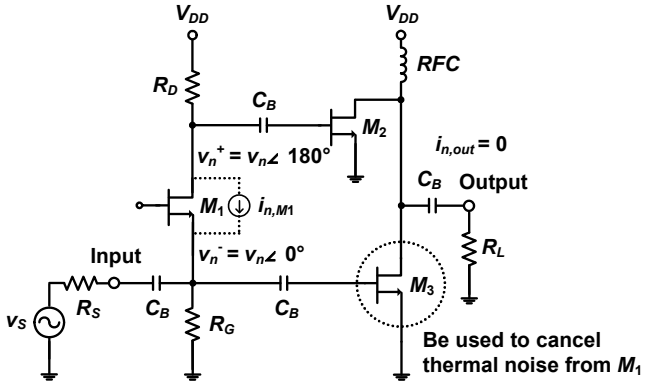


Fig. 2. Circuit schematic of the proposed low-noise amplifier design with a noise canceling technique.

3.2 Downconverter with Diode Linearizer

In the downconverter design, designers usually have to make concession in gain and noise in order to attain high linearity performance. Fig. 3 shows the proposed downconverter based on a Gilbert mixer with a diode linearizer, which improves linearity without the above-mentioned expenses [19]. Notably, [19] provided only preliminary results of the downconverter without the detailed analysis of diode linearization provided here. Additionally, the downconverter in this work was fabricated by WIN GaAs HEMT foundry process, unlike the implementation with discrete transistors in [19].

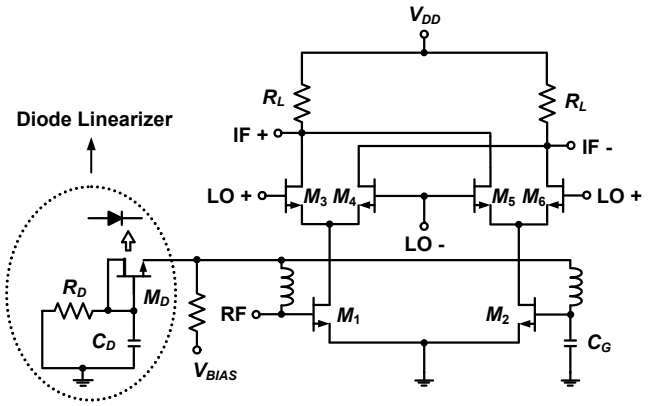


Fig. 3. Schematic diagram of circuit with a Gilbert mixer and a diode linearizer for use in a WiMAX downconverter design.

In the circuit shown in Fig. 3, the basic structure of a Gilbert mixer is mainly constructed by the transistors from M_1 to M_6, in which M_1 and M_2 comprise a differential-pair transconductance stage while M_3, M_4, M_5, and M_6 comprise a switch stage. The differential-pair transconductance stage has one input for the incoming single-ended RF signal and has the other input alternating current (ac) grounded. Initially, the input single-ended RF signal is amplified by differential-pair transconductance stage. Then the output voltage drops on the load resistances (R_L) result from the differential LO signal used for switching transistors M_3 to M_6 on and off. The mixed RF and LO signals then generate the output differential IF signal. The same voltage drop across R_L and M_1 or M_2 maximizes the output voltage swing. Therefore, the dc bias design is based on this principle and under a condition not to push each switch transistor to the cut-off state.

Fig. 3 also shows that the diode linearizer primarily consists of a diode, a resistor, and a capacitor. The gate of transistor M_D is connected to its drain to form a Schottky diode. As a matter of fact, a diode linearizer acts as a rectifier circuit. Fig. 4 shows that its equivalent half-wave rectifier is composed of a diode (D) and a resistor (R_D) with a filter capacitor (C_D). Note that the cathode of a diode is connected to the input RF port of a Gilbert mixer, that is, the gate of transistors M_1 and M_2, as shown in Fig. 4. Therefore, the diode switches off during the positive half cycle of input RF signal and switches on during the negative half cycle.

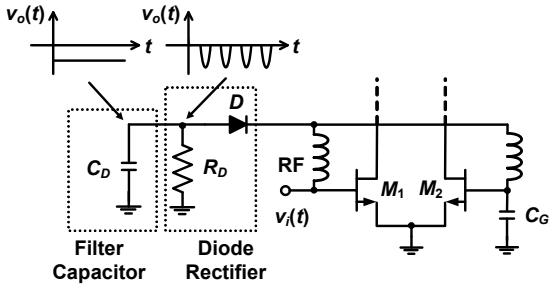


Fig. 4. Circuit and waveforms for a half-wave rectifier with a filter capacitor.

The time-dependent expression of input RF voltage can be written as a sine function. That is

$$v_i(t) = A \sin \omega t \tag{6}$$

where A is the amplitude; ω is the angular frequency; and t is the time. The diode voltage drop is assumed to be ideally zero. In the positive half cycle of an input RF signal, that is, when input voltage $v_i(t)$ exceeds 0 V, the diode is turned off. Thus, the output voltage $v_o(t)$ of a half-wave rectifier is equal to zero. Conversely, in the negative half cycle of input RF signal, that is, when the input voltage $v_i(t)$ is below 0 V, the diode is turned on. Thus, $v_o(t)$ is equal to the input voltage $v_i(t)$. This gives

$$v_o(t) = 0,\ v_i(t) > 0 \text{ V}, \tag{7}$$

$$v_o(t) = A \sin \omega t,\ v_i(t) < 0 \text{ V}. \tag{8}$$

Let the conduction angle θ be equal to ωt. Then, (7) and (8) can be written in terms of θ as

$$v_o(\theta) = 0,\ 0 < \theta < \pi, \tag{9}$$

$$v_o(\theta) = A \sin \theta,\ \pi < \theta < 2\pi. \tag{10}$$

This clearly shows that a half-wave rectifier transforms an input sine waveform into an output unidirectional waveform with a dc component. The dc voltage V_o can be obtained by integrating $v_o(\theta)$ over the interval from 0 to 2π and then dividing by 2π, which is given as

$$\begin{aligned} V_o &= \frac{1}{2\pi}\int_0^{2\pi} v_o(\theta)\, d\theta \\ &= \frac{1}{2\pi}\int_{\pi}^{2\pi} A\sin\theta\, d\theta \\ &= -\frac{A}{\pi}. \end{aligned} \tag{11}$$

As illustrated in Fig. 4, a pulsating waveform generated from the half-wave rectifier can not be used as a dc bias for a Gilbert mixer. Thus, a filter capacitor C_D is needed to smooth the pulsating half-wave rectified waveform.

According to (11), the negative dc voltage with respect to amplitude A is produced by the rectification of a diode linearizer, which increases the dc component of the gate-source voltage (V_{GS}) in transistors M_1 and M_2. Note that the larger the input amplitude A, i.e., the higher the incoming power level, the larger the increase in V_{GS} of M_1 and M_2. The drain-source current (I_{DS}) of the transistors M_1 and M_2 increases with the square of their V_{GS}, and the conversion gain (CG) of a Gilbert mixer is generally proportional to I_{DS} of its input stage, so a diode linearizer in a Gilbert mixer substantially increases conversion gain when input power is high. This mechanism compensates for gain compression and substantially enhances linearity in a Gilbert mixer.

4. Simulation and Measurement

The RF front end is implemented in HMIC. The first-stage low-noise amplifier is manufactured with an Agilent discrete GaAs enhancement-mode HEMT. Notably, the amplitude and phase imbalances of signal traces between transistors M_2 and M_3 shown in Fig. 2 degrade noise cancellation. Therefore, the layout of the low-noise amplifier on a printed circuit board (PCB) must be adequately balanced. The supply voltage of the low-noise amplifier is 1.8 V. Tab. 1 compares the characteristics of the low-noise amplifier with and without a noise canceling technique. Note that in Tab. 1 *RL* represents the return loss and IP_{1dB} denotes the input-referred 1 dB compression point. The power consumption is represented by P_{DC}. Tab. 1 shows the measured noise figure of the low-noise amplifier can be reduced by 1.4 dB with a noise canceling technique.

The BFCN-2555+ filter produced by Mini-Circuits is used as a second-stage RF BPF. Both input and output impedances of BFCN-2555+ are matched to 50 Ω. The measured VSWR and insertion loss from 2.5 GHz to 2.69 GHz is smaller than 1.43 and 4 dB, respectively, which meets the specifications indicated in the Mini-Circuits data sheet [20].

	with Noise Cancellation		without Noise Cancellation	
	Simulation	Measurement	Simulation	Measurement
G (dB)	10.2	10.2	9.9	10
Input *RL* (dB)	> 10	> 9	> 10	> 14
Output *RL* (dB)	> 15	> 8	> 10	> 9
NF (dB)	2.4	2	3.4	3.4
IP_{1dB} (dBm)	-2	-2	1	-2
IIP_3 (dBm)	4.5	4	5	4
P_{DC} (mW)	9.8	10	9.8	10

Tab. 1. Performance comparison of low-noise amplifier with and without noise cancellation.

The third-stage downconverter is fabricated by the use of WIN GaAs HEMT foundry process with f_T up to 85 GHz. Both Gilbert mixers including and excluding a diode linearizer are implemented on the same chip with 3 mm × 2 mm. Fig. 5 shows the microphotograph of the downconverters. For the chip-on-PCB measurement, the transformer NCS4-232+ generated from Mini-Circuits is used as a passive balun for converting an incoming single-ended LO signal into a differential one with input impedance matched to 50 Ω. Similarly, an output IF differential signal is transformed into a signal-ended one with output impedance matched to 50 Ω by using a Mini-Circuits TC1-1-13M+ passive balun. The supply voltage of 2.5 V is used in the downconverter. The applied LO power is 0 dBm. Tab. 2 compares the performances of Gilbert mixers with and without linearization. As indicated in Tab. 2, a diode linearizer has increased the measured IIP_3 of the downconverter by 5.1 dB.

	with Linearization		without Linearization	
	Simulation	Measurement	Simulation	Measurement
CG (dB)	5.2	4.9	5.2	4.9
RF *RL* (dB)	> 10	> 10	> 10	> 11
LO *RL* (dB)	> 11	> 9	> 11	> 10
IF *RL* (dB)	> 10	> 7	> 10	> 8
NF (dB)	4.3	5.5	4.3	5.2
IP_{1dB} (dBm)	-0.5	-2.5	-6.5	-6.5
IIP_3 (dBm)	4.5	5	0.9	-0.1
P_{DC} (mW)	31	30	31	30

Tab. 2. Performance comparison of the Gilbert mixer with and without linearization.

The BPF-A410+ filter manufactured by Mini-Circuits is used as the fourth-stage IF BPF. Its input and output impedance are matched to 50 Ω. Within 365 MHz and 380 MHz, the measurement results of VSWR and insertion loss are below 1.43 and 2.9 dB, respectively, which meets the specifications given in the data sheet provided by Mini-Circuits [21].

Fig. 6 shows that the implemented RF front end HMIC has an area of 38 mm × 15 mm after integrating the individual components. Note that the IF BPF is arranged

on the reverse side of the PCB to reduce the size of the RF front end HMIC. The RF front end requires a three-port measurement setup to provide the RF signal and the LO carrier with power and frequency sweeps as input signals, and to generate the output IF signal. For comparison purposes, the RF front end with noise cancellation, i.e., transistor M_3 shown in Fig. 2 is turned on, and a diode linearizer is called the proposed RF front end while the RF front end without noise cancellation and a diode linearizer is called the conventional RF front end.

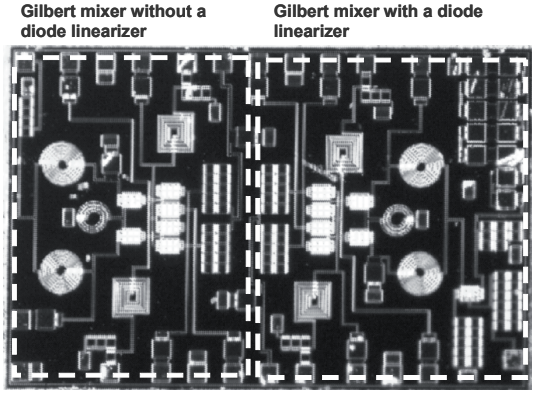
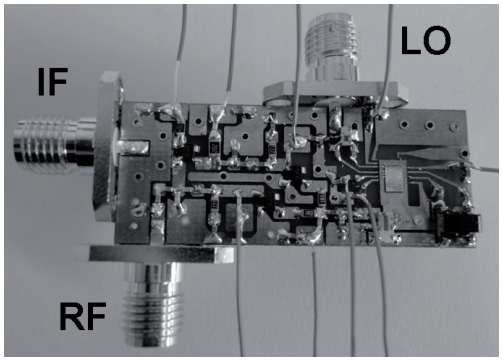
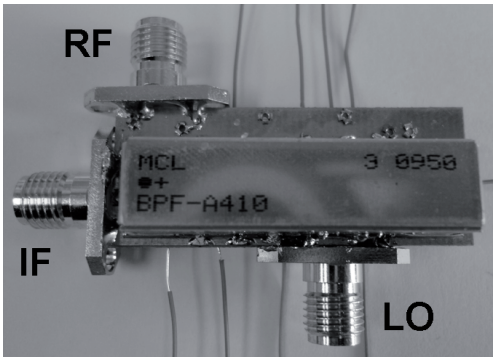


Fig. 5. Chip micrograph of the implemented two different WiMAX downconverters.



(a) Top view



(b) Back view

Fig. 6. Photo of the implemented RF front end HMIC.

Fig. 7 compares the results for the noise figure of the proposed and conventional RF front ends within the WiMAX MMDS band that covers frequencies from 2.5 to 2.69 GHz. The simulation results are generated by Agilent Advanced Design System (ADS). The *Y*-factor method is used for the noise figure measurement. The measured noise figure is obtained via a Noisecom NC346C noise source, an R&S SMBV100A vector signal generator, and an R&S FSV signal analyzer. The noise source requires a voltage of 28 V to be switched on as a hot source and 0 V to be switched off as a cold source. The R&S FSV signal analyzer needs to be calibrated in advance. The comparison shows good agreement with an average difference of 4% and 2% for the proposed and conventional RF front end, respectively. The average of the measured noise figure in the proposed RF front end is 3.6 dB. However, the average noise figure of the measurement in the conventional RF front end is 4.5 dB. Comparison of noise figure between the proposed and conventional RF front end shows that the proposed RF front end reduces the noise figure by 0.9 dB. The improved noise figure is mainly achieved by using a low-noise amplifier in the first stage of the RF front end which dominates the noise performance of the overall RF front end exploits a noise canceling technique to eliminate thermal noise.

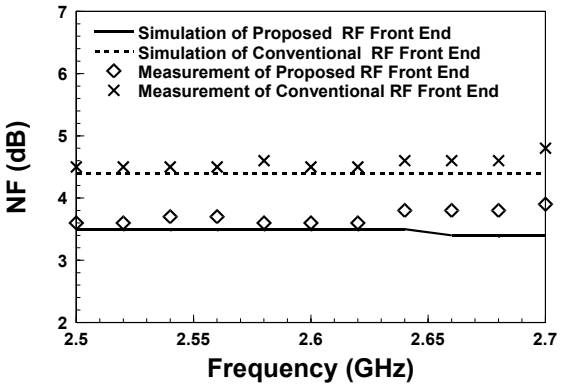


Fig. 7. Comparison of the noise figure in the proposed and conventional RF front ends.

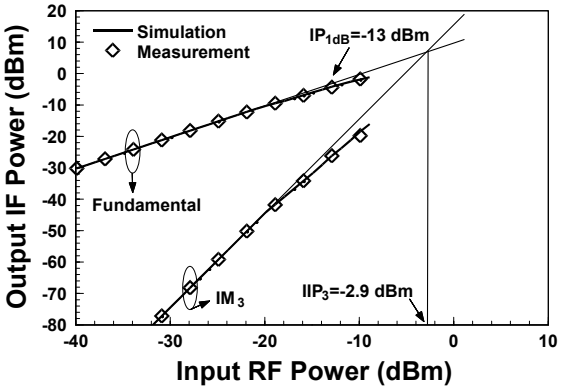


Fig. 8. Simulated and measured output powers for the fundamental and IM_3 products in the proposed RF front end.

The RF, LO, and IF frequencies are 2.6 GHz, 2.226 GHz, and 374 MHz, respectively. The frequency spacing in a two-tone test is set to 20 MHz which is the channel bandwidth in a WiMAX system. For the proposed RF front end, the output fundamental and IM_3 powers are plotted in Fig. 8 where the simulated and measured results

show good consistency with each other. Note that the test setup consists of an R&S SMBV100A vector signal generator, an R&S SMF 100A signal generator, and an R&S FSV signal analyzer. Fig. 8 shows that the gain and the IP_{1dB} of the proposed RF front end are 9.4 dB and -13 dBm, respectively. Fig. 8 also shows that the proposed RF front end has an IIP_3 of -2.9 dBm.

Fig. 9 shows the simulated and measured results for the output powers of fundamental and IM_3 products in the conventional RF front end. Again, the agreement is quite good. The conventional RF front end performs a gain of 9.2 dB and an IP_{1dB} of -17.5 dBm. Fig. 9 also indicates that the conventional RF front end achieves an IIP_3 of -7.2 dBm.

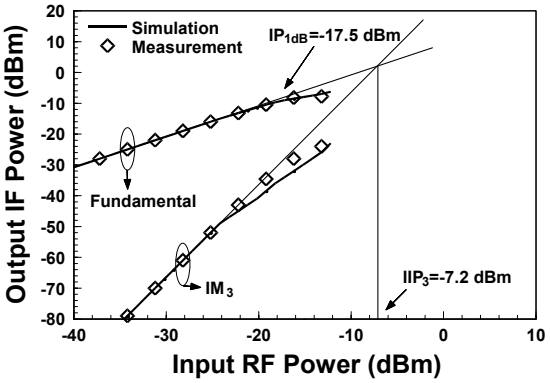


Fig. 9. Simulated and measured output powers for the fundamental and IM_3 products in the conventional RF front end.

A comparison of Figs. 8 and 9 shows that the IIP_3 of the proposed RF front end is higher than that of the conventional RF front end by 4.3 dB. The improvement is achieved by using a downconverter in the latter stage of the RF front end which dominates the linearity performance of the whole RF front end and uses a diode linearizer to increase the power level of the gain compression point.

As described in Section 2, the spurious-free dynamic range of an RF front end can be enhanced by reducing the noise figure or by increasing IIP_3. Fig. 7 shows a noise canceling technique has caused the noise figure to decrease by 0.9 dB. Additionally, a diode linearizer has caused IIP_3 to increase by 4.3 dB when compared Figs. 8 and 9. According to (3), this results in an enhancement of 3.5 dB in the spurious-free dynamic range due to the presence of the noise cancellation and linearization.

Fig. 10 compares the simulated gain with the measured results over the entire applied frequency range. Note that these gains are measured with an R&S ZVA 40 vector network analyzer and an R&S SMF 100A signal generator. Clearly, both proposed and conventional RF front ends maintain almost the same gain about 9 dB, which reveals the increase in the spurious-free dynamic range obtained by using noise cancellation and linearization but without loss of gain.

Tab. 3 summarizes the performance merits of this work and compares it with previous proposed designs for heterodyne RF front ends in [6], [8], and [10]. In Tab. 3, the values of IIP_3 and NF can be used to calculate the spurious-free dynamic range by referring to (3). The system bandwidth B in (3) is set to 1 Hz for convenient comparison between this and prior works. According to this comparison, the proposed design provides high dynamic range with a significantly low NF and high IIP_3.

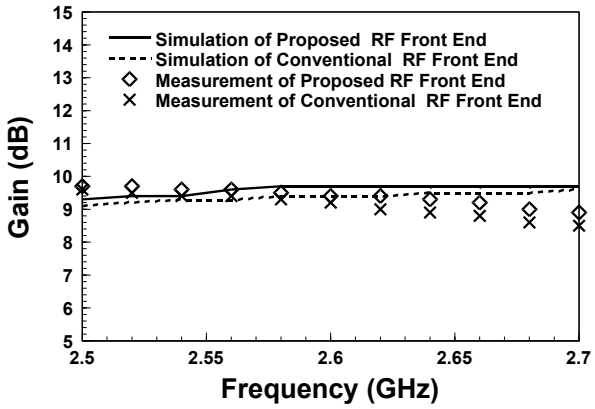


Fig. 10. Comparison of the gain in the proposed and conventional RF front ends.

	Proposed RF Front End	Conventional RF Front End	[6]	[8][b]	[10]
Freq. (GHz)	2.6	2.6	2	2.4	1
G (dB)	9.4[a]	9.2[a]	33[c]	18[c]	10.8
NF (dB)	3.6	4.5	4.7	7.5	4.8
IIP_3 (dBm)	-2.9	-7.2	-1	-13	-8
DR_f (dB)	111.7	108.2	112.2	102.3	107.5
P_{DC} (mW)	40	40	44.6	15.5	35.1

a: Including the insertion loss of passive baluns

b: Simulated results

c: Voltage gain

Tab. 3. Performance summary for this work and comparison with prior works.

5. Conclusions

A 2.6 GHz heterodyne RF front end HMIC featuring a noise canceling technique and a diode linearizer for WiMAX receivers has been presented. The main advantage is to extend the dynamic range of a conventional heterodyne RF front end substantially. After simulation with verification by measurement data, the resulting spurious-free dynamic range increases by 3.5 dB. The components responsible for this improvement are the first-stage low-noise amplifier and the latter-stage downconverter. The noise canceling technique has caused to reduce the noise figure of the low-noise amplifier by 1.4 dB, which improves the overall noise figure of the RF front end by 0.9 dB. The downconverter has obtained the increment in IIP_3 by 5.1 dB due to the presence of a diode linearizer, which increases the IIP_3 by 4.3 dB for the whole RF front end.

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About Authors ...

Jian-Ming WU was born November 13, 1974, in Kaohsiung, Taiwan. He received the B.S.E.E degree from the Yuan Ze University, Chungli, Taiwan, in 1997, and the M.S.E.E. and Ph.D. degrees from the National Sun Yat-Sen University, Kaohsiung, Taiwan, in 2000 and 2006, respectively. He joined the Graduate Institute of Communication Engineering, National University of Tainan, Tainan, Taiwan, as an assistant professor in 2006. In 2007, he joined the Department of Electronic Engineering, National Kaohsiung Normal University, Kaohsiung, Taiwan, as an assistant professor. His current research interests include design of monolithic microwave integrated circuit, modeling of RF components, and chip-package-board codesign. He was the recipient of the 2006 National Sun Yat-Sen University Outstanding Doctoral Dissertation Award. Since 2006, he has been serving on the IC Implementation Review Committee, National Chip Implementation Center, Hsinchu, Taiwan.

Chun-Hung YEH was born December 1, 1986, in Kaohsiung, Taiwan. He received B.S.E.E. degree from the National Kaohsiung Marine University, Kaohsiung, Taiwan, in 2009, and is currently working toward the M.S. degree

in electronic engineering, at the National Kaohsiung Normal University, Kaohsiung, Taiwan.

Ching-Jui CHUANG was born October 8, 1985, in Taoyuan, Taiwan. He received B.S.E.E. degree from the National Taiwan Ocean University, Keelung, Taiwan, in 2008, and is currently working toward the M.S. degree in electronic engineering, at the National Kaohsiung Normal University, Kaohsiung, Taiwan.

RADIOENGINEERING REVIEWERS II

June 2012, Volume 21, Number 2

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