# Low-Voltage Ultra-Low-Power Current Conveyor Based on Quasi-Floating Gate Transistors

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**Abstract.** *The field of low-voltage low-power CMOS technology has grown rapidly in recent years; it is an essential prerequisite particularly for portable electronic equipment and implantable medical devices due to its influence on battery lifetime. Recently, significant improvements in implementing circuits working in the low-voltage low-power area have been achieved, but circuit designers face severe challenges when trying to improve or even maintain the circuit performance with reduced supply voltage. In this paper, a low-voltage ultra-low-power current conveyor second generation CCII based on quasi-floating gate transistors is presented. The proposed circuit operates at a very low supply voltage of only ±0.4 V with rail-to-rail voltage swing capability and a total quiescent power consumption of mere 9.5 μW. Further, the proposed circuit is not only able to process the AC signal as it's usual at quasi-floating gate transistors but also the DC which extends the applicability of the proposed circuit. In conclusion, an application example of the current-mode quadrature oscillator is presented. PSpice simulation results using the 0.18 μm TSMC CMOS technology are included to confirm the attractive properties of the proposed circuit.*

## Keywords

Quasi-floating gate MOST, low-voltage low-power MOST, CCII, quadrature oscillator.

## 1. Introduction

Admittedly, the perpetual trends in CMOS technology towards increasing density of components on chip, continuous down-scaling of processes and prolonging the battery lifetime of portable and battery-powered equipment have shifted the research towards the low-voltage (LV) low-power (LP) area. The term "low-voltage low-power" has taken a leading role in analog circuit research over the past decade. Such research involves finding promising ways of making the whole analog system work in the LV LP area. Although the effort to reduce the voltage power supply to ever-lower values seems to be endless, the results achieved from this research are still controversial and fiercely debated. These controversial results have been coming up since the results achieved are not adequately balanced, i.e. the LV LP requirement can be fulfilled only at the expense of speed and accuracy of the circuit, and vice versa. However, designers should allocate priority to the most important parameters of their designs.

Actually, in modern LV LP analog circuit design the threshold voltages of standard CMOS technologies are an obstacle facing analog circuit designers. The threshold voltage values are not expected to be decreased much below what is available today. To overcome the threshold voltage, several techniques exist for LV LP analog circuit design [1], [2]. The vast majority of the recently published papers [3-27], [55], [57] show that the bulk-driven (BD) and floating-gate (FG) MOST techniques are good and attractive solutions used either to remove or to reduce the threshold voltage from the signal path in modern LV LP analog circuit design.

The floating-gate MOST technique is used to reduce the supply requirement in a number of new and interesting analog applications. The first well-known application of the FG MOST was to store data in EEPROMs, EPROMs and FLASH memories. The FG MOST can be fabricated in all CMOS technologies, although a double poly CMOS technology is preferred. These devices show potentials for analog signal processing, where they may find many applications [20], [21]. Several active elements in the analog mode have been designed using the FG technique, such as Op Amp [22], OTA [23-25], Transconductors [26], class AB output stage for CMOS Op-Amps [27], differential voltage current conveyor [55] and others.

The effective threshold voltage of the FG MOST can be lowered from its conventional value using an appropriate bias voltage to be applied at one of its input terminals through a large-value capacitance. Unfortunately, this large capacitance leads to an increase in the silicon area and a reduction of the effective transconductance and gain-bandwidth (GB) product [45], [49]. Besides, FG MOST can trap a significant amount of residual charge during the fabrication process, which may cause DC offsets if it is not removed using additional processing steps such as ultra-violet (UV) light; tunnel effect; hot electron injection; or setting an initial condition with a switch [21]. Hence the

quasi-floating gate (QFG) technique appears to be an alternative approach to overcome the above-mentioned drawbacks of FG MOST and thus the initial charge is no longer an issue [21], [49].

A variety of recent publications describe various attractive implementations of the QFG MOST technique in signal processing LV LP applications [45-49], [51]. Several low-voltage active elements have been designed utilizing the QFG MOST, such as the current mirror [45], differential amplifier [46], transconductor [47-49], second-generation current conveyor [51], and others.

It is worth mentioning that a similar QFG circuits to our proposed one are presented by the same authors in [50], [56]. Nevertheless, the QFG circuits proposed in [50], [56] have the following drawbacks: firstly each transistor of the differential pairs is connected to unnecessarily grounded capacitors ($C_2$) which in fact doesn't influence the circuit functionality but they just increase the total die size of the chip. Secondly, the way the DC voltage transfer characteristics ($V_X/V_Y$) were obtained is unclear since it's well-known that the QFG transistor cannot process DC signals. Furthermore, the proposed circuits have the following mistakes: at Fig. 1 (d) [56] the X terminal of the QFG-DVCC must be connected to the drains of $M_5$ and $M_6$ transistors rather than the gates, otherwise the circuit becomes non-functional. Other mistake appears at Fig. 3 [50] where transistors $M_6$ and $M_8$ operate in the cutoff region since their gate and drain terminals are tied together, hence the circuit is also non-functional.

Since the second-generation current conveyor is a versatile building block that could be used in many applications, we decided to design a class AB CCII based on QFG MOST able to operate at a very low supply voltage of only ±0.4 V with ultra low power consumption of a mere 9.5 μW. The proposed circuit exhibits rail-to-rail voltage swing capability. Technology accessibility, design simplicity, voltage supply value and total power consumption were taken into account while designing the proposed circuit.

The paper is organized as follows. In Section 2, the QFG MOST is presented while in Section 3, the LV LP CCII based on QFG folded cascode OTA and its main features are presented; its non-ideal model, simulation results, and their evaluations are given in detail. As an application example of the proposed LV LP CCII, a current-mode quadrature oscillator is presented in Section 4. Finally, Section 5 concludes the paper.

## 2. Quasi-Floating Gate MOST

Similarly to FG MOST the QFG MOST can also be fabricated in all CMOS technologies, although a double poly CMOS technology is preferred. Fig. 1(a) shows the symbol of a single-input QFG NMOS transistor, which is used in our design of the proposed circuit.

The floating gate of the QFG MOST is weakly connected to a proper bias voltage using a large-value resistor $R_{large}$, which is usually implemented by a large resistance of a reverse-biased junction of a diode-connected MOS transistor ($M_R$) operating in the cutoff region as shown in Fig. 1(b). The equivalent circuit of Fig. 1(b) is shown in Fig. 1(c).

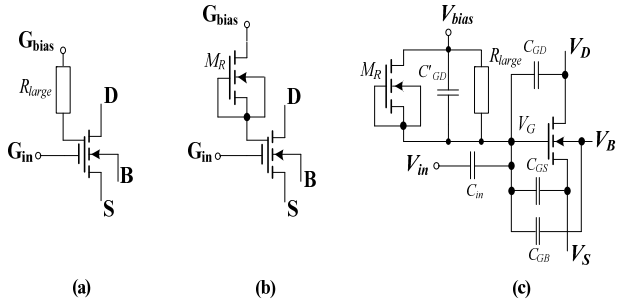


**Fig. 1.** Single input QFG MOST: a) symbolic with $R_{large}$, b) symbolic with $M_R$, c) equivalent circuit of (b).

The input terminal ($G_{in}$) is capacitively coupled to the quasi-floating gate just like in the FG MOST case, but the DC gate voltage is set independently of the DC level of the input voltage. Concerning the AC voltage at the floating gate, it is in the s-domain [21], [49]:

$$V_G = \frac{sR_{large}}{1+sR_{large}C_{total}}(C_{in}V_{in} + C_{GD}V_D + C_{GS}V_S + C_{GB}V_B) \quad (1)$$

where $C_{total}$ is the total capacitance, and is given by:

$$C_{total} = C_{in} + C_{GD} + C_{GS} + C_{GB} + C'_{GD} \quad (2)$$

where $C_{GD}$, $C_{GS}$, $C_{GB}$ denote the capacitances from gate to drain, source and bulk, respectively. $C'_{GD}$ denotes the capacitances from gate to drain of the $M_R$ transistor.

The relation between the effective transconductance of the QFG MOST ($g_{m,eff}$) and the transconductance of MOST ($g_m$) is given by:

$$g_{m,eff} = \frac{C_{in}}{C_{total}} g_m . \quad (3)$$

As can be observed from (1), the input is a high-pass filter with cut-off frequency:

$$f_c = \frac{1}{2\pi R_{large}C_{total}} . \quad (4)$$

The value of the cut-off frequency is very low, in the range of sub-hertz, as long as $R_{large}$ remains large enough (in the order of Giga-Ohms) in order not to influence the circuit operation at the lowest frequency required [45], [49]. The exact value of $R_{large}$ is unimportant [49].

In general, attention must be paid to a drawback of the QFG technique that could arise in feed-forward applications. The gate voltage of the QFG MOST ($V_G$) must not

exceed the rail by more than the cut-in voltage of the p-n junction diode-connected MOST realizing the $R_{large}$, so that it does not become forward-biased [21]. However, this drawback is not the case of our proposed circuit.

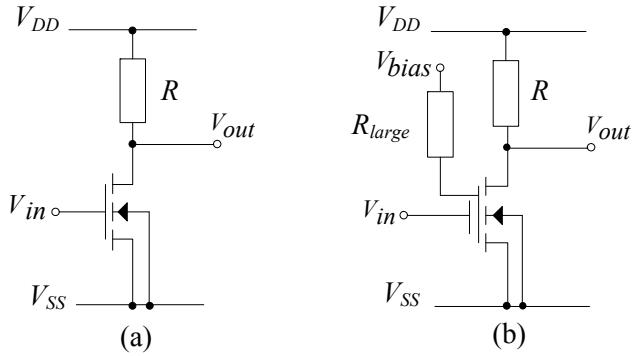


**Fig. 2.** Common-source amplifier: conventional gate-driven (a) and QFG MOST (b).

Fig. 2 shows the principle of the common-source amplifier based on a conventional gate-driven MOST (a) in comparison with the quasi-floating gate MOST (b), whereas their drain currents versus gate-source voltages are shown in Fig. 3.

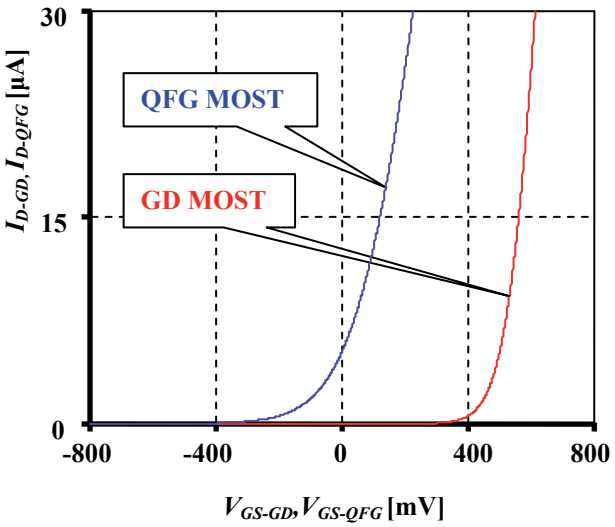


**Fig. 3.** Drain currents versus gate-source of GD MOST and QFG MOST voltages.

It is obvious that the drain current in a conventional gate-driven (GD) MOST increases when the gate-source voltage exceeds the threshold voltage. This is not the case of the quasi-floating gate MOST, where the threshold voltage is completely removed from the signal path and the transconductance value is almost the same as for the conventional MOST.

## 3. CCII Based on Quasi-Floating Gate MOSTs

The CCII is a three-terminal device that was first presented by Sedra and Smith [30]. The ideal CCII is defined by the following hybrid matrix:

$$\begin{pmatrix} V_X \\ I_Z \\ I_Y \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \end{pmatrix} \tag{5}$$

where X and Y are the input terminals and Z is the output terminal. The impedance level of the X terminal is zero whereas the Y and Z terminals have infinite internal impedances for the ideal CCII.

The LV LP class AB CCII based on folded cascode OTA is shown in Fig. 4. The folded cascode topology was chosen for the operational transconductance amplifier design because of its higher bandwidth and gain potential and also larger input common-mode range in comparison with the two-stage OTA topology [52], [53].

The CCII consists of a folded cascode OTA ($M_1$-$M_{11}$, $M_{8c}$-$M_{11c}$) with unity gain feedback used to obtain the unity gain buffer between the Y and X terminals. The input stage of the QFG-OTA consists of N-MOST QFG differential pairs $M_1$ and $M_2$, whose gate terminals are connected to $V_{DD}$ using the large resistance of a reverse-biased junction of a diode-connected MOS transistor $M_{R1}$ and $M_{R2}$, respectively, operating in the cut-off region. Similarly, $M_{R3}$ and $M_{R4}$ have large-value resistances, which are connected in parallel to the input capacitors $C_{in1}$ and $C_{in2}$, respectively, the benefit of this connection is that the QFG transistors can process DC signals as well. Transistors $M_6$ and $M_7$ provide a level shift function, and the cascoded current mirror ($M_8$, $M_9$, $M_{8c}$, $M_{9c}$) provides a differential to single-ended conversion. The folded version requires two additional current sources, $M_3$ and $M_4$, to provide the current necessary for the input and output branches. Transistors ($M_{10}$, $M_{10c}$) and ($M_{11}$, $M_{11c}$) form the second stage of OTA. The second part of the CCII is the branch containing the transistors ($M_{12}$, $M_{12c}$) and ($M_{13}$, $M_{13c}$), which are identical to ($M_{10}$, $M_{10c}$) and ($M_{11}$, $M_{11c}$), respectively, therefore $I_Z = I_X$. Transistors ($M_{12c}$, $M_{13c}$) are used here to increase the output resistance of the Z terminal.

Compensation capacitor will be required to ensure stability. Therefore a capacitor $C_C$ has been added to form a compensation network between the first and the second stage of the folded cascode OTA. Transistors $M_{b1}$-$M_{b3}$ with $I_{bias}$ form the necessary voltage and current biases for the first stage of the folded cascode OTA.

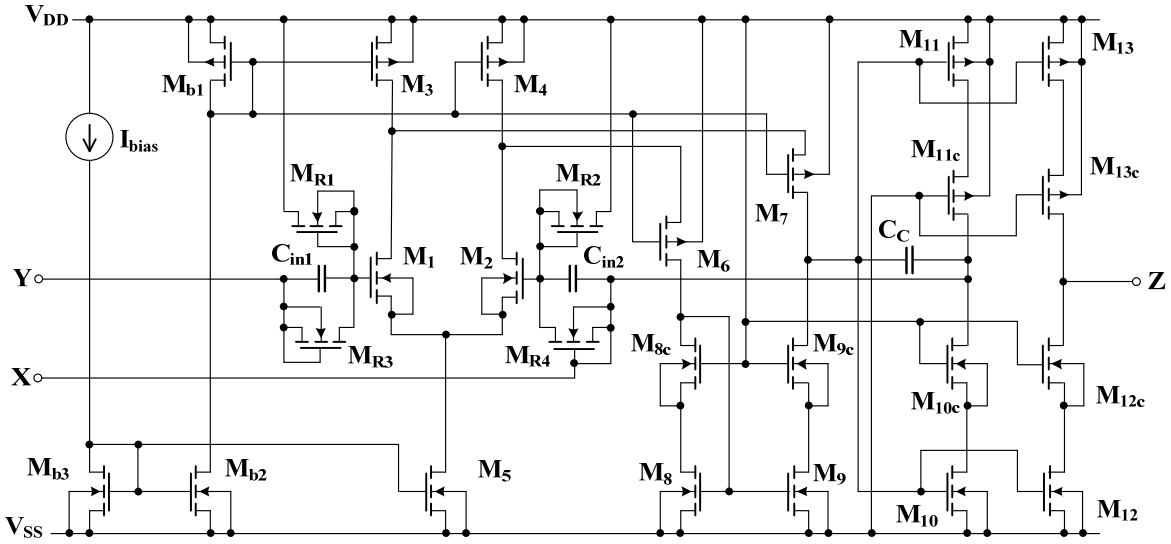


**Fig. 4.** CMOS implementation of the LV LP class AB CCII based on quasi-floating gate transistors.

It is worth noting here that some applications require additional Z+ or Z- terminals. They can be added as follows: the number of Z+ terminals can be arbitrarily increased simply by using the current mirror technique, while a cross-coupled current mirror technique or a suitable connection of more CCIIs could be utilized to achieve the Z-terminals [42], [44]. These various possible implementations of the Z terminals do not affect the parameters of X, Y, and the original Z+ terminals.

## 3.1 Non-Ideal Model of CCII

A detailed model of non-ideal current conveyor is presented in [31], [32], [41], [52]. Fig. 5 illustrates the non-ideal model of the CCII characterized by parasitic internal impedances of terminals and frequency-dependent voltage (VF) and current (CF) followers.

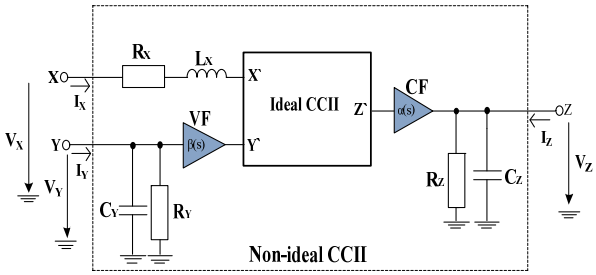


**Fig. 5.** Model of non-ideal CCII.

This non-ideal model is characterized by the following matrix:

$$\begin{pmatrix} V_X \\ I_Z \\ I_Y \end{pmatrix} = \begin{pmatrix} \beta(s) & Z_X & 0 \\ 0 & \alpha(s) & 1/Z_Z \\ 1/Z_Y & 0 & 0 \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \end{pmatrix} \tag{6}$$

The parasitic impedance at terminal X has a resistive behavior at lower frequencies and an inductive behavior at higher frequencies. The total X terminal parasitic impedance $Z_X$ then consists of a serial combination of $R_X$ and $L_X$. The value of $L_X$ can be determined by:

$$L_X = \frac{R_X}{2\pi f_{X,+3dB}} \tag{7}$$

where $f_{X,+3d}$ denotes the cut-off frequency of $Z_X$.

At terminal Y, a parasitic impedance $Z_Y$ appears; it consists of a parallel combination of $R_Y$ and $C_Y$. $R_Y$ is the value of the impedance at a low frequency. The value of $C_Y$ is then computed from the -3 dB cut-off frequency $f_{Y,-3dB}$.

$$C_Y = \frac{1}{2\pi f_{Y,-3dB} R_Y}. \tag{8}$$

At terminal Z, parasitic impedance $Z_Z$ can be modeled as a parallel connection of resistance $R_Z$ and capacitance $C_Z$. Here, $R_Z$ is the value of the impedance at a low frequency. The value of $C_Z$ is then computed from the -3 dB cut-off frequency $f_{Z,-3dB}$.

$$C_Z = \frac{1}{2\pi f_{Z,-3dB} R_Z}. \tag{9}$$

The voltage and current transfers of the CCII are given by $\beta(s)$ and $\alpha(s)$, respectively:

$$\beta(s) = \frac{\beta_0}{1 + s/\omega_\beta}, \tag{10}$$

$$\alpha(s) = \frac{\alpha_0}{1 + s/\omega_\alpha} \tag{11}$$

where $\beta_0$ and $\alpha_0$ are the values of these transfers at low frequencies, with $\omega_\beta$ and $\omega_\alpha$ representing their corresponding poles. We can also write $\beta_0 = 1 - \varepsilon_v$ and $\alpha_0 = 1 - \varepsilon_i$, where $\varepsilon_v$ and $\varepsilon_i$ ($|\varepsilon_v| << 1$ and $|\varepsilon_i| << 1$) represent the voltage and current tracking errors of the CCII, respectively.

From the small-signal equivalent circuit, a straightforward analysis brings the following expression for $\beta_0$ and $\alpha_0$ [42]. The voltage transfer ratio $\beta_0$ is:

$$\beta_0 = \frac{V_X}{V_Y} = \frac{g_{m,effM1} r_{out1} (g_{mM10} + g_{mM11}) r_{out2}}{1 + (g_{m,effM2} r_{out1} (g_{mM10} + g_{mM11}) r_{out2})} \approx \frac{g_{m,effM1}}{g_{m,effM2}} \approx 1 \quad (12)$$

where $r_{out1}$ and $r_{out2}$ are the output impedances of the first and second stages of OTA, and are given by:

$$r_{out1} = \frac{1}{\frac{g_{oM9c} g_{oM9}}{g_{mM9c}} + \frac{g_{oM7}(g_{oM3} + g_{oM1})}{g_{mM7} + g_{mbM7}}}, \quad (13)$$

$$r_{out2} = \frac{1}{\frac{g_{oM10} g_{oM10c}}{g_{mM10c}} + \frac{g_{oM11} g_{oM11c}}{g_{mM11c} + g_{mbM11c}}}. \quad (14)$$

The current transfer ratio $\alpha_0$ is:

$$\alpha_0 = \frac{I_Z}{I_X} \approx \frac{g_{mM12} + g_{mM13}}{g_{mM10} + g_{mM11}} \approx 1. \quad (15)$$

The Y terminal impedance of the proposed CCII is very high, because the inputs of QFG MOSTs are used as the input of the amplifier stage. The resistances of the remaining terminals X and Z are as follows:

$$R_X = \frac{1}{g_{m,effM1}(g_{mM10} + g_{mM11}) r_{out1}}, \quad (16)$$

$$R_Z = \frac{1}{\frac{g_{oM12} g_{oM12c}}{g_{mM12c}} + \frac{g_{oM13} g_{oM13c}}{g_{mM13c} + g_{mbM13c}}}. \quad (17)$$

It is worth noting here that the $R_Z$ achieves high values thanks to using the cascoded transistors ($M_{12c}$, $M_{13c}$). Therefore, the output current remains unaffected by the load. In (12)-(17) the $g_m$, $g_{m,eff}$ and $g_{mb}$ denote the gate, effective and bulk transconductances, respectively, and $g_o$ is the output conductance of the transistor.

## 3.2 Simulation Results

Tab. 1 summarizes the main characteristics of the proposed LV LP CCII circuit, whereas the optimum transistor aspect ratios are given in Tab. 2.

| Characteristics | Simulated results |
|---|---|
| Quiescent power consumption | 9.5 µW |
| DC current range | -75 µA to +75 µA |
| Input voltage range | -400 mV to +400 mV |
| 3dB bandwidth $I_Z/I_X$ | 26 MHz |
| Current gain $I_Z/I_X$ | 1 |
| 3dB bandwidth $V_X/V_Y$ | 26 MHz |
| Voltage gain $V_X/V_Y$ | 1 |
| Node X parasitic impedances: $R_X$, $L_X$ | 15 Ω, 162 µH |
| Node Y parasitic impedances: $R_Y$, $C_Y$ | 2.34 GΩ, 0.17 pF |
| Node Z parasitic impedances: $R_Z$, $C_Z$ | 6.24 MΩ, 50 fF |
| Measurement condition: $V_{DD} = -V_{SS} = 400$ mV, $I_{bias} = 1.6$ µA | |

**Tab. 1.** Simulation results for the LV LP class AB CCII.

| CCII | W/L [µm/µm] |
|---|---|
| $M_1$, $M_2$ | 6/0.5 |
| $M_3$, $M_4$ | 13/1 |
| $M_5$ | 8/0.6 |
| $M_{b1}$ | 6/1 |
| $M_6$, $M_7$ | 20/1 |
| $M_8$, $M_9$ | 8/1 |
| $M_{10}$, $M_{12}$, $M_{10c}$, $M_{12c}$ | 10/0.5 |
| $M_{8c}$, $M_{9c}$, $M_{b2}$, $M_{b3}$ | 2/1 |
| $M_{11}$, $M_{13}$, $M_{11c}$, $M_{13c}$ | 30/0.5 |
| $M_{R1}$, $M_{R2}$, $M_{R3}$, $M_{R4}$ | 5/1 |
| $C_{in\text{-}M1,M2}$=0.5 pF, $C_c$=0.01 pF | |

**Tab. 2.** Component values and transistor aspect ratios from Fig. 4.

The simulation results of the proposed LV LP CCII based on folded cascode OTA are shown in Figs 6 to 10.

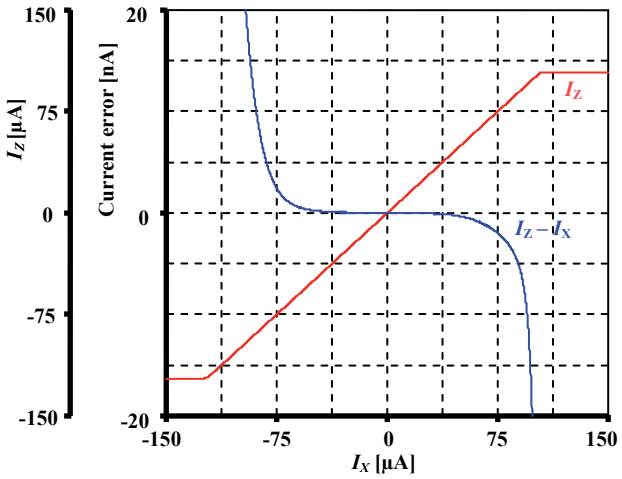


**Fig. 6.** DC curve $I_Z$ versus $I_X$ and the current error.

Fig. 6 shows the $I_Z$ curve vs. $I_X$ and the current error of the LV LP CCII, simulated on the condition that the Y terminal is grounded. Note that for input current $I_X$, the boundary of linear operation is in the range of [-100 to +100] μA. For a current range of [-75 to +75] μA the current error is only in the range from [2.45 to -2] nA. However, this DC range of linear operation is suitable for many applications that need extra low power consumption and high precision.

Fig. 7 shows the $V_X$ vs. $V_Y$ DC curve with rail-to-rail swing capability [-400 to +400] mV and the voltage error. Due to the use of the OTA with unity gain feedback, this topology ensures a low tracking error between the Y and X terminals. This voltage error is only in the range from [750 to -20] μV.

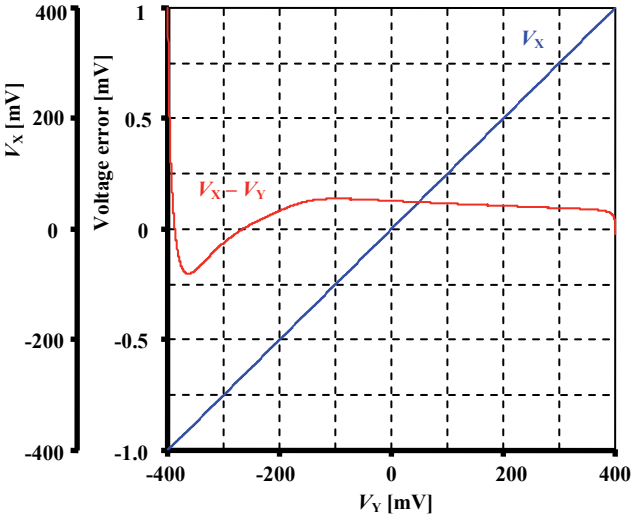


**Fig. 7.** $V_X$ versus $V_Y$ shows the rail-to-rail swing capability and the voltage error.

The frequency responses of the voltage $V_X/V_Y$ and current $I_Z/I_X$ gains are given in Fig. 8. The corresponding small-signal gains $V_X/V_Y = I_Z/I_X = 1$. The cut-off frequency for both gains is 26 MHz.

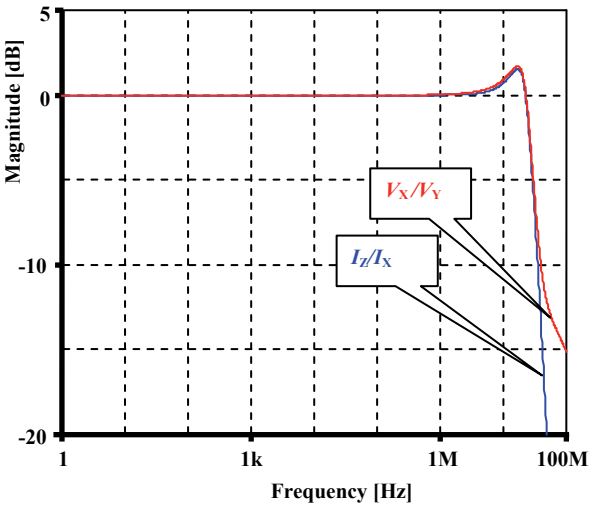


**Fig. 8.** Frequency responses of current and voltage gains.

Fig. 9 shows the frequency dependence of the parasitic impedances of terminals X and Z. The low-frequency values of these impedances are 15 Ω and 6.24 MΩ, respectively, and they remain constant up to about tens and hundreds of kilohertz, respectively. Then the impedance of the X terminal increases due to the frequency dependence of the folded cascode OTA transconductance, whereas the impedance of the Z terminal decreases due to the parasitic capacitance $C_Z$.

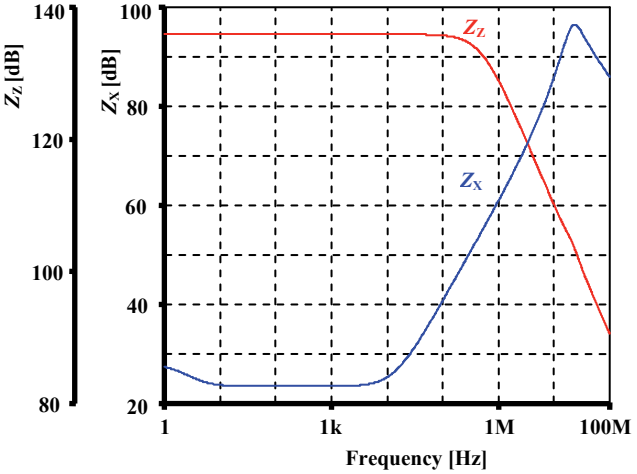


**Fig. 9.** Frequency dependence of parasitic impedance of X and Z terminals.

Fig. 10 shows the drain current of transistor $M_{R1}$ versus $V_Y$ for temperatures of 0, 27, 60 °C. Since the value of drain current is in the range from 0 to 73 pA, it can be neglected.

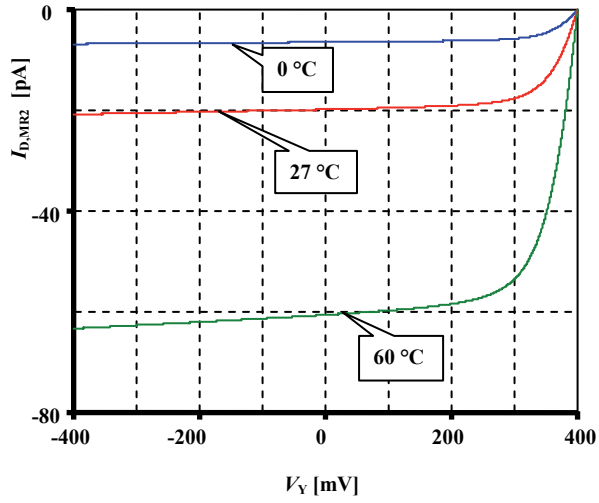


**Fig. 10.** Temperature analysis of drain current of $M_{R2}$ vs. $V_Y$.

Based on our survey of the most recently published papers related to LV LP CCII, their implementations are based on the conventional gate-driven transistors [33-40], bulk-driven technique [52] and floating-gate transistors [53]. Therefore, a comparison with our proposed circuit will be drawn here. Results reported in some references are as follows: [33] the supply voltage is ±0.75 V, power consumption is 1.62 mW, X-node parasitic impedance is

2.53 Ω, and Z-node parasitic impedance is 119.8 MΩ; [34] supply voltage ±1 V, X-node parasitic impedance 22.8 Ω, and Z-node parasitic impedance 12.563 kΩ; [35] supply voltage ±0.75 V, X-node parasitic impedance 6 Ω; [36] supply voltages ±1.5 V, X-node parasitic impedance 286 Ω, and Z-node parasitic impedance 45 MΩ; [37] supply voltage 1.5 V; [38] supply voltage ±1.5 V, X-node parasitic impedance 15 Ω; [39] supply voltage 3.3 V, X-node parasitic impedance 42 Ω, and parasitic output impedance at Z terminal 2.24 MΩ; [40] supply voltage ±3 V; [52] supply voltage ± 0.4 V, power consumption 0.064 mW, X-node parasitic impedance 27 Ω, and parasitic output impedance at Z terminal 0.89 MΩ; [53] supply voltage ± 0.5 V, power consumption 0.01 mW, X-node parasitic impedance 42 Ω, and parasitic output impedance at Z terminal 53 MΩ.

In comparison with our results, it is obvious that our CCII has many attractive features. These valuable features make our circuit preferentially utilized in many applications that need a low-voltage and extremely low-power consumption with an acceptable bandwidth range. It is worth noting that circuits needed for processing biological signals are a typical and good example of LV LP circuits due to the fact that the main features of biological signals are low amplitude and a low frequency range, which is limited to a few kHz [28], [29].

Tab. 3 illustrates in detail the performance comparison of our proposed LV LP QFG-CCII with other LV LP CCIIs and high-precision CCIIs based on conventional gate-driven MOST in [33-35], bulk-driven MOST in [52] and floating gate MOST in [53]. The low supply voltage, rail-to-rail voltage swing capability, high-precision, and the extremely low power consumption make our proposed circuit unique.

# 4. Example of Application

As an application example of the proposed LV LP CCII we have designed a current-mode quadrature oscillator as shown in Fig. 11. The circuit generates two harmonic signals with a 90 degree phase shift. Quadrature oscillators are frequently used circuits, e.g. in telecommunications for quadrature mixers, digital modulators and demodulators, etc.

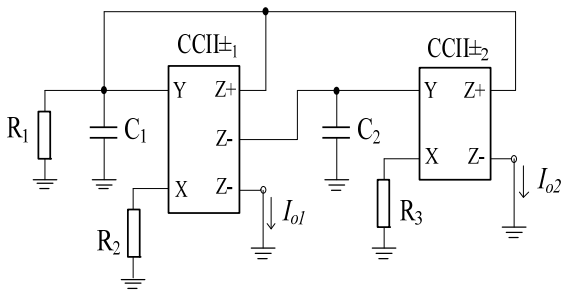


**Fig. 11.** Quadrature oscillator with LV LP class AB CCII.

The quadrature oscillator employs two conveyors CCII± with multiple output terminals. The negative output terminals (Z-) of these conveyors have been obtained simply by connecting the proposed CCII+ with a current follower (formed by another CCII+ with the Y terminal grounded), as presented, for example, in [44]. The other Z-terminal has been created simply by the current mirror technique.

The oscillator employs five passive elements; all of them are grounded, which is advantageous for integrated circuit implementation. Both of the circuit outputs are of high impedance and thus the oscillator can be loaded by arbitrary finite impedance. The characteristic equation (CE) of the oscillator is:

$$s^2 C_1 C_2 R_1 R_2 R_3 + sC_2 R_3 \left(R_2 - R_1\right) + R_1 = 0 . \quad (18)$$

The oscillation condition and oscillation frequency $\omega_0$ can be written as:

$$R_2 = R_1 , \quad (19)$$

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_2 R_3}} . \quad (20)$$

It is apparent that the oscillation condition (19) can be set by the resistance $R_1$ without affecting the oscillation frequency $\omega_0$. To tune the oscillation frequency independently of the oscillation condition, we can change one or multiple parameters from the group $C_1$, $C_2$, $R_3$.

The following relation is valid between the two output currents:

$$I_{O1} = -sC_2 R_3 I_{O2} = \omega_0 C_2 R_3 e^{-j90^\circ} I_{O2} \quad (21)$$

which means that the phase difference between $I_{O1}$ and $I_{O2}$ is ideally –90 degrees under sinusoidal steady state, i.e. the output currents are in quadrature. The amplitude ratio of output signals is:

$$\frac{I_{O1}}{I_{O2}} = \sqrt{\frac{C_2 R_3}{C_1 R_2}} . \quad (22)$$

With the resistances and capacitances chosen as $C_1 = C_2$ and $R_2 = R_3$, the output amplitudes are equal.

## 4.1 Influence of Conveyor Non-Idealities and Circuit Sensitivities

The gains and terminal impedances of the single-output conveyor can be expressed symbolically as illustrated by (6). It is easy to extend the equation to the multiple-output CCII± that is used in the oscillator. The current gain between X and Z+ will be labeled as $\alpha_+$ and between X and Z– as $\alpha_-$. The internal impedances of positive and negative

| Parameter | [33] CCII± | [34] CCII± | [35] CCII+ | [53] CCII+ | [52] CCII± | Proposed CCII+ |
|---|---|---|---|---|---|---|
| Power consumption (mW) | 1.62 | – | 0.123 | 0.01 | 0.064 | 0.0095 |
| Voltage supply (V) | ±0.75 | ±1 | ± 0.75 | ±0.5 | ±0.4 | ±0.4 |
| 3dB bandwidth $I_{Z+}/I_X$, $I_{Z-}/I_X$ (MHz) | 100 | – | 6.2 | 8.2 | 13, 12.5 | 26 |
| Input voltage range (mV) | – | – | -650 to 650 | -500 to 500 | -380 to 380 | -400 to 400 |
| Offset voltage variation (mV) | – | – | – | 0.418 to -0.798 | -0.4 to 0.5 | 0.75 to -0.02 |
| DC current range (mA) | – | – | -1 to 1 | -0.03 to 0.03 | -0.007 to 0.007 | -0.075 to 0.075 |
| Offset current variation (nA) | – | – | – | 0.116 to -30, – | -0.9 to 0.4 -0.17 to 0.2 | 2.45 to -2 |
| Current gain $I_{Z+}/I_X$, $I_{Z-}/I_X$ | – | – | 0.995 | 1 | 1 | 1 |
| 3dB bandwidth $V_X/V_Y$ (MHz) | – | – | 10.5 | 4.8 | 14 | 26 |
| Voltage gain $V_X/V_Y$ | – | – | 0.998 | 1 | 1 | 1 |
| Node X parasitic impedance: $R_X$ (Ω) | 2.53 | 22.8 | 6 | 42 | 27 | 15 |
| Node Y parasitic impedance: $R_Y$ (kΩ) | ≈∞ | ≈∞ | – | ≈∞ | ≈∞ | ≈∞ |
| Node Z parasitic impedance: $R_Z$ (MΩ) | 119.8 | 0. 12563 | – | 53 | 0.89 | 6.24 |
| Technology | 0.5 μm | 0.13 μm TSMC | 0.35 μm | 0.18 μm TSMC | 0.18 μm TSMC | 0.18 μm TSMC |

**Tab. 3.** Performance comparison of the proposed LV LP CCII with LV LP CCIIs and high-precision CCIIs in the literature.

Z terminals will be considered equal ($Z_{Z\pm}$). The ideal case is $\beta = 1$, $\alpha_+ = -\alpha_- = 1$ (the complex variable ($s$) at the gains will be omitted below), $Z_X = R_X + sL_X = 0$ Ω, $Y_{Z\pm} = 1/Z_{Z\pm} = 1/R_Z + sC_Z = 0$ S, and $Y_Y = 1/Z_Y = 1/R_Y + sC_Y = 0$ S. We assume that the non-idealities are equal for both conveyors. Simulations have shown that it is enough to take into account only the following parts of conveyor internal impedances: $R_X$, $C_Y$, and $C_Z$. Other parts do not have any significant influence on the oscillator behavior or are close to their ideal values due to the proper conveyor design. To show the influence of the conveyor non-idealities (gains and impedances) on the oscillator, we can rewrite the characteristic equation:

$$\begin{aligned} &s^2\left(C_1+2C_Z+C_Y\right)\left(C_2+C_Z+C_Y\right)R_1\left(R_2+R_X\right)\\ &\left(R_3+R_X\right)+s\left(R_3+R_X\right)\left(C_2+C_Z+C_Y\right)\\ &\left(R_2+R_X-R_1\beta\alpha_+\right)-R_1\beta^2\alpha_+\alpha_-=0 \end{aligned} \tag{23}$$

The oscillation condition is expressed as:

$$R_2 + R_X = R_1\beta\alpha_+ . \tag{24}$$

The oscillation frequency is modified to:

$$\omega_0 = \beta \sqrt{\frac{-\alpha_+\alpha_-}{\left(C_1+2C_Z+C_Y\right)\left(C_2+C_Z+C_Y\right)\left(R_2+R_X\right)\left(R_3+R_X\right)}} \tag{25}$$

The oscillation condition can be still set by the resistance $R_1$ independently of the oscillation frequency. The influence of conveyor gains is clearly apparent from the relations. It is also seen that the original values of oscillator resistances $R_2$ and $R_3$ are simply increased by $R_X$, and filter capacitances are also increased by the respective terminal capacitances parallel to them. This causes a decrease of $\omega_0$. But it is easy to pre-distort the original parameters of passive oscillator elements to compensate for the influence of the parasitic impedances of the conveyor in question.

## 4.2 Simulation

To verify the functionality of the proposed oscillator and the theoretical results, a PSpice simulation was carried out. The transistor-level model of the LV LP CCII shown in Fig. 4 was used. The passive element parameters chosen were $C_1 = C_2 = 1$ nF, $R_2 = R_3 = 15\,920$ Ω, and $R_1 = 16$ kΩ, which is slightly higher than the value 15 920 Ω computed from oscillation condition (19). This is to ensure that the oscillations would start. The theoretical oscillation frequency is $f_0 = \omega_0/2\pi = 10$ kHz.

The growing oscillations and the steady-state waveforms of the output currents are shown in Figs. 12 and 13, respectively. Fig. 14 shows the spectrum of the oscillator output currents.

The simulated oscillation frequency is in agreement with the theoretical value. The THD is 0.20 % for $I_{O1}$ and 0.43 % for $I_{O2}$. The total power consumption of the proposed oscillator is only 33 μW.

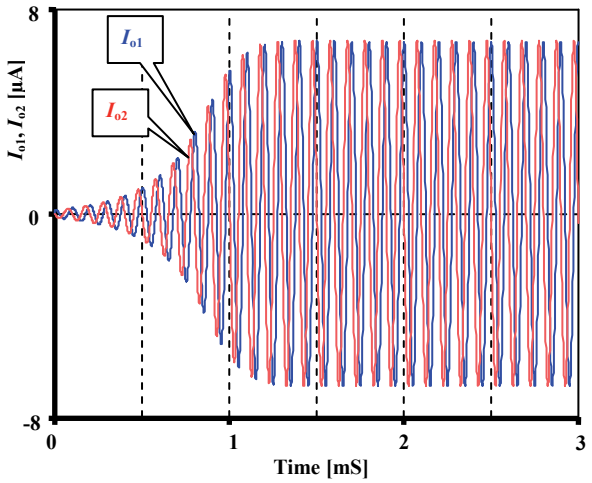


**Fig. 12.** Growing oscillations of the quadrature oscillator output currents.

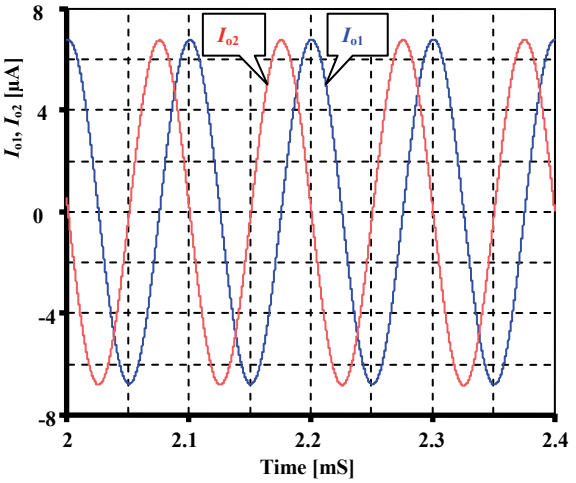


**Fig. 13.** Steady-state waveforms of the quadrature oscillator output currents.

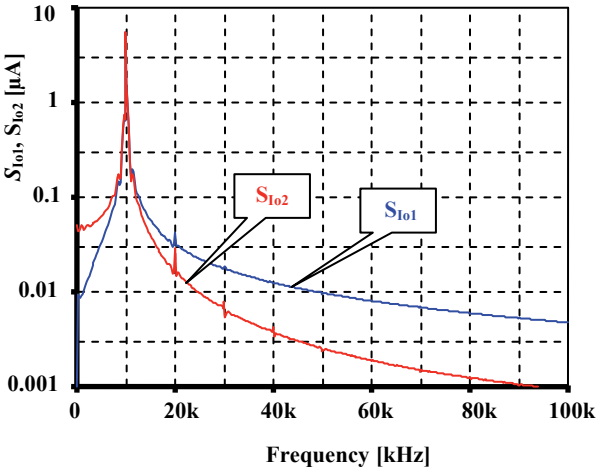


**Fig. 14.** Spectrum of the oscillator output currents.

# 5. Conclusion

In this paper we have proposed a LV LP CCII based on the quasi-floating gate MOST. The simulation results have been used to validate the theoretical predictions. The low supply voltage, rail-to-rail voltage swing capability, high-precision, and the extremely low power consumption make our proposed circuit unique in comparison with papers published up to now.

Finally, the proposed LV LP CCII was successfully utilized in a current-mode quadrature oscillator. The circuit exhibits several advantages such as: only grounded passive elements are used, high-impedance current outputs, and the possibility of independent setting of oscillation condition and frequency. Simulations in the PSpice environment verified a precise oscillation frequency, low THD and low power consumption.

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