

A Modified Bipolar Translinear Cell with Improved Linear Range and Its Applications

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Abstract. *This paper presents a technique to extend the linear input voltage range of a sinh mixed translinear cell proposed by Fabre [1]. This technique extends the linear operation range of the circuit by inserting common-anode-connected pairs into the mixed translinear cell. Then the relationship between the output current and the input voltage is developed to be linear. The transconductance gain can be adjusted electronically while keeping its linearity. The performance of the proposed circuit is verified by mathematical analysis and by SPICE simulations. Finally, applications of the proposed cell in a floating resistor and a CCCII for designing an instrumentation amplifier are presented.*

Keywords

Analog Integrated Circuit, Translinear Circuit, Linearization, Transconductance.

1. Introduction

The sinh mixed translinear cell [1] as described in Fig. 1 is a useful function block for analog signal processing since it is a combined voltage/current mode device which can be used to realize tunable transconductors without additive resistances. One familiar application is used for input front end of a second-generation current controlled conveyor (CCCII) [2] and an operational transconductance amplifier (OTA) [3], [4]. It can also be used as current controlled floating and/or grounded resistor [5], [6], [7] to help setting the operating condition in an electronic circuit such as oscillatory conditions in an oscillator circuit. However, the voltage-to-current characteristic (V - I characteristic) of this circuit is expressed as a hyperbolic sine function [8]. Thus the linear operation range is quite narrow. One of the technique to improve V - I characteristic is the multi-sinh technique [9]. The

main disadvantage of this technique is that the linear operation range increases with the number of series connected diodes which increases the chip area and the power consumption. Hence, in this paper, we propose a novel technique to extend the linear operating range of the sinh mixed translinear cell by adding common-anode-connected pairs into translinear circuits in order to provide a biasing current for transistors. This technique requires additional chip area for four additional transistors and increase the power consumption slightly. The proposed circuit is suitable for IC implementation and its electronically tunable features make it appealing for practical applications. Simulation results obtained confirm the validity of the theoretical analysis of the proposed design, in particular that the proposed principle improves the linearity of the sinh mixed translinear cell.

The organization of this paper is as follows. A review of mixed translinear cell is described in Section 2. In Section 3, the proposed mixed translinear cell with additional common-anode-connected pairs into the translinear loop is shown. First, the extended linear input range is derived using mathematical approaches. The theoretical results are then verified using simulations. The outcomes of the simulations are shown in Section 4. In Section 5, a floating resistor and the CCCII for design an instrumentation amplifier are demonstrated as an example of applications for the proposed mixed translinear cell. Finally, our work is concluded in Section 6.

2. Review of Mixed Translinear Cells

The schematic of the mixed translinear cell as proposed in [1] is shown in Fig. 1. For a small difference of input voltage, for example $|V_{YX}| < V_T$, where $V_T \approx 26$ mV is the thermal voltage at 27°C, all BJT transistors ($Q_1 - Q_4$) are conducting. In this range, the V - I characteristic of the mixed translinear cell is nearly linear. However, for $|V_{YX}| \gg V_T$, one

transistor becomes nearly non-conducting (Q_2 or Q_4). Consequently, the V - I characteristic in this range is non-linear.

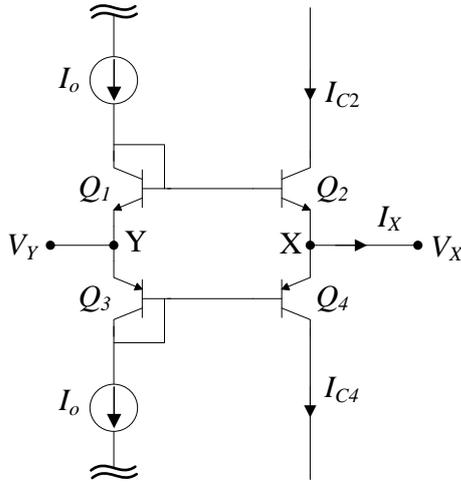


Fig. 1. Schematic of the mixed translinear cell [1].

From Fig. 1, by neglecting base currents, Early effect and parasitic capacitances of all transistors, the output current I_X which is composed of two exponential currents I_{C2} and I_{C4} can be expressed as

$$I_X = I_{C2} - I_{C4} = 2I_0 \sinh\left(\frac{V_{YX}}{V_T}\right) \quad (1)$$

where I_0 is the bias current, $V_T \approx 26$ mV is the thermal voltage at 27°C, and $V_{YX} = V_Y - V_X$ is differential input voltage.

The sinh function of (1) can be expressed using a Taylor series for a zero voltage input ($V_{YX} \approx 0$) as

$$I_X = 2I_0 \frac{V_{YX}}{V_T} + \frac{2I_0}{6} \left(\frac{V_{YX}}{V_T}\right)^3 + \frac{2I_0}{120} \left(\frac{V_{YX}}{V_T}\right)^5 + \dots \quad (2)$$

Equation (2) confirms that the input voltage swing should be limited to V_T for linear V - I characteristic. If this is not the case the higher order terms become non negligible. The ideal linear V - I characteristic can be obtained by considering the first terms of (2) only,

$$I_{X,L} = 2I_0 \frac{V_{YX}}{V_T} \quad (3)$$

where $I_{X,L}$ is defined as an ideal linear V - I characteristic of the output current I_X .

The V - I characteristic as noted in (1) and its linearized version in (3) are plotted in Fig. 3.

In this paper, we propose a novel approach to improve the linear input voltage range for the sinh mixed translinear cell. The schematic of the proposed circuit is shown in Fig. 2. The circuit contains four NPN transistors (Q_1 to Q_4) and four PNP transistors (Q_5 to Q_8). The constant current sources I_A and I_B provide the bias currents for the mixed translinear cell. In order to extend the linear operating range of the mixed translinear cell, we insert the common-emitter-connected pairs (Q_2 - Q_3 and Q_6 - Q_7) into the mixed

translinear cell. The main objective is to use the additional transistors to provide a biasing current for the transistors Q_4 and Q_8 , such that both of them remain conducting. By this mean, it is expected that the non-linear exponential currents between I_{C4} and I_{C8} are cancelled and the linearity of the current I_{XN} of the proposed mixed translinear will be improved. We will verify this expected result by a mathematical derivation and simulations. Note that we define the output current of the proposed circuit as I_{XN} in order to difference from the previous cell.

3. Proposed Mixed Translinear Cell

3.1 Theory

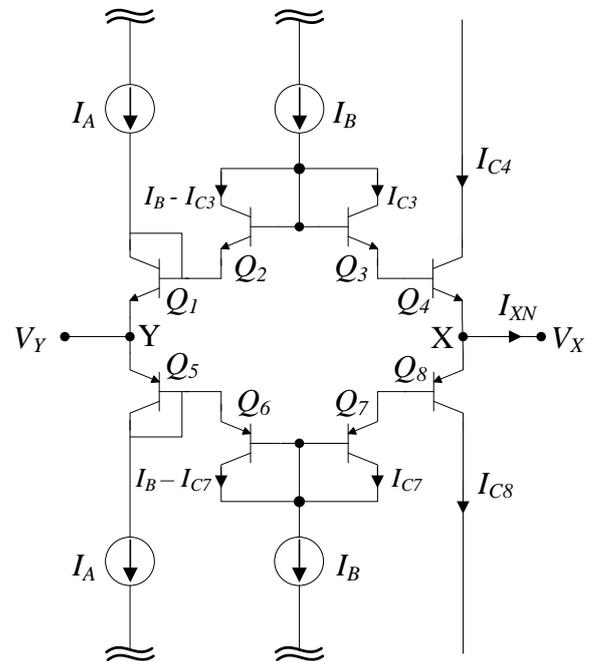


Fig. 2. Schematic of the proposed mixed translinear cell.

From Fig. 2, the voltage difference between nodes Y and X is given by the following sum

$$V_{YX} = V_{BE3} + V_{BE4} - V_{BE1} - V_{BE2}. \quad (4)$$

For simplification, we neglect the Early effect and the base currents (assuming sufficiently high current amplification β_N) for all the transistors. Also, we assume that the emitter areas of all NPN transistors (Q_1 to Q_4) are identical (resulting in an identical reverse saturation current I_S) and all the transistors are at the same temperature hence have the same thermal voltage V_T . With these assumptions, (4) can be expressed in function of the bias currents I_A and I_B and the (not yet known) current I_{C3} as

$$V_{YX} = V_T \ln\left(\frac{I_{C3}}{I_S}\right) + V_T \ln\left(\frac{\beta_N I_{C3}}{I_S}\right) - V_T \ln\left(\frac{I_A + I_B - I_{C3}}{I_S}\right) - V_T \ln\left(\frac{I_B - I_{C3}}{I_S}\right) \quad (5)$$

where β_N is the current gain of NPN transistor. Equation (5) can be expressed as

$$\frac{V_{YX}}{V_T} = \ln\left(\frac{(I_{C3})(\beta_N I_{C3})}{(I_A + I_B - I_{C3})(I_B - I_{C3})}\right) \quad (6)$$

and finally as a quadratic equation for the current I_{C3}

$$I_{C3}^2 (e^{V_{YX}/V_T} - \beta_N) - I_{C3}(I_A + 2I_B)e^{V_{YX}/V_T} + (I_B^2 + I_A I_B)e^{V_{YX}/V_T} = 0. \quad (7)$$

To solve (7) for the current I_{C3} , we limit the input voltage such that $-\ln(\beta_P)V_T \ll V_{YX} \ll \ln(\beta_N)V_T$. Given this condition, the quadratic coefficient $e^{V_{YX}/V_T} - \beta_N$ is non-zero. The positive collector current I_{C3} is hence given by

$$I_{C3} = \frac{K_1 - \sqrt{K_1^2 + 4K_2(\beta_N e^{-V_{YX}/V_T} - 1)}}{2(1 - \beta_N e^{-V_{YX}/V_T})} \quad (8)$$

where $K_1 = I_A + 2I_B$ and $K_2 = I_B^2 + I_A I_B$. Considering Fig. 2, it can be seen that $I_{C4} = \beta_N I_{C3}$. Noted that $\beta_N e^{-V_{YX}/V_T} \gg 1$ and considering (8), the current I_{C4} is given by

$$I_{C4} = \beta_N \left(\frac{K_1 - \sqrt{K_1^2 + 4K_2\beta_N e^{-V_{YX}/V_T}}}{-2\beta_N e^{-V_{YX}/V_T}} \right). \quad (9)$$

Equation (9) can be rewritten by using a Taylor series for $\sqrt{a+x}$ and becomes

$$I_{C4} = -\frac{K_1}{2} e^{V_{YX}/V_T} + \sqrt{K_2\beta_N} e^{\frac{1}{2}V_{YX}/V_T} + \frac{K_1^2}{8\sqrt{K_2\beta_N}} e^{\frac{3}{2}V_{YX}/V_T} - \frac{K_1^4}{128\sqrt{(K_2\beta_N)^3}} e^{\frac{5}{2}V_{YX}/V_T} + \dots \quad (10)$$

Likewise, the current I_{C8} is given by

$$I_{C8} = -\frac{K_1}{2} e^{-V_{YX}/V_T} + \sqrt{K_2\beta_P} e^{-\frac{1}{2}V_{YX}/V_T} + \frac{K_1^2}{8\sqrt{K_2\beta_P}} e^{-\frac{3}{2}V_{YX}/V_T} - \frac{K_1^4}{128\sqrt{(K_2\beta_P)^3}} e^{-\frac{5}{2}V_{YX}/V_T} + \dots \quad (11)$$

where β_P is the current gain of PNP transistor.

From Fig. 2, the current at the X terminal is given by the difference of the currents I_{C4} and I_{C8} ,

$$I_{XN} = I_{C4} - I_{C8}. \quad (12)$$

Assuming that $\beta_N = \beta_P = \beta$, substituting (10) and (11) into (12) and rewriting the exponentials as sinh, then the current I_{XN} becomes

$$I_{XN} = -\underbrace{K_1 \sinh\left(\frac{V_{YX}}{V_T}\right)}_{1st \text{ term}} + 2\sqrt{K_2\beta} \underbrace{\sinh\left(\frac{V_{YX}}{2V_T}\right)}_{2nd \text{ term}} + \underbrace{\frac{K_1^2}{4\sqrt{K_2\beta}} \sinh\left(\frac{3V_{YX}}{2V_T}\right)}_{3rd \text{ term}} - \dots \quad (13)$$

It is noted that for $|V_{YX}| < V_T \ln(\beta)$ the third and higher order terms in (13) are smaller than the first and the second one. Hence, in this case, (13) can be simplified to

$$I_{XN} \approx \underbrace{2\sqrt{K_2\beta} \sinh\left(\frac{V_{YX}}{2V_T}\right)}_{\text{positive sinh}} - \underbrace{K_1 \sinh\left(\frac{V_{YX}}{V_T}\right)}_{\text{negative sinh}}. \quad (14)$$

From (14), we see that the V - I characteristic of the proposed mixed translinear cell is composed of a positive term and a negative term of hyperbolic sine function, thus it is possible that the non-linear term will be reduced because of a summing of the positive term and negative term of hyperbolic sine function.

3.2 Optimal Parameters for Linear Operation

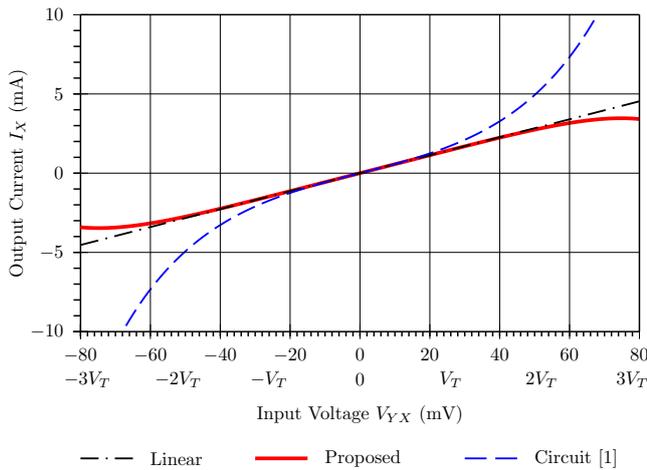
As shown in (1), the mixed translinear cell in Fig. 1 contains a single hyperbolic sine function so that the linear input voltage range is quite narrow. According to (14), we can see that the V - I characteristic of the proposed mixed translinear cell is formed by two hyperbolic sine functions composed of a positive term and a negative term. Because of the positive and the negative signs of the two terms in (14), it is possible to reduce the non-linearity which results from the third-order harmonics by adjusting the parameters K_1 and K_2 . In order to find the optimal parameters K_1 and K_2 to minimize the non-linearity coming from the third-order harmonics terms of output current I_{XN} , we expand the positive and the negative contributions of (14) with Taylor series and set the terms corresponding to the third-order harmonics as equal. When substituting K_1 and K_2 with the currents I_A and I_B , the optimal parameters for a linear operation are given by

$$\frac{\sqrt{(I_B^2 + I_A I_B)\beta}}{24} = \frac{(I_A + 2I_B)}{6}. \quad (15)$$

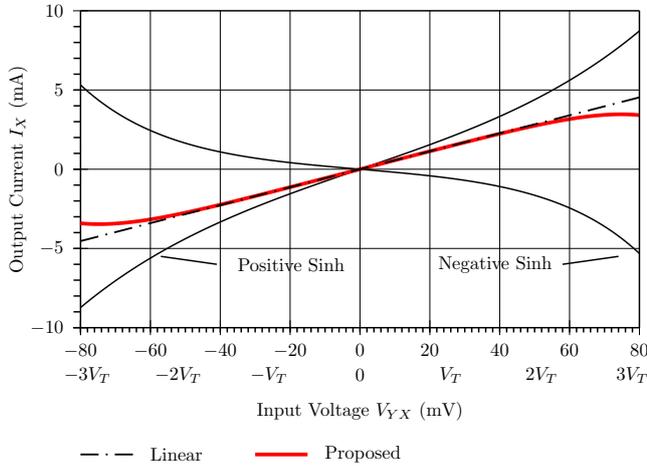
Equation (15) can be solved for a positive current I_A and becomes linear to the current I_B ,

$$I_A = I_B \frac{(\beta - 64) + \sqrt{\beta(\beta - 64)}}{32}. \quad (16)$$

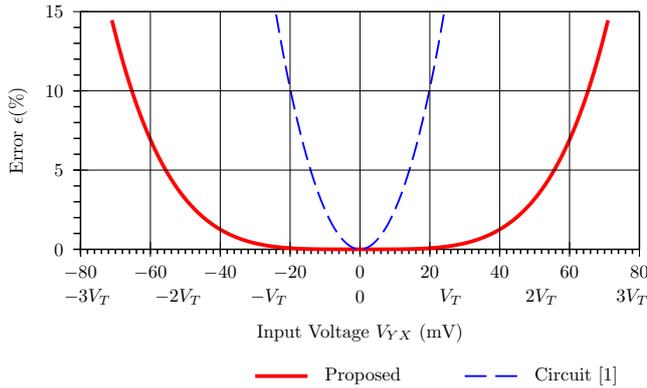
Equation (16) provides a simple mean to estimate the relation of the bias currents I_A and I_B which minimizes the third-order harmonic term of current I_{XN} when the β is given. For example, for $\beta = 100$, it is expected that the optimal linearity is obtained for $I_A = 3I_B$.



(a) The $V-I$ characteristic of the mixed translinear cell [1] and the proposed translinear cell compared to their ideal linear $V-I$ characteristic.



(b) Plot of the positive and negative sinh terms with the $V-I$ characteristic of the proposed translinear cell.



(c) The non-linearity error.

Fig. 3. Comparative plot of $V-I$ characteristics between the mixed translinear cell [1] and the proposed translinear cell, as well as their non-linearity errors.

We have shown the ideal linear $V-I$ characteristic of the mixed translinear cell (Fig. 1) in (3). Now, we calculate the ideal linear $V-I$ characteristic for the proposed translinear cell. Again expanding (14) with Taylor series for $|V_{YX}| \ll V_T$, the ideal linear $V-I$ characteristic of the proposed circuit can

be expressed as

$$I_{XNL} = \left[\sqrt{(I_B^2 + I_A I_B) \beta} - (I_A + 2I_B) \right] \frac{V_{YX}}{V_T} \quad (17)$$

where I_{XNL} is defined as the ideal linear $V-I$ characteristic of the output current I_{XN} .

This linear $V-I$ characteristic will be used for two reasons. First, it allows to select the bias currents for the mixed translinear cell in Fig. 1 and the proposed translinear cell such that the ideal linear $V-I$ characteristics are the same value. Second, the linear $V-I$ characteristic serves as a reference to estimate the non-linearity error (ϵ) as

$$\epsilon(\%) = \left| \frac{I_{XN} - I_{XNL}}{I_{XNL}} \right| 100. \quad (18)$$

To demonstrate the improvement of the linear range of the proposed translinear cell, the $V-I$ characteristics of the mixed translinear cell in Fig. 1 and the proposed translinear cells will be compared. To provide a numerical example, shown in Fig. 3, we select $\beta = 175$ and $I_B = 50 \mu A$, to maximize the linear input range according to (16), resulting in $I_A = 390 \mu A$ ($I_A = 7.8I_B$). To compare with the mixed translinear cell in Fig. 1, its bias current I_0 is set such that the ideal linearized $V-I$ characteristic is the same value. Comparing (17) and (3), it is noted that this happens when $2I_0 = \sqrt{(I_B^2 + I_A I_B) \beta} - (I_A + 2I_B)$. For the numerical example, this results in $I_0 = 736 \mu A$. In Fig. 3a, the ideal linear $V-I$ characteristics (3) and (17) are shown together with the non-linear ones as given in (1) and (14). For clarity, the positive sinh and negative sinh (14) are plotted individually in Fig. 3b. It can be seen that the linear input range of the proposed translinear cell is improved significantly compared to the mixed translinear cell in Fig. 1. This is confirmed by the non-linearity error as defined in (18) which is shown in Fig. 3c. As expected, the error for the proposed translinear cell is smaller than the mixed translinear cell in Fig. 1. For example, at $V_{YX} = 20$ mV, the error of the mixed translinear cell in Fig. 1 is about 10 % while the proposed translinear cell smaller than 0.1 %.

4. Simulation Results

To verify the validity of the theoretical derivations for the circuit operation, the mixed translinear cell in Fig. 1 and the proposed translinear cell in Fig. 2 are simulated by PSPICE. Therefore, the general purpose bipolar transistors 2N3904 (NPN) and 2N3906 (PNP) are used with a symmetric supply voltage of $V_{CC} = -V_{EE} = 2$ V. In the PSPICE simulation, the current gain (β) of transistor is approximately 175. As shown in (16), the best linearity is expected for the bias currents with a relation of $I_A = 7.8I_B$ ($\beta = 175$). For simulation, we select the current $I_B = 50 \mu A$ thus $I_A = 390 \mu A$.

To have a fair comparison between the two translinear cells, the bias currents of both circuits are set such that the

ideal linearized is the same value, the same transconductance (G_M), results in (3) and (17). As shown in Section 3.2, this results in a bias current $I_0 = 736 \mu\text{A}$. It is noted that the bias currents for the PSPICE values are identical to the ones selected during the theoretical estimations.

and the proposed mixed translinear cell uses approximately 6 mW and 8.6 mW, respectively. As expected, the power consumption of the proposed cell has increased slightly.

Fig. 4a shows a comparison of the large signal $V-I$ characteristics of the mixed translinear cell in Fig. 1 and the proposed cell for V_{YX} between -0.3 V and 0.3 V and node X connected to ground. Again, it is noted that the deviation of the $V-I$ characteristic from the ideal linear $V-I$ characteristic is smaller for the proposed circuit than the mixed translinear cell in Fig. 1.

Fig. 4b illustrates again that the linear input range of the proposed mixed translinear cell is increased compared to the mixed translinear cell in Fig. 1. It is noted that the offset voltage of the mixed translinear cell in Fig. 1 is approximately $700 \mu\text{V}$ while the proposed circuit has approximately 5 mV , because the proposed circuit is affected by the difference of the current gains (β) between the PNP and NPN transistors. To minimize the offset voltage, matched transistor pairs may be used. If it is not practical to match the β of the transistors, the offset can also be adjusted by setting a different bias current I_A and I_B for the PNP transistors and for the NPN transistors. In the example shown in Fig. 4c, the bias current I_B for the transistors Q_2 and Q_3 are $59 \mu\text{A}$ and the bias current I_A of transistor Q_1 is $460 \mu\text{A}$. The bias currents for Q_5 to Q_7 have not been changed and are still $I_B = 50 \mu\text{A}$ and $I_A = 390 \mu\text{A}$. It is noted that, the ratio between I_A and I_B is given by $I_A = 7.8 I_B$ to minimize the non-linearity. From the simulation result, the offset voltage of the proposed circuit is approximately $100 \mu\text{V}$ when adjusted the bias current I_A and I_B for the transistors $Q_1 - Q_3$.

Furthermore, Fig. 5 shows the tuning ability of the transconductance of the mixed translinear cell in Fig. 1 and the proposed mixed translinear cell when varying the bias currents. To compare the two architectures, the bias currents are selected such that G_M are approximately the same value for a zero input voltage. In the simulations, this has been achieved by varying the bias current I_0 from $294 \mu\text{A}$ to 2.35 mA with $294 \mu\text{A}$ steps for the mixed translinear cell in Fig. 1 and the bias current I_B from $20 \mu\text{A}$ to $160 \mu\text{A}$ with $20 \mu\text{A}$ steps for the proposed translinear cell. Note that the bias current I_A is always set to $7.8 I_B$.

Fig. 5a shows the characteristic of the simulated transconductances (G_M) of the mixed translinear cell in Fig. 1 and the proposed mixed translinear cell when varying their bias currents I_0 , I_A and I_B . For the proposed translinear cell, the transconductance G_M is nearly independent of the input voltage V_{YX} over a large range.

Fig. 5b shows the transconductance G_M of the proposed mixed translinear cell and the mixed translinear cell in Fig. 1. It is noted that the G_M of the proposed mixed translinear cell is closer to a constant value than the mixed translinear cell in Fig. 1. Again, this confirms the improved linearity of the proposed translinear cell when compared to the mixed translinear cell in Fig. 1.

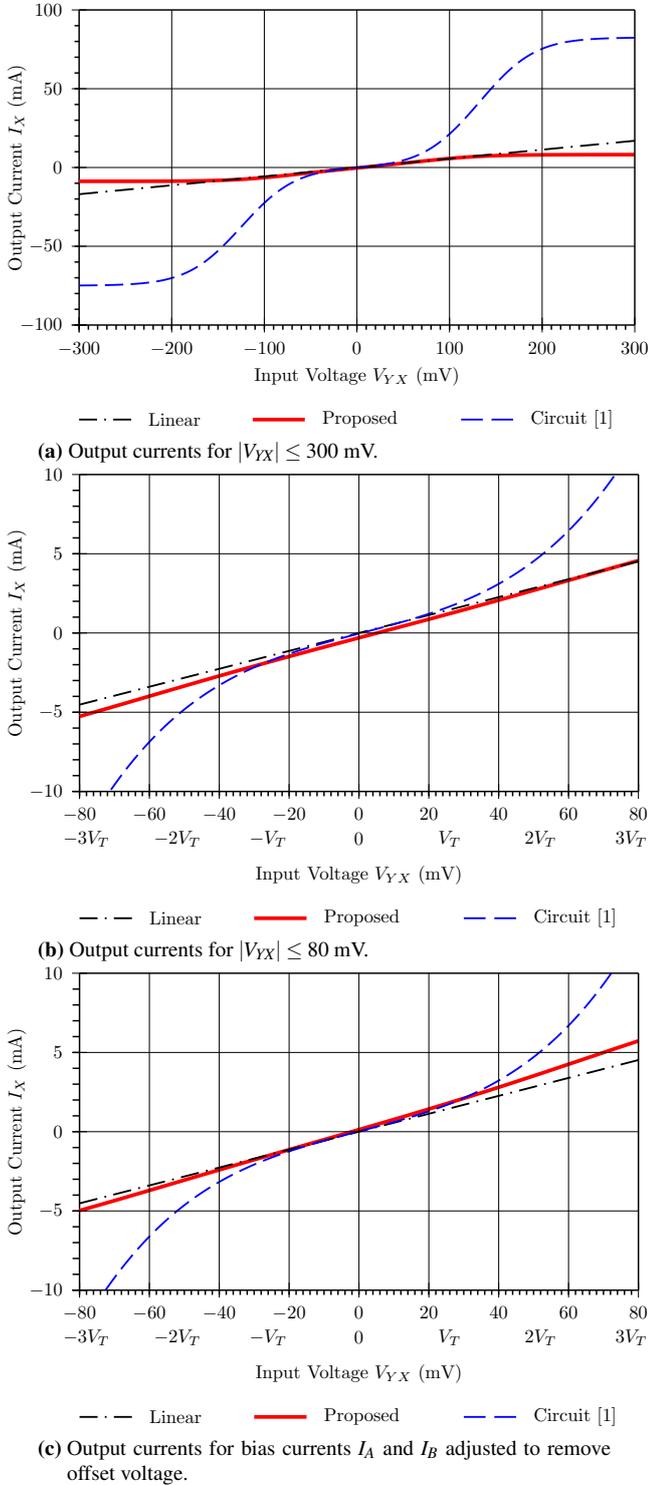
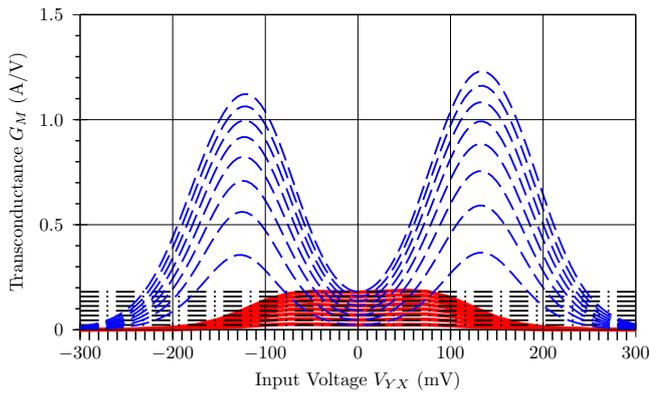
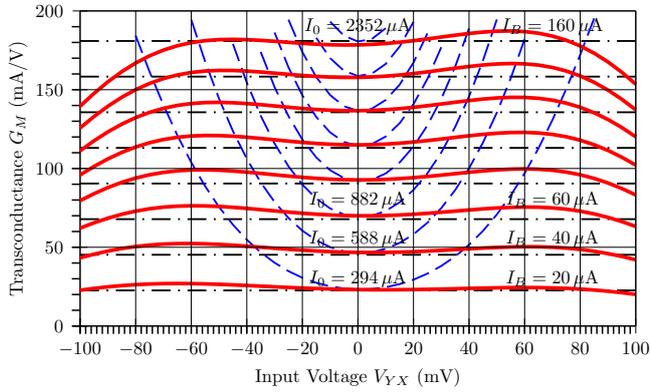


Fig. 4. Comparison $V-I$ characteristic of the mixed translinear cell [1] and proposed mixed translinear cell.

As a first simulation, the power consumption at a quiescent point is estimated. The mixed translinear cell in Fig. 1



(a) Transconductance characteristics for $|V_{YX}| \leq 0.3$ V.



(b) Transconductance characteristics for $|V_{YX}| \leq 0.1$ V.

Fig. 5. Tuning behavior of G_M comparison between the mixed translinear cell [1] and proposed mixed translinear cell. The G_M is shown for different bias currents I_A and I_B .

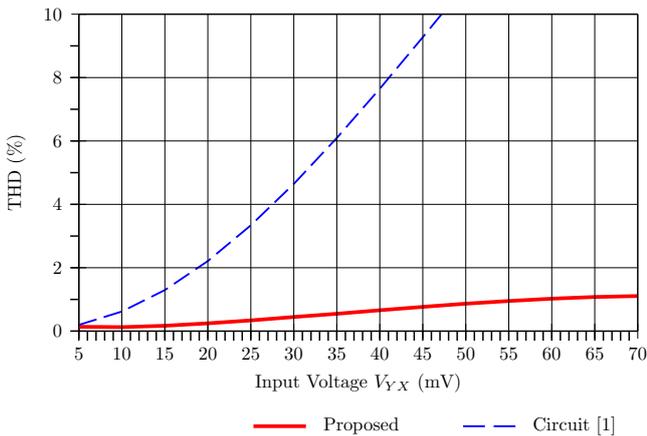


Fig. 6. Total harmonic distortion as a function of the input amplitude of a 100 kHz sinusoidal signal, for the mixed translinear cell [1] and the proposed mixed translinear cell.

To validate the linearity performance of the proposed circuit, total harmonic distortion (THD) of the proposed mixed translinear cell is also simulated. The bias current of the mixed translinear cell in Fig. 1 is set to $I_0 = 736 \mu\text{A}$ and the bias currents I_B and I_A of the proposed cell to $50 \mu\text{A}$ and

$390 \mu\text{A}$, respectively. Again, this results in the same value G_M at zero input voltage. The THD is calculated for a sinusoidal signal at V_{YX} at 100 kHz with varying amplitude. The simulation result is displayed in Fig. 6. It is noted that the maximum amplitude of V_{YX} for the THD below 1% is approximately 60 mV for the proposed mixed translinear cell and lower than 15 mV for the mixed translinear cell in Fig. 1.

Comparative results of the simulated performances between the proposed circuit and the mixed translinear cell in Fig. 1 are shown in Tab. 1. It can be seen that the linear input range is increased more than by a factor 4 with a moderate increase of the power consumption (factor 1.4).

	Circuit [1]	Proposed
Input operating swing ($\epsilon(\%) = 1\%$)	≈ 7 mV	≈ 40 mV
THD $\leq 1\%$	15 mV	60 mV
Power consumption	6 mW	8.6 mW

Tab. 1. Comparison of the performances for the mixed translinear cell [1] and the proposed mixed translinear cell with approximately the same G_M .

5. Selected Applications

5.1 Floating Resistor

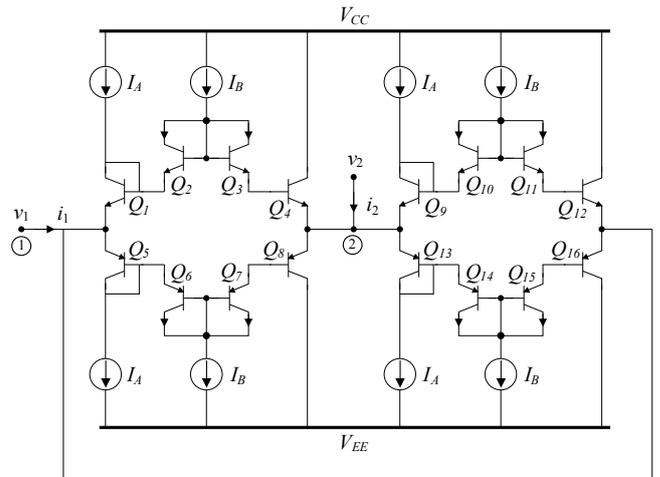


Fig. 7. Floating resistance circuit.

To demonstrate an application that benefits from the increased linear input range of the proposed mixed translinear cell, a floating resistor as proposed in [6] is realized by using the proposed mixed translinear cell. The circuit is shown in Fig. 7. It consists of two of the proposed mixed translinear cells by a parallel-back-to-back connection. Assuming that all transistors are matched and the current gains (β) of all transistors are greater than unit, then relations of the current and voltage of the floating resistor can be found as

$$i_1 = -i_2 = 2\sqrt{K_2\beta} \sinh\left(\frac{v_1 - v_2}{2V_T}\right) - K_1 \sinh\left(\frac{v_1 - v_2}{V_T}\right). \quad (19)$$

The equivalent resistance between port 1 and 2, when $|v_{12}| \ll V_T$, is the inverse of the transconductance G_M cal-

culated in (17) and is given by

$$R_{12} = \frac{V_T}{\sqrt{(I_B^2 + I_A I_B)\beta} - (I_A + 2I_B)} \tag{20}$$

The above equation shows that the floating resistance can be tuned by adjusting the bias current I_A or I_B . However, in order to reduce the third order harmonics distortion, the relation between the current I_A and I_B have to set accordingly to (16). When port 2 is connected to ground, the circuit becomes a grounded resistance. In this case, the transistors Q_9 to Q_{16} can be removed while the relation between the current and voltage of the resistor remains as written in (20). For the floating resistance realized by the mixed translinear cell in Fig. 1 as proposed in [6], the value of resistance between port 1 and port 2 is $R_{12} = V_T/2I_0$ [6] and it can be adjusted by the bias current I_0 . To show the increased linear input range of the floating resistance when use the proposed mixed translinear cell. The floating resistance in Fig. 7 realized by the proposed translinear cell has been simulated in PSPICE and compared with the floating resistance realized by the mixed translinear cell in Fig. 1.

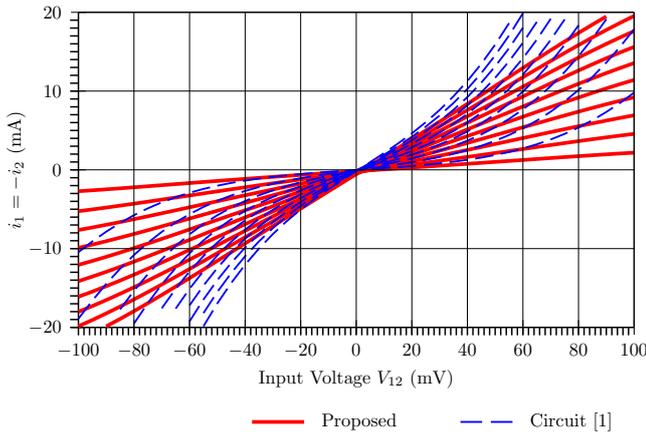


Fig. 8. Comparison of the DC transfer characteristics of the floating resistor realized by the mixed translinear cell [1] and the proposed translinear cells.

For simulation, we use the general purpose bipolar transistors 2N3904 (NPN) and 2N3906 (PNP) with a supply voltage of $V_{CC} = -V_{EE} = 2\text{ V}$. Because the current gain (β) of the transistors in PSPICE is approximately 175, the relation between the bias currents I_A and I_B of the proposed translinear cell is set to $I_A = 7.8I_B$. For comparison, the bias currents of both circuits are set for the same value of resistance as (20). Fig. 8 shows a simulated comparison of V - I characteristics of the floating resistance using the proposed mixed translinear cell and the mixed translinear cell in Fig. 1, when the bias current I_0 was varied from $294\ \mu\text{A}$ to $2.94\ \text{mA}$ with $294\ \mu\text{A}$ step size while the bias currents I_B was varied from $20\ \mu\text{A}$ to $200\ \mu\text{A}$ with $20\ \mu\text{A}$ step size. The bias current I_A always set to $7.8I_B$. It can be seen that the relation between the currents $i_1 = -i_2$ and the input voltage v_{12} of the floating resistance using the proposed translinear cell is very close to linear – the same V - I characteristic as for an ideal resistor that follows Ohms law than the floating resistance realized by the

mixed translinear cell in Fig. 1. Furthermore, the slope of the V - I characteristic can be adjusted using the bias currents I_A and I_B . Hence, the simulation results as shown in Fig. 8 confirm that the circuit presented in Fig. 7 provides a floating electronically controllable resistor and the linear range is approximately 100 mV. Fig. 9 shows a value of the floating resistance as a function of their bias currents for both circuits. From the simulation results, it can be seen that the value of the resistance realized by the mixed translinear cell in Fig. 1 and the proposed resistance are nearly the same and both are in good agreement with the theoretical results in (20) calculated for $\beta = 175$.

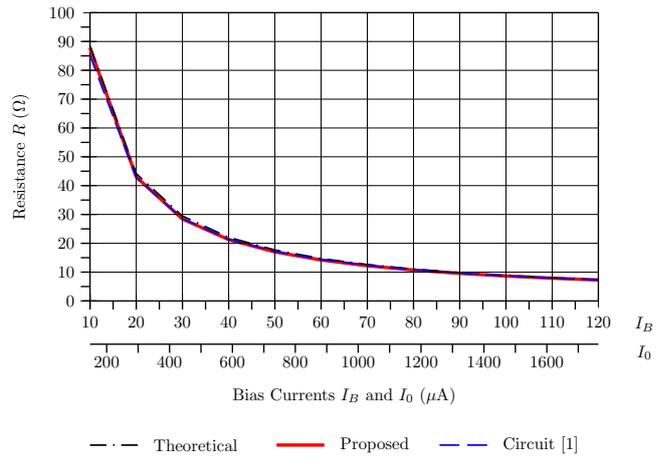


Fig. 9. Magnitude of floating resistance as a function of I_B and I_0 .

5.2 Instrumentation Amplifier

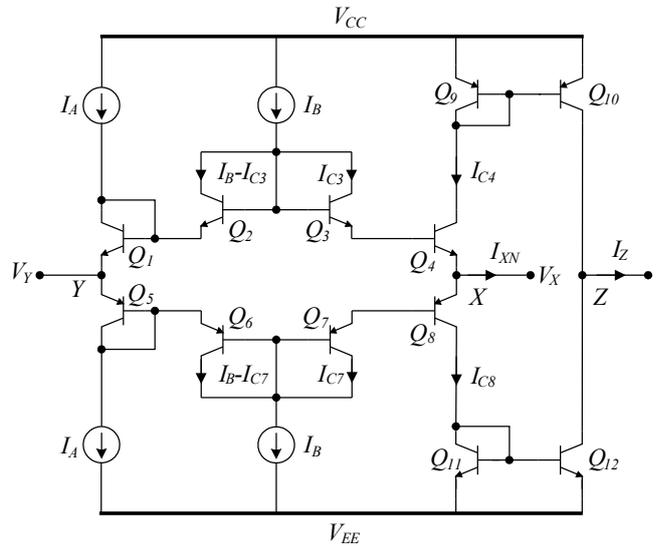


Fig. 10. Schematic of a CCCII using the proposed mixed translinear cell as an input front end.

As mentioned above, the mixed translinear cell can be used as an input front end for the second-generation current controlled conveyor (CCCII). Thus, to implement the CCCII by using the proposed mixed translinear cell can be easily done by adding two complementary current mirrors

to duplicate the current from port X to port Z as shown in Fig. 10. The relationship between the output current I_Z and input voltage V_{YX} of the proposed CCCII in Fig. 10 is given by (14) and for the CCCII based on the mixed translinear cell in Fig. 1 has the V - I characteristic as shown in (1).

We will show the increased linearity at the example of an instrumentation amplifier as proposed in [10]. The instrument amplifier consists of two CCCIIs connected as shown in Fig. 11.

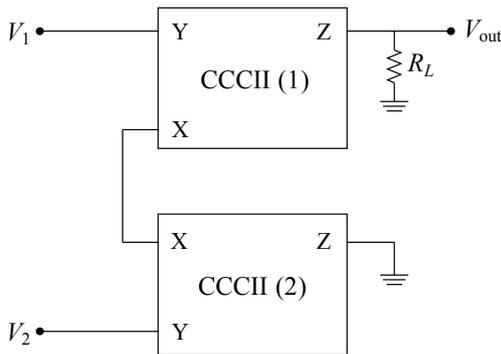


Fig. 11. Instrumentation amplifier proposed in [10].

The output voltage of the instrumentation amplifier in Fig. 11 is related to the parasitic resistance (R_X) at the port X of the CCCII and the input voltages V_1 and V_2 by [10]

$$\frac{V_{out}}{V_1 - V_2} = \frac{R_L}{2R_X}. \quad (21)$$

Therefore, the output voltage gain can be adjusted by R_X of the mixed translinear cell. For the CCCII implemented by the mixed translinear cell in Fig. 1, the parasitic resistance R_X is adjusted by the bias current I_0 as $R_X \approx V_T/2I_0$ when $V_{YX} \ll V_T$ [2]. This means that the gain of the instrumentation amplifier is controlled by the current I_0 . However, when the input voltage comes close (or exceeds) the thermal voltage, the parasitic resistance cannot be considered as linear anymore. Thus, the linear input range of the instrumentation amplifier is also limited. For increasing the input linear range of the instrumentation amplifier, the proposed CCCII as shown in Fig. 10 will be used to realize the instrumentation amplifier.

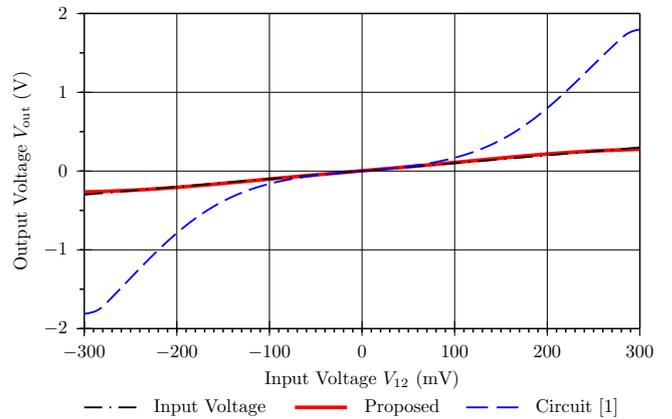
The parasitic resistance at port X of the proposed CCCII in Fig. 10 is defined as (R_{XN}) and the value of the resistance is the inverse of the transconductance G_M which has been calculated in (17). Hence, the R_{XN} of the proposed CCCII in Fig. 10 is given as

$$R_{XN} = \frac{V_T}{\sqrt{(I_B^2 + I_A I_B)\beta} - (I_A + 2I_B)} \quad (22)$$

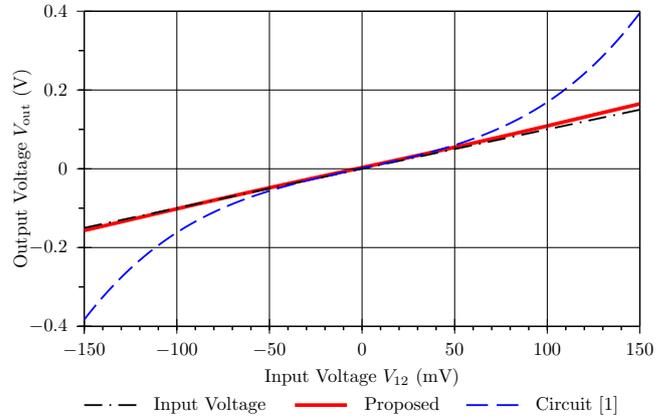
where R_{XN} is the parasitic resistance at port X of the proposed CCCII in Fig. 10.

From (22), it can be seen that the value of R_{XN} can be adjusted by the bias currents I_A or I_B . It should be noted that, for suppression the third-order harmonic term, the relation

between the bias current I_A and I_B should be set according to (16).



(a) Output voltages for $|V_{12}| \leq 0.3$ V.



(b) Output voltages for $|V_{12}| \leq 0.15$ V.

Fig. 12. Comparison of the V - I characteristics of the instrumentation amplifier realized from the mixed translinear cell [1] and the proposed mixed translinear cell at unity gain.

To demonstrate the improvement of the linear input range, the instrumentation amplifier realized by the proposed CCCII is simulated in PSPICE and the results are compared to the instrumentation amplifier realized by the CCCII based on the mixed translinear cell in Fig. 1. For simplification of comparison, the gain of the instrumentation amplifier is set to unity. The resistive load was set to 50Ω and the supply voltage is $V_{CC} = -V_{EE} = 2$ V. Again, the bias currents are set to $I_A = 7.8I_B$ to minimize the third order harmonics for $\beta = 175$. To obtain the unity gain, the $R_{XN} \approx 25 \Omega$, then the current I_A and I_B are set to $273 \mu A$ and $35 \mu A$, respectively. For the CCCII based on the mixed translinear cell in Fig. 1, the bias current $I_0 = 514.5 \mu A$ for $R_X \approx 25 \Omega$ also.

Fig. 12a shows a comparison of a large signal V - I characteristic of the instrumentation amplifier as demonstrated in Fig. 11 when implementing with the CCCII based on the mixed translinear cell in Fig. 1 and the proposed CCCII in Fig. 10. The input differential voltage ($V_{12} = V_1 - V_2$) was swept continuously from -0.3 V to 0.3 V. From Fig. 12b, it is obvious that the linear input range (V_{12}) of the instrumentation amplifier employing the proposed CCCII is wider than using the CCCII based on the mixed translinear cell in Fig. 1.

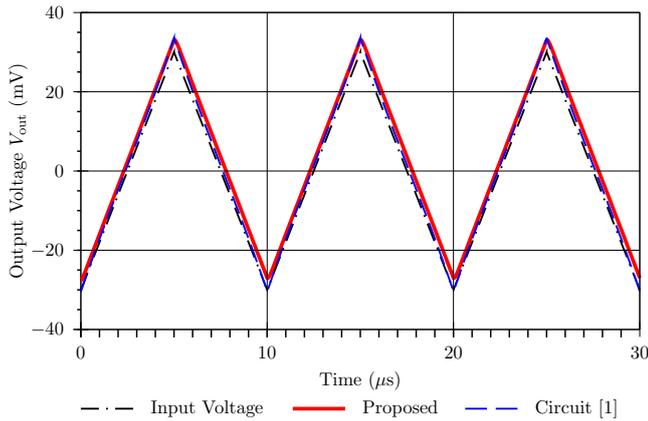
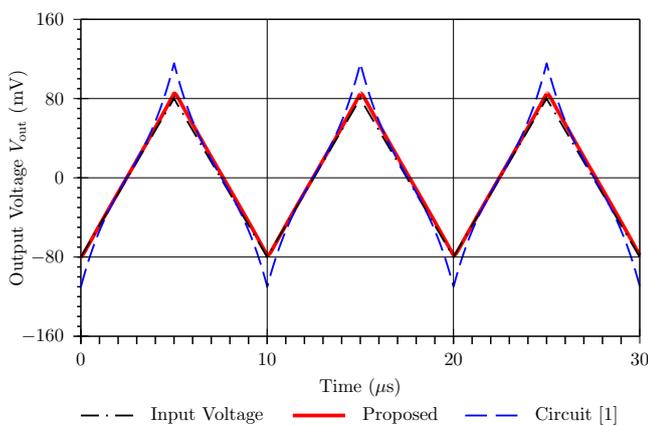
(a) Amplitude of $V_{12} = 30$ mV.(b) Amplitude of $V_{12} = 80$ mV.**Fig. 13.** Comparison of the transient response of the instrumentation amplifier at unity gain.

Fig. 13 shows a time domain representation of the output voltage (V_{out}) of the instrumentation amplifier in Fig. 11 when a triangle signal at a frequency of 100 kHz is applied. The input amplitudes are $V_{12} = 30$ mV for Fig. 13a and 80 mV for Fig. 13b. It can be seen that for a small input voltage (V_{12}), the output voltage of both instrumentation amplifier can follow the input voltage as shown in Fig. 13a. However, for a large input voltage, the output voltage of the instrumentation amplifier using the proposed CCCII follows the input voltage while the instrumentation amplifier using the CCCII based on the mixed translinear cell in Fig. 1 deviates from the input voltage as shown in Fig. 13b. In this representation, the reduced distortion of V_{out} of the instrumentation amplifier can be seen best at the shape of the edges of the triangular signal.

6. Summary

A new compact architecture for improving the linear input voltage range of the sinh mixed translinear cell has

been presented. The proposed circuit adds common-anode-connected pairs into the sinh mixed translinear cell to provide the bias current to the transistors such that they remain conducting, thus extending its linear operation range. Explicit equations are given and used to minimize the third-order harmonic term. The proposed circuit is suitable for implementation in integrated circuits, since it does not require external resistors or other passive components. Simulation outcomes, which are in excellent agreement with the theoretical results, confirm that the linearity of the proposed cell is improved compared to the mixed translinear cell in Fig. 1.

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