Third-order Intermodulation Reduction in Mobile Power Amplifiers by the First Stage Bias Control

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Abstract. *In this paper, the third order intermodulation distortion (IMD3) of three-stage power amplifier (PA) is analyzed using the Volterra series. The analysis explains how the total IMD3 of the three-stage power amplifier can be reduced by the first-stage bias condition. The three-stage PA, which is fabricated using InGaP/GaAs hetero-junction bipolar transistor (HBT), operates with an optimized first driver stage bias for higher P1dB and good gain flatness. The power amplifier has been designed for 1626.5 MHz~1660.5 MHz satellite mobile communications. With π/4 DQPSK modulation signals, this PA can deliver a highly linear output power of 33 dBm from 3.6V supply voltage. At 33 dBm output power, it shows a gain of 31.9 dB, a power-added efficiency (PAE) of 39.8%, an adjacent channel power ratio (ACPR) of -28.2 dBc at a 31.25 kHz offset frequency.*

Keywords

Satellite mobile phone, first driver stage bias, three-stage power amplifier (PA), high 1 dB gain compression point, IMD reduction.

1. Introduction

In mobile satellite communication systems, the power amplifier (PA) is a key component for providing high efficiency and good linearity as it dissipates most DC power in the transmitter and transmits the modulation signals with accepted linearity specifications. The PA in satellite mobile systems must be optimized to deliver a high linear output power for very wide coverage area, with only a few earth stations. Currently, semiconductor technologies for mobile power amplifier designs include silicon, silicon germanium (SiGe), gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), and so on. The GaAs heterojunction bipolar transistor (HBT) is a leading technology in the present PA markets, due to its high cutoff frequency, low phase-noise, high linearity and efficiency, and high power density. As such, it is currently the best candidate for satellite mobile phone PAs because of its high power density, high linearity, and single supply voltage operation.

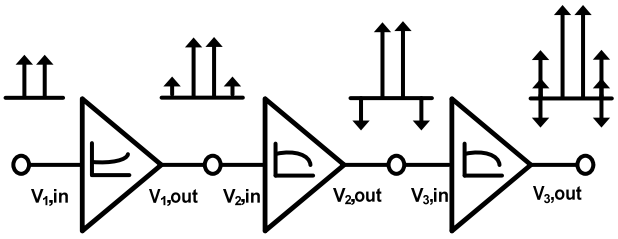


Fig. 1. Simplified block diagram of the three-stage power amplifier with the concept of IMD cancellation.

As the market requires ever-smaller module sizes and lower costs, the integration of a power amplifier with matching components in a single package is very important for the commercial implementation of RF modules. On the other hand, PA linearity is usually evaluated by the level of the 3rd order intermodulation distortion (IMD3) or the ratio of adjacent channel power (ACPR). It has been previously reported that the 3rd order IMD level of active devices is strongly affected by a bias condition, and that the IMD sweet spots can be shifted by the bias variation [1]. However, it has analyzed the optimum bias point of only one-stage PA to have the minimum IMD3. Also, there are some papers that have analyzed the IMD3 cancellation mechanism for the two-stage PA using a Volterra series expansion for each stage [2], [3]. In [2], they have analyzed IMD3 cancellation technique using optimization of each stage's bias resistors. In [3], anti-phase IMD generation technique using amplitude compressor has been used for IMD3 cancellation.

In this paper, we applied the well-known Volterra series expansion to our three-stage PA. Then, we verified that the IMD3 of three-stage PA is strongly affected by the first-stage bias and gain deviation of each stage. Fig. 1 shows a block diagram of the three-stage amplifier which explains the IMD cancellation concept. In the next section, the magnitude and phase of IM3 components generated from each stage will be obtained, and it will be shown that the vector summation of the IM3 components causes the overall IMD3 reduction. The IM3 voltages are simulated to figure out the reason why the IMD3 performance is im-

proved on the first-stage bias current rise. The designed PA has an optimized bias condition of the first driver stage for a high 1 dB gain compression point and good linearity at various output power. The IMD3 and AM/PM characteristics of the PA under variation of the first driver stage bias point were measured using spectrum and vector network analyzers.

2. Principles of IMD3 Reduction

2.1 IMD3 Analysis for the Three-stage Amplifier

The nonlinear transfer characteristics of PA are analyzed by the Volterra series expansion. The input voltage/output voltage transfer characteristics of the each stage expressed as [2]

$$V_{1,out}(t) = a_1 \cdot V_{1,in}(t) + a_2 \cdot V_{1,in}^2(t) + a_3 \cdot V_{1,in}^3(t) + \cdots, \quad (1)$$

$$V_{2,out}(t) = b_1 \cdot V_{2,in}(t) + b_2 \cdot V_{2,in}^2(t) + b_3 \cdot V_{2,in}^3(t) + \cdots, \quad (2)$$

$$V_{3,out}(t) = c_1 \cdot V_{3,in}(t) + c_2 \cdot V_{3,in}^2(t) + c_3 \cdot V_{3,in}^3(t) + \cdots \quad (3)$$

where $V_{n,\mathrm{out}}(t)$ and $V_{n,\mathrm{in}}(t)$ are the output and input voltages for the n-th stage, and a_i, b_i and c_i are the Volterra coefficients, including phase. To study the IMD behavior of three stages PAs, the two tone signals are applied to the input of the first-stage. The input signals will be

$$V_{1,in}(t) = A \cdot (\cos\omega_1 t + \cos\omega_2 t) \quad (4)$$

where A is a magnitude of the applied input voltage.

With the two-tone input signal, the fundamental and third-order intermodulation (IM3) signals of each stage can be derived. Substitution of (4) into (1) gives the fundamental and the IM3 signals at the first-stage output as follows:

$$V_{1,out}\big|_{\omega_1} \approx A a_1 \cdot \cos(\omega_1)t, \quad (5)$$

$$V_{1,out}\big|_{2\omega_1-\omega_2} \approx \frac{3}{4} A^3 a_3 \cdot \cos(2\omega_1 - \omega_2)t. \quad (6)$$

And the output signals of second-stage are

$$V_{2,out}\big|_{\omega_1} \approx A a_1 b_1 \cdot \cos(\omega_1)t, \quad (7)$$

$$V_{2,out}\big|_{2\omega_1-\omega_2} \approx \left(\frac{3}{4} A^3 a_3 b_1 + \frac{3}{4} A^3 a_1^3 b_3\right) \cdot \cos(2\omega_1 - \omega_2)t. \quad (8)$$

The final fundamental and IM3 output voltage at final third-stage are given by

$$V_{3,out}\big|_{\omega_1} \approx A a_1 b_1 c_1 \cdot \cos(\omega_1)t, \quad (9)$$

$$V_{3,out}\big|_{2\omega_1-\omega_2} \approx \left(\frac{3}{4} A^3 a_3 b_1 c_1 + \frac{3}{4} A^3 a_1^3 b_3 c_1 + \frac{3}{4} A^3 a_1^3 b_1^3 c_3\right) \cdot \cos(2\omega_1 - \omega_2)t$$
$$\approx \frac{3}{4} A^3 a_1 b_1 c_1 \cdot \left(\frac{a_3}{a_1} + \frac{a_1^2 b_3}{b_1} + \frac{a_1^2 b_1^2 c_3}{c_1}\right) \cdot \cos(2\omega_1 - \omega_2)t. \quad (10)$$

where the high-degree terms are ignored because they are relatively small. The IM3 voltage of final-stage is represented by the summation of three terms performed vectorially. From (10), the first term is the IM3 component generated by the first-stage and the second term is formed by the second-stage utilizing the fundamental output signal from the first-stage. Similarly, the third term is formed by the third-stage using the fundamental output generated from the second-stage.

We can see that the three terms represent the gain deviation of each stage from (10). If the gain expansion occurs, the signs for a_3/a_1, b_3/b_1, and b_3/b_1 should be positive. However, when the gain compression occurs, these should be negative [3]. Here, the first-stage will have gain expansion, while the second and the third stage will be compressed as seen in Fig. 1. So, the gain deviation of each stage and Volterra coefficients, a_1 and b_1 affect the magnitude and phase of three terms of IM3 voltage as in (10).

2.2 Effect of First-stage Bias on the IM3 Voltage

From (10), the three terms of IM3 voltage are related with a_1, which is the gain of first-stage depending on bias condition. Therefore, the IM3 voltage at the final stage output is strongly affected from bias condition of the first-stage. To verify the effect of the first-stage bias, a two-tone simulation has been conducted at an output power of 30 dBm for various first-stage bias current. As the bias point of the first-stage increases, $a_1$is also increased, then the first term of (10) is reduced and the second and the third term are increased, as shown in Fig. 2. The three terms in (10) are vectors, which have phase information.

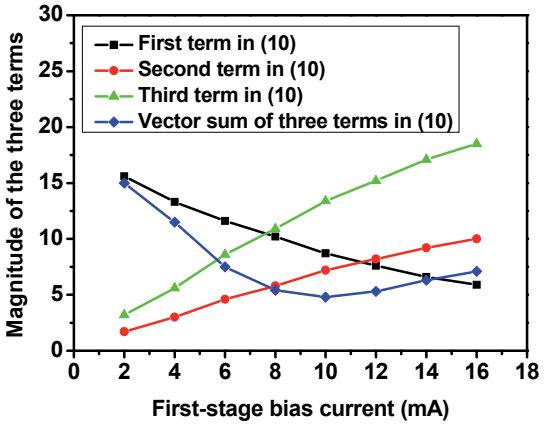


Fig. 2. Simulated magnitude of three terms in (10), which presents the overall IM3 voltage of three-stage PA.

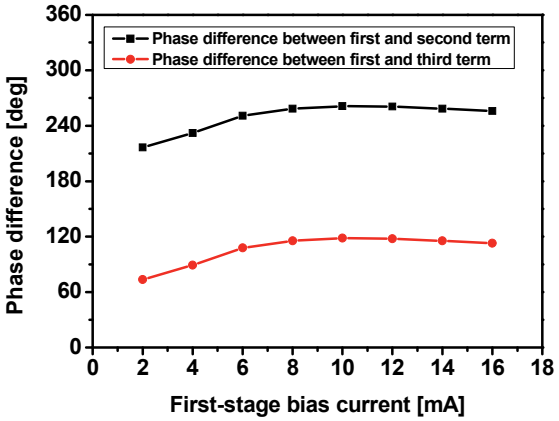


Fig. 3. Simulated phase difference between the first, the second and the third term in (10).

Fig. 3 shows the phase difference of the three terms. The phase difference between the first term and the second term in (10) is about 250°. The phase difference between the first term and the third term in (10) is about 110°. The vector summed the first and the third term in (10) has opposite phase with the second term in (10). The second term in (10), which has opposite phase, is increased depending on the first-stage bias rises. As a result, the summation of vectors in (10) is reduced, thus the overall IMD3 of the three-stage PA is also decreased as shown in Fig. 6.

3. Circuit Implementations

Fig. 4 shows a simplified schematic of the three-stage InGaP/GaAs HBT power amplifier. For gain expansion of the first-stage, the load impedance of the first-stage was set to be $19 + j\,29\ \Omega$, and a deep class-AB bias level was chosen. To find optimum bias point of the first-stage, with a fixed Rb1, the R_{REF} was optimized to be 1.2 kΩ for Icq1 of 8.2mA at Vcbias = 3.6 V and Vreg = 2.8 V. Each stage's bias circuits have a current mirror topology with a linearization capacitor (C_b) being used to maintain a constant base-emitter bias voltage.

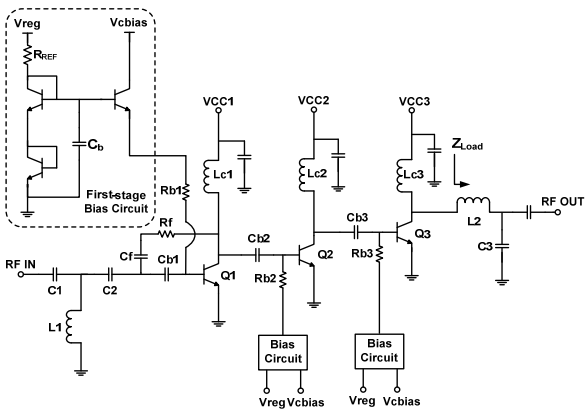


Fig. 4. Schematic circuit diagram of the three-stage HBT power amplifier.

All the input, inter-stage, output matching components and bias circuits for each stage are integrated on chip. From the figure, the capacitors (Cb1, Cb2, and Cb3) and the resistors (Rb1, Rb2, and Rb3) represent the sum of the unit-cell components of each stage. The unit-cell includes base ballasting resistor and inter-stage matching capacitor. Here, base ballasting resistor is used to prevent current collapse and to suppress circuit instability. The capacitor also serves as DC block component. C1, C2, and a spiral inductor L1 are used for input matching. Cf and Rf form the RC feedback circuit in the driver stage for stability. For the inter-stage matching, Lc1, Cb2, Lc2, and Cb3 form the high pass structure. Specifically, the inter-stage matching between the second and final stages requires a small shunt inductor value because the input capacitance of the final power stage is very large. So, short bond wire inductors are used for Lc2. The other components, L2, C3 are used for output matching, their values were chosen for realizing small load impedance. The output matching has a one-section low-pass topology to attain high output P1dB. The measured insertion loss of the output matching circuit was 0.5 dB. Inductors Lc1, Lc2, and L2 are realized using bond wires in a single package.

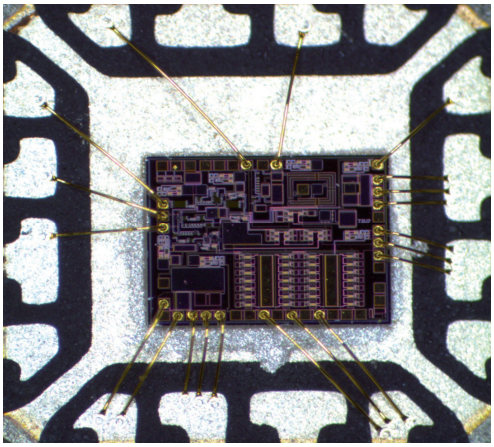


Fig. 5. Photograph of the fabricated power amplifier on a QFN package (chip size: 1.7 mm x 1.4 mm).

Fig. 5 shows a chip photograph of the three-stage power amplifier which has a size of 1.7 mm x 1.4 mm. It is integrated on a 4 mm x 4 mm QFN package using bond wires. The emitter sizes are 480 μm^2, 1,280 μm^2, and 10,080 μm^2 for the first, second, and final stages, respectively. To obtain a highly linear output power level from a 3.6V supply, the load impedance of the PA was set to be 2.6 Ω. The PA could achieve a highly linear output power of 33 dBm with only one-section output matching network over a frequency range from 1626.5 MHz to 1660.5 MHz.

4. Measurement Results

To determine the optimized bias point for the first driver stage, two-tone and AM/PM measurements were conducted using a vector signal generator, a vector network analyzer, and a spectrum analyzer. For IMD3 meas-

urements, two-tone signals having 20 kHz tone spacing at a 1640 MHz frequency were generated by the vector signal generator. The IMD3 levels at each output power were then measured using a spectrum analyzer. On the other hand, the AM/PM characteristics of the power amplifier were easily obtained by measuring the phase of S21 as a function of the input power using a vector network analyzer; this measurement technique is a single-tone test, which has been regarded as a conventional method for this task [4].

Fig. 6 shows the IMD3 levels as function of the output power based on bias variation of the first driver stage. In the figure, a small variation of DC bias current in the first driver stage strongly affects the overall linearity of the three-stage power amplifier. The IMD3 sweet spots were also shifted by the bias conditions; as the collector current of the first-stage was increased from 2.6 mA to 14.8 mA, the sweet spots moves from 31 dBm to 29 dBm output power. When the first driver stage has a low bias, the PA has the closest sweet spots to the 1 dB compression point. This result indicates that we can obtain some benefits of linearity at a very high output power range. But in the low output power, IMD3 increases more than 5 dBc compared to the high first driver stage bias case (14.8 mA) when the first driver stage has a low bias current (2.6 mA).

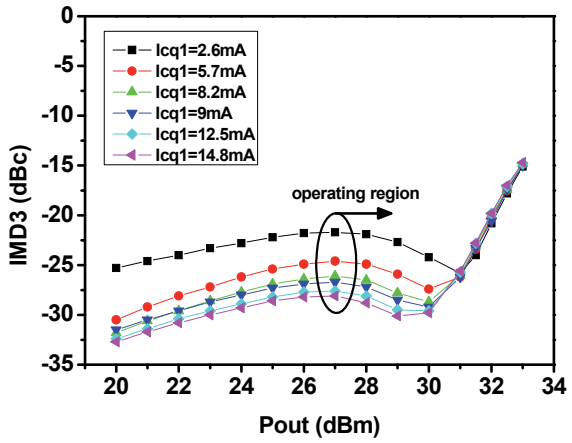


Fig. 6. Measured IMD3 versus output power under different bias conditions of the first driver stage.

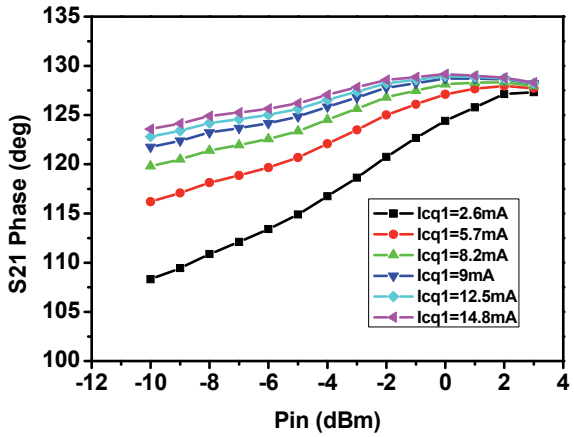


Fig. 7. Measured AM/PM characteristics under different bias conditions of the first driver stage.

Fig. 7 shows the AM/PM characteristics of the PA under various first driver stage bias conditions. The measured phase of S21 is plotted as a function of the input power. As the input power is further increased, the insertion phase shift of the PA also gradually increases. For the 2.6mA bias current, the AM-to-PM conversion is about 2.1 deg/dB; other cases show 1.2 deg/dB for 8.2 mA, and 0.7 deg/dB for 14.8 mA. As the collector bias current of the first driver stage is decreased, the AM-to-PM conversion of the overall PA increases.

In order to select the optimized bias current of the first driver stage, we measured the linearity of the three-stage power amplifier, including IMD3 and AM/PM. When the first driver stage bias current was 2.6 mA, the sweet spot of the IMD3 was very high, but the AM-to-PM conversion was too large; at a low power range, the IMD3 level was too low. In addition, the gain flatness of the PA also became degraded because the gain expansion increased. When the collector bias current was 14.8 mA, the PA had good gain flatness, low AM-to-PM conversion, and good linearity in the low output power range. However, the sweet spots of IMD3 were too low. In other words, there were no linearity benefits at a very high output power range because of the low sweet spots. Moreover, efficiency of the overall PA was also reduced due to the increased DC power consumption of the first driver stage. Therefore, the optimized collector bias current of the first driver stage was selected to be 8.2 mA because at this current the PA has appropriate linearity in the low output power range, low AM-to-PM conversion, and IMD3 sweet spots close to the 1-dB compression point. Fig. 8 shows the measured and simulated results of the three-stage PA with the two-tone signals which have a center frequency of 1640 MHz and a tone-spacing of 20 kHz. The differences between the measured and the simulated are about 7 dB in gain, more than 5 dBc in IMD3. It results from inaccurate large signal model of a GaAs HBT.

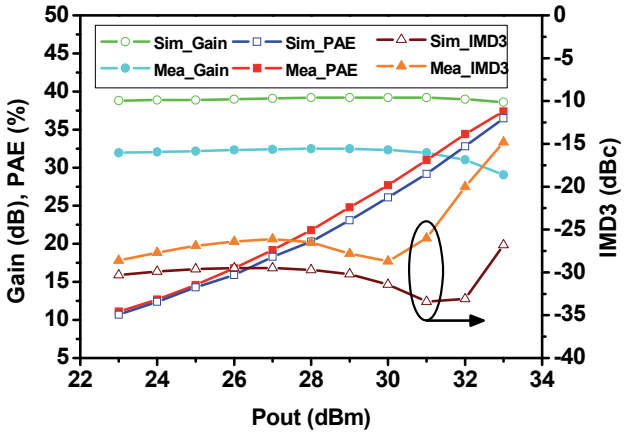
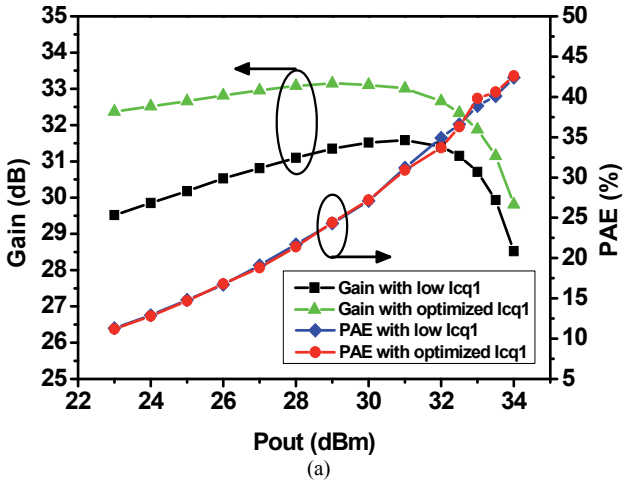


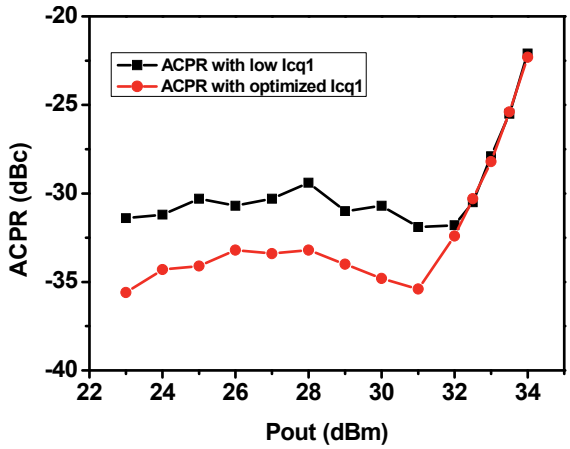
Fig. 8. The simulated and measured results of the three-stage PA for two-tone excitation (Icq1 = 8.2 mA).

Fig. 9 shows the measured performance of three-stage power amplifier using the π/4 DQPSK signal. Fig. 9(a) describes the gain versus output power of the PA at 1640 MHz for a single 3.6 V supply voltage. The PA gain

was 31.9 dB with the Icq1= 8.2 mA, 30.7 dB with the Icq1=2.6 mA at 33 dBm output power. With the raised first driver stage bias current, the PA has good gain flatness less than 1 dB. Fig. 9(b) then presents the ACPR characteristics versus output power at 1.64 GHz. For the ACPR-measurement, a π/4 DQPSK modulation signal (α= 0.35, channel spacing = 31.25 kHz, channel BW = 23.4 kHz) was generated by a vector signal generator. From the figure, the ACPR for the output power of 33 dBm achieved -28.2 dBc at an offset of 31.25 kHz. Compared with the PA using low first-stage bias current, it shows better linearity in the lower power region. Tab. I shows performance comparison with other PAs. Compared to the others, the proposed three-stage power amplifier shows comparable performance.



(a)



(b)

Fig. 9. Measured performances of the three-stage power amplifier using the π/4-DQPSK signal: (a) gain and PAE, (b) ACPR.

Ref.	Pout	PAE (%)	Linearity	Signal
[5]	33dBm	34	-28dBc	IS-95
[6]	30dBm	40	-28dBc	Two-tone
This work	33dBm	39.8	-28.2dBc	π/4 DQPSK

Tab. 1. Performance comparison.

5. Conclusion

In this paper, the third-order intermodulation distortion of three-stage PAs is analyzed using the Volterra series expansion. The analysis has shown that the IM3 voltage consists of three vectors, which are related with the first-stage bias. The simulated results show that the vector summation is decreased by the first-stage bias current rise. Based on the measurement data, it has been verified that the PA has the better IMD3 performance by increasing the bias current of the first-stage. The developed three-stage power amplifier for satellite mobile communications has a very high P1dB of 33 dBm, using an InGaP/GaAs HBT. All matching circuits were integrated into a small MMIC chip (1.7 mm x 1.4 mm).

To obtain higher P1dB and good gain flatness, the bias current of the first driver stage was optimized. For a π/4 DQPSK modulation signal, a power amplifier operating at 3.6 V achieved a high linear output power of 33 dBm (2 W), a PAE of 39.8%, and a gain of 31.9 dB at 1640 MHz. The measured ACPR was -28.2 dBc at a channel offset of 31.25 kHz.

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Jongsoo LEE was born in Seoul, Korea in 1971. He received his BS, MS and Ph.D from Korea Advanced Institute of Science and Technology in 1994, 1996 and 2001, respectively. After his Ph.D, he joined start-up company, Telephus for developing front end module in mobile wireless communications. From 2003 to 2004, he was a research faculty at Georgia Institute of Technology in Atlanta, GA working on RFIC and mmW IC with SiGe HBT technology. From 2004 to 2007, he was a senior design engineer at RF Micro Devices in Phoenix, AZ working on highly integrated power amplifier and front end modules for mobile phones. He is currently an assistant professor at Gwangju Institute of Science and Technology (GIST) since 2007 and his research interests include advanced power amplifier designs, transmitter architecture for wireless communications, multiband power amplifiers, antenna tuners and mmW IC designs beyond 60 GHz.