Design of a 2.4 GHz High-Performance Up-Conversion Mixer with Current Mirror Topology

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Abstract. *In this paper, a low voltage low power up-conversion mixer, designed in a Chartered 0.18 μm RFCMOS technology, is proposed to realize the transmitter front-end in the frequency band of 2.4 GHz. The up-conversion mixer uses the current mirror topology and current-bleeding technique in both the driver and switching stages with a simple degeneration resistor. The proposed mixer converts an input of 100 MHz intermediate frequency (IF) signal to an output of 2.4 GHz radio frequency (RF) signal, with a local oscillator (LO) power of 2 dBm at 2.3 GHz. A comparison with conventional CMOS up-conversion mixer shows that this mixer has advantages of low voltage, low power consumption and high-performance. The post-layout simulation results demonstrate that at 2.4 GHz, the circuit has a conversion gain of 7.1 dB, an input-referred third-order intercept point (IIP3) of 7.3 dBm and a noise figure of 11.9 dB, while drawing only 3.8 mA for the mixer core under a supply voltage of 1.2 V. The chip area including testing pads is only 0.62×0.65 mm^2.*

Keywords

CMOS, up-conversion mixer, current mirror, current-bleeding, low voltage, low power.

1. Introduction

In the last few years, the growing demand for wireless communication applications has led to extensive researches on radio frequency (RF) integrated circuits and systems with the advanced CMOS technologies. Designs for low voltage, low power, and highly integrated circuits have been significant considerations in RF front-end systems, such as IEEE 802.11b WLAN and Bluetooth standards [1]. In the RF transmitter front-end, the up-conversion mixer is one of the important blocks mainly used to convert an incoming intermediate frequency (IF) signal to an output RF signal. The signal is then transmit to the power amplifier for reliable transmission.

Several different solutions have been proposed to describe the researches of the CMOS mixers in recent years. Passive mixers have been widely adopted for direct conversion transceivers owning to their low supply voltage and low flicker noise characteristics, but they have conversion loss and require a high LO drive for operation [2]. An active mixer based on a bulk-injection method has been presented [3], [4]. The input signal is connected to the gates, and the LO frequency is connected to the bulk (wells, back-gates) of the input transistors or vice versa. By doing this, the required bias voltage is smaller than the threshold voltage of the device and then results in a low voltage and low power operation, but it suffers from limited gain and relatively poor noise performance. The conventional Gilbert-type mixer is commonly used because of the benefits in the active CMOS mixer design such as good port-to-port isolations and a low even-order distortion [5]. However, the supply voltage available to active mixer decreases with CMOS technology scaling, and therefore the issue of voltage headroom remains in low supply voltage design. A modified Gilbert-cell mixer with folded structure has often been published [6], [7]. Implementing the mixer with folded structure could reduce the number of stacked transistors and obtain a lower required supply voltage. However, because this method requires two branch currents to flow, it consumes a similar power as the conventional Gilbert-type mixer. Meanwhile, a very efficient implementation of current-bleeding with resonating inductor is presented in [8] which uses less current flow at the switching stage to lower the noise figure, but it still shows several limits in terms of circuit complexity and lower linearity. However, the linearity requirement of the up-conversion mixer will be higher than the down-conversion mixer.

This paper sets out to design and realize a low voltage, low power and high-performance integrated CMOS up-conversion mixer for IEEE 802.11b WLAN transmitter applications. The up-conversion mixer uses the current mirror topology and current-bleeding technique with a simple degeneration resistor, which can enhance the conversion gain and improve the linearity as well as the noise figure. Compared to the previously published CMOS mixer operating at the similar frequency ranges, the proposed up-conversion mixer has the advantages of the large conversion gain with 7.1 dB, high linearity, low noise figure and small power consumption, and it operates at a low supply voltage of 1.2 V.

The remaining parts of this paper are organized as follows. In Section 2, the design concept of the up-conversion mixer is described with operating principles of the current mirror topology and current-bleeding technique. The results of post-layout simulation are reported in Section 3 to verify the performances of the proposed CMOS up-conversion mixer. Finally, the conclusions of this work are given in Section 4.

2. Operational Principle and Circuit Implementation

Based on the traditional Gilbert-cell topology, a double balanced CMOS up-conversion mixer with some modifications was designed. Different from the previously published work, this mixer uses the current mirror topology [9], [10] and current-bleeding technique [11-13] in both the driver and switching stages with a simple degeneration resistor. Some of these critical sub-circuits are described in detail below.

2.1 Current Mirror Topology in the Driver Stage

The linearity of the conventional Gilbert-cell mixer is not good due to the nonlinearity of the driver stage, which becomes more serious especially at lower bias current. Because the current mirror topology is highly linear in regardless of the bias current, much better linearity can be expected [14]. Therefore, the current mirrors composed of M1-M3 and M4-M6 are added into the driver stage and the degeneration resistor R1 is connected between the output sides of the two current mirror transistors, as shown in Fig. 1. On the one hand, the required biasing voltage V_{b1} at the gate of the current mirror transistors M1 and M4 plays an important role in the low voltage capability of the mixer design. With proper transistor gate width of current mirror transistors M1-M3 and M4-M6, a suitable gate biasing voltage V_{b1} can be obtained, and thus results in a constant transconductance over a relatively wide range of input differential voltages which in turn translates into good linearity performance for the mixer. On the other hand, although even order nonlinearities are suppressed by the fully differential mixer configuration, the mismatch in the driver stage between the two current mirrors cause residual even-order distortion. Therefore, the degeneration resistor R1 is used for linearization of input driver stage again.

The gain of the current mirror can be easily set through appropriate scaling factor between the current mirror transistors. Since the current mirror gain K_{CM} can be written as:

$$K_{CM} = \frac{g_{m3,6}}{g_{m2,5}} = \frac{(W/L)_{3,6}}{(W/L)_{2,5}} \ . \tag{1}$$

When the IF signals $v_{IF\pm}(t) = \pm V_{IF} \cos \omega_{IF} t$ and LO signals $v_{LO\pm}(t) = \pm V_{LO} \cos \omega_{LO} t$ are applied, the RF output voltage V_{RF} can be written as:

$$\begin{aligned} V_{RF} &= V_{RF+} - V_{RF-} \\ &= r_{OL} * 2K_{CM} g_{m1,4} V_{IF} \cos(\omega_{IF}) t \times square\left[\cos(\omega_{LO} t)\right] \\ &= r_{OL} * 2K_{CM} g_{m1,4} V_{IF} \cos(\omega_{IF}) t \times \frac{4}{\pi}\left[\cos(\omega_{LO} t) + \frac{1}{3}\cos(3\omega_{LO} t) + ...\right] \\ &\approx \frac{4}{\pi} K_{CM} g_{m1,4} r_{OL} V_{IF} \cos(\omega_{IF} \pm \omega_{LO}) t \end{aligned} \tag{2}$$

Then the conversion gain (CG) of the mixer shown in Fig. 1 can be calculated as:

$$CG = \frac{V_{RF,rms}}{V_{IF,rms}} = \frac{2}{\pi} K_{CM} g_{m1,4} r_{OL} \tag{3}$$

with g_m is the input stage transconductance, r_{OL} is the output resistance of the RF terminal and W/L is the channel width to channel length ratio of the MOS devices.

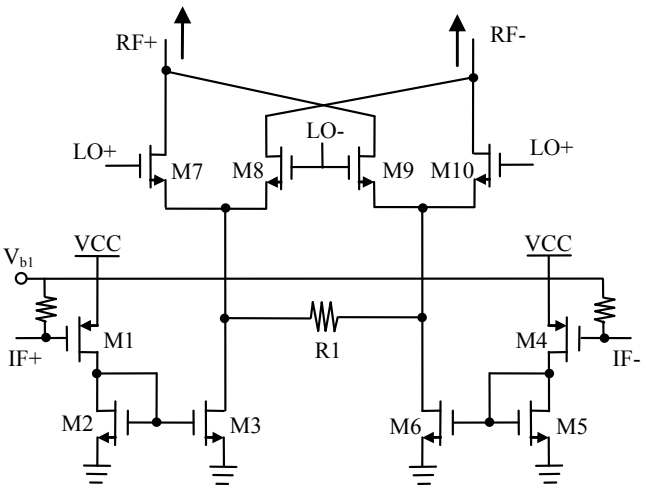

Fig. 1. Current mirror topology with a degenerative resistor in the driver stage.

From (3), the conversion gain can be increased by a factor of K_{CM} via the current mirror topology. However, the current mirror has a fundamental trade-off between gain and bandwidth. The gain-bandwidth product of the simple current mirror consisted of two current mirror transistors is given by [15]:

$$CG \times BW_{3dB} \approx \frac{K_{CM}}{K_{CM} + 1} \cdot \omega_T \approx \omega_T \tag{4}$$

where ω_T is the frequency with the unity gain of a current mirror transistor. Under this gain-bandwidth trade-off, the scaling factor of the current mirror can be carefully determined to get the optimal conversion gain.

2.2 Current-Bleeding Technique in the Switching Stage

The second improved method of the up-conversion mixer is the current-bleeding technique with a degeneration resistor. Fig. 2 is a typical bleeding circuit with two PMOS transistors (M11, M12) providing dc current into the driver stage. The PMOS pair provides high output impedance that is in parallel with the low input impedance of the switching pair. Therefore, the weak IF signal is forced to go into the switching pairs. The gain of the mixer is maximized with fast switching similar to a square wave. At the same time, the bias current through the driver stage can be increased without increasing the current through the switching transistors. Also, with bleeding, either the switching transistors can be operated at a lower gate-source voltage or smaller size transistors can be used.

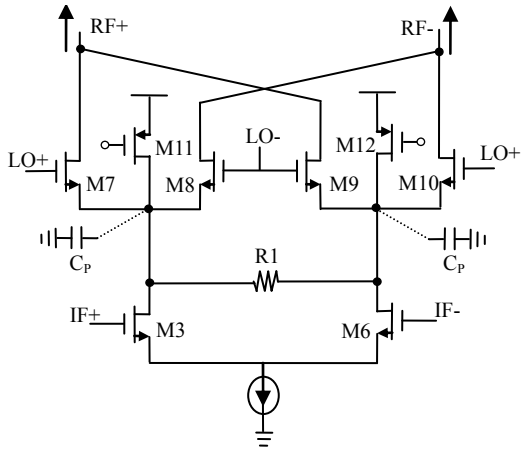

Fig. 2. Simplified schematic of current-bleeding with a degeneration resistor.

As shown in Fig. 2, C_p represents the tail capacitance of the LO switching stage. Then, the conversion gain will be reduced due to leakage of the IF signal to ground via the tail capacitance C_p. Our improved approach is to use the current-bleeding technique with an internal degeneration resistor R1 connected between the common source node of the LO switches. Since this is an up-conversion mixer and the common source node of the LO switches is operating at low frequency, a degeneration resistor in parallel to the two small tail capacitors of the switching transistors has been used to eliminate the LO leakage and current spikes. The effect of C_p is reduced, which means that not only the flicker noise is minimized but also conversion gain can be improved. The current-bleeding topology, incorporating with an internal degeneration resistor, has shown very good performance concerning conversion gain and noise figure.

2.3 Circuit Design

The complete schematic diagram of the proposed up-conversion mixer is shown in Fig. 3. The mixer consists of several parts, including the IF input driver stage, the LO switching stage, the current-bleeding circuit, the load stage and the output buffers.

The current mirror topology composed of transistors M1-M3 and M4-M6 acts as the input driver stage, as presented in the previous section. It can transfer the received incoming IF signals from voltage to current that served as the biased current of the upper four NMOS (M7-M10) transistors. The mixer gain and linear control can be easily set through appropriate scaling factor of the current mirror topology. While the upper transistors (M7~M10) act as switching cores to modulate the current provided by the driver stage, which is doubled balanced topology with the advantages of rejecting the strong LO signals and the even-order distortion products. To make M7-M10 transistors as ideal switches, the current-bleeding sources are used and the switching transistors are biased in the saturation region close to the triode region. The bleeding current can be tuned through the PMOS transistors M11 and M12. The current-bleeding technique with a degeneration resistor R1 in the switching stage is adopted for the up-conversion mixer to have not only a high conversion gain due to allow larger transconductance but also a low noise figure because of reduction of the flicker noise. On-chip capacitors (C1-C2 and C5-C8) are applied to be the DC-blocking capacitors to isolate the input or output port from the dc source. The circuit is biased by means of current mirrors (not shown in Fig. 3). V_{b1} to V_{b4} are the bias voltages with the maximum supply voltage at 1.2 V. The resistors R2 to R9 are added for signal choking, which must be selected so large that their equivalent interference current signals can be ignored. The main idea of the proposed up-conversion mixer is implemented with a linear and gain controlled current mirror topology in the driver stage and followed by a current-bleeding technique in the LO switching stage, and a simple degeneration resistor is applied in the driver and switching stages at the same time. The combination of several techniques offers a high degree of freedom to optimize the conversion gain and improve the linearity as well as the noise figure.

As the output load of up-conversion mixer, the two parallel LC resonant tanks (L1, C3) and (L2, C4) are used as the band-pass filter to reject the further products except the RF frequency at around 2.4 GHz. Nevertheless, the signal at the LO frequency plus the IF frequency, and the signal at the LO frequency minus the IF frequency, are both mixed to the RF frequency. Besides the desired signal (2.4 GHz), the image signal (2.2 GHz) is also produced. A common way of avoiding this image problem in fully-integrated transmitter is the use of I/Q up-conversion mixer, the IF signal is multiplied by both the in-phase (I) LO signal and a quadrature (Q) LO signal. Using this technique in the transmitter, the image and desired signals remain distinct in the complex RF signal. Finally, the output of the mixer is buffered with source followers in order to realize 50Ω output impedances. The buffers are designed to affect the mixer performance as little as possible, while the power consumption is not included in the mixer performance summary. The design parameters of most instances in Fig. 3 are summarized in Tab. 1.

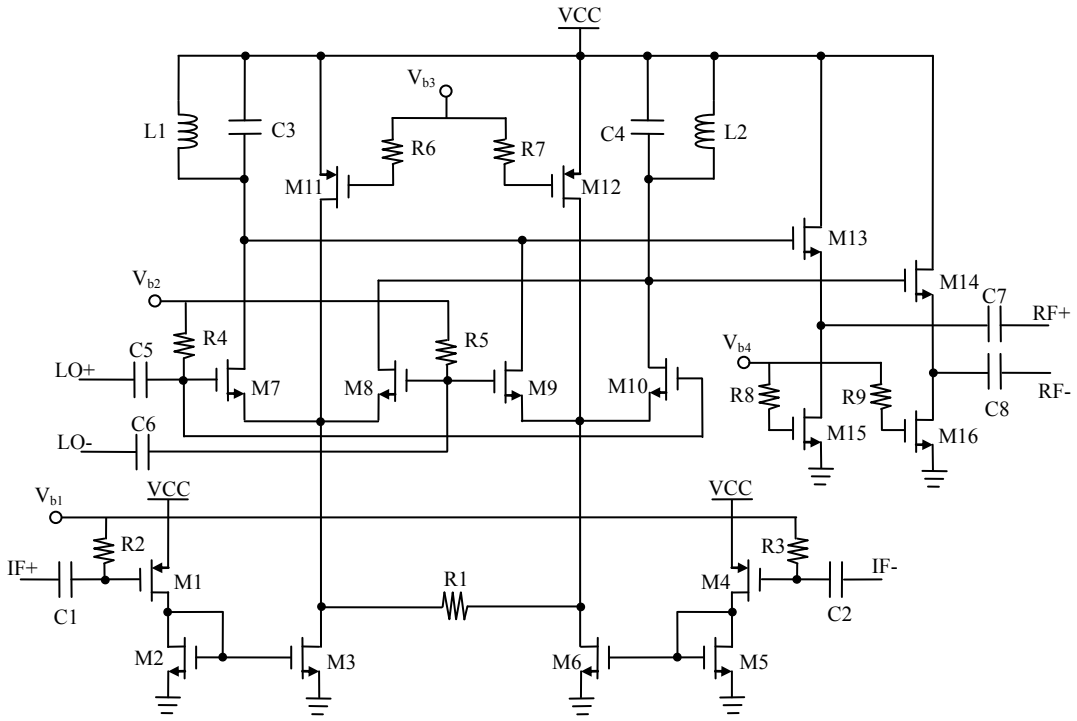

Fig. 3. Circuit diagram of the proposed CMOS up-conversion mixer.

Inst.	Para.	Inst.	Para.	Inst.	Para.
M1, M2	w/l =32/0.18 μm	C1,C2	4.6 pF	R1	5 kΩ
M4, M5	w/l =32/0.18 μm	C3,C4	1.5 pF	R2,R3	15kΩ
M3, M6	w/l =320/0.18 μm	C5,C6	4.8 pF	R4,R5	10kΩ
M7-M10	w/l =80/0.18 μm	C7,C8	6.8 pF	R6,R7	5 kΩ
M11,M12	w/l =160/0.18 μm	L1,L2	2.39 nH	R8,R9	15kΩ
M13,M14	w/l =200/0.18 μm	M15,M16	w/l =160/0.18 μm		

Tab. 1. Summary of instance parameters.

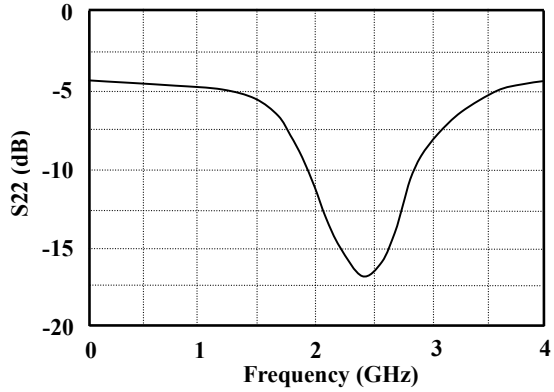

Fig. 4. S22 output return loss of the up-conversion mixer.

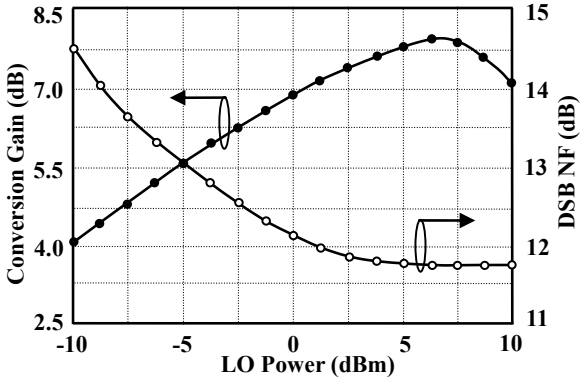

Fig. 5. The conversion gain and DSB noise figure versus LO power.

3. Post-Layout Simulation Results

The proposed up-conversion mixer with current mirror topology and current-bleeding technique is designed by Chartered 0.18 μm RFCMOS technology, and simulated using Cadence SpectreRF simulator. The Chartered's Design Rule (YI-093-DR001_Rev1V_1.8V-3.3V) and Chartered's Spice Model spec (yi093dr001_1v_00_ 20090731a) are used. The layout has been drawn and the arrangement has been placed as symmetrical as possible to decrease mismatches. All of the components in this design, including spiral inductors and metal-insulator-metal (MIM) capacitors, are on-chip implemented. The parasitic resistances and capacitances are also extracted from the layout and taken into account in simulation. Fig. 4 shows the simulation of the S22 (RF) output return loss, which is below −12.5 dB from 2.1 GHz to 2.7 GHz, indicating a good RF output matching. The simulated LO-to-IF, LO-to- RF, and IF-to-RF isolations from 1.5 GHz to 3 GHz are better than −48 dB, −50 dB, and −45 dB, respectively (not shown here). The intrinsic performance of the port-to-port

isolations in a conventional double-balanced Gilbert mixer is maintained.

In this design, the input signal at 100 MHz is up converted to 2.4 GHz through a 2.3 GHz LO signal. The conversion gain (CG) of the up-conversion mixer versus LO power is shown in Fig. 5. It shows that the proposed mixer can provide a large CG when the LO power is larger than 0 dBm. By taking into account that power amplifiers in transmitter are used to increase the signal gain and power, the necessary value of 2 dBm is chosen for LO power in which the CG of 7.1 dB is obtained for achieving a tradeoff between LO power and CG. Notice that too much LO power can deteriorate the linearity of the switching transistor pairs. The double-sideband (DSB) noise figure (NF) versus LO power is also depicted in Fig. 5. The DSB noise figure is 11.9 dB when the LO power is 2 dBm.

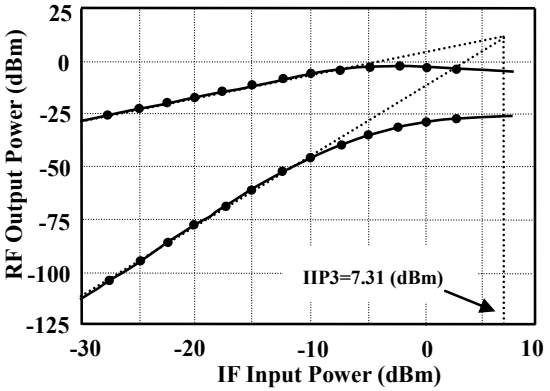

Fig. 6. IIP3 of the up-conversion mixer with the LO power at 2 dBm.

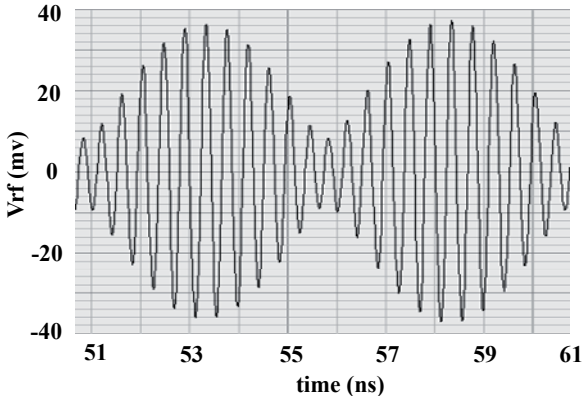

Fig. 7. The transient analysis of the up-conversion mixer.

Two tone tests have been performed for the input-referred third-order intercept point (IIP3) simulation as shown in Fig. 6. IIP3 is set at input frequency 100 MHz and 101 MHz with 1 MHz separation with IF input power and LO power is applied at -30 dBm and 2 dBm respectively. As can be seen in Fig. 6, the IIP3 of 7.3 dBm is obtained. Fig. 7 shows the transient simulation results with input IF signal at 100 MHz of which the signal level is -30 dBm and the LO signal at 2.3 GHz. The power dissipation of the mixer core is 4.56 mW from a 1.2V supply voltage. Although the output buffers show high power consumption, it can be actually neglected: on a higher level of integration no 50 Ω output matching will be needed. The layout diagram of the circuit is shown in Fig. 8, which takes a compact chip area of 0.62×0.65 mm^2 including testing pads.

Moreover, the specifications of the up-conversion mixer are summarized and listed in Tab. 2 and compared with those of prior references. As can be seen in Tab. 2, the proposed up-conversion mixer can achieve a large conversion gain and a good linearity with a low power consumption while, at the same time, achieving a small chip area by adjusting the compact structure.

Reference	[6]	[7]	[11]	[13]	This work
Technology	0.18 µm	0.18 µm	0.18 µm	0.25 µm	0.18 µm
LO power	0 dBm	0 dBm	0 dBm	4 dBm	2 dBm
CG	2.5 dB	5.8 dB	7.5 dB	3.8 dB	7.1 dB
IIP3	6.5 dBm**	-6 dBm	-5 dBm	-2 dBm	7.3 dBm
NF	--	13 dB	10.9 dB	8.0 dB	11.9 dB
Supply voltage	1 V	1 V	1.8 V	1.5 V	1.2 V
Power dissipation	39 mW	3.8 mW	8.1 mW	3.5 mW	4.5 mW
Area (mm^2)	1.4×1.3	1.0×1.1	0.88×0.88	0.6×0.6	0.62×0.65

** The result is estimated from its P_{1dB}.

Tab. 2. Performance summaries of the proposed mixer and comparison with other work.

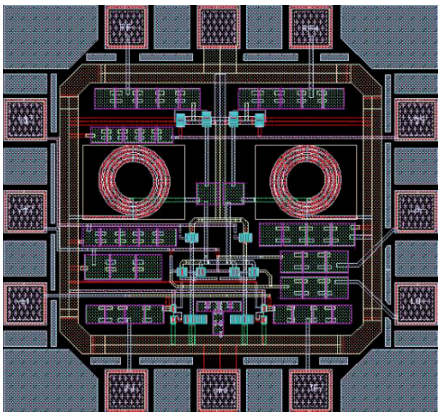

Fig. 8. The layout diagram of the up-conversion mixer (0.62×0.65 mm^2).

4. Conclusion

This paper has proposed the analysis and simulation of a 2.4 GHz up-conversion mixer based on a Chartered 0.18 µm RFCMOS technology. By using the current mirror topology and current-bleeding technique in both the driver and switching stages with a simple degeneration resistor, the overall conversion gain of the up-conversion mixer is enhanced and the input-referred third-order intercept point

(IIP3) is improved significantly. With the LO power of 2 dBm, the proposed up-conversion mixer has a large conversion gain of 7.1 dB, a good IIP3 of 7.3 dBm and a low noise figure of 11.9 dB, while it consumes 4.56 mW from a 1.2V supply voltage. The chip area including testing pads is only 0.62×0.65 mm^2. For the demands of modern wireless communications, such as IEEE 802.11b WLAN and Bluetooth applications, this RF mixer is suitable as a building block in low voltage and low power transceiver design owing to its superior performance.

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