Developing Model-Based Design Evaluation for Pipelined A/D Converters

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Abstract. *This paper deals with a prospective approach of modeling, design evaluation and error determination applied to pipelined A/D converter architecture. This is in contrast with conventional ADC modeling algorithms targeted to extract the maximum ADC non-linearity error. Our innovative approach presented in this paper allows decomposing magnitudes of individual error sources from a measured or simulated response of an ADC device. Design Evaluation methodology was successfully applied to Nyquist rate cyclic converters in our works [13]. Now, we extend its principles to pipelined architecture. This qualitative decomposition can significantly contribute to the ADC calibration procedure performed on the production line. This is background by the fact that the knowledge of ADC performance contributors provided by the proposed method helps to adjust the values of on-chip converter components so as to equalize (and possibly minimize) the total non-linearity error. In this paper, the design evaluation procedure is demonstrated on a system design example of pipelined A/D converter. Significant simulation results of each stage of the design evaluation process are given, starting from the INL performance extraction proceeded in a powerful Virtual Testing Environment implemented in Maple™ software and finishing by an error source simulation, modeling of pipelined ADC structure and determination of error source contribution, suitable for a generic process flow.*

Keywords

Pipelined A/D converter, ADC modeling, design evaluation, integral and differential non-linearity, error determination.

1. Introduction

1.1 Novel Design Evaluation Approach

Verification of design performance and subsequent device calibration of an A/D converter is a challenging task. This is backgrounded by the fact that the ADC performance depends on many parameters of the analog design part. This becomes apparent especially in complex design structures, such as pipelined A/D converters where the number of circuit components is high due to partitioning into several stages. Therefore, it is very uneasy to develop an explicit expression of the ADC performance contributors, represented in this case by the error sources of underlying circuit instances. Prior works were focused predominantly on a classical ADC modeling and design approach [1], [2] providing only the information about the maximum INL and DNL values, with no subsequent search for the root-cause error contributors. Interesting approach of pipeline ADC calibration was described in [3], [4]. Unfortunately, its application in our work is difficult as the method is dedicated for the post-fabrication measurement rather than design evaluation focused in this paper.

In contrast to this, the innovative approach of design evaluation presented in this article is capable to extract the magnitudes of individual error sources contributing to the ADC performance. Assigning an error mechanism to a specific circuit component or a group of instances, efficient ADC device calibration is possible. At this point, it should be emphasized that the design evaluation approach developed throughout our article represents an efficient tool for design optimization as an inherent part of the integrated circuit design flow.

1.2 Modeling and Parameter Extraction of Pipelined ADCs

The basic building blocks of pipelined ADCs [6] are organized into consecutive stages, each containing a sample&hold (S&H), a low-resolution ADC and DAC, and a summing circuit that includes an inter-stage amplifier. In our work, a combination of the pipelined architecture with a flash converter type is implemented into converter stages. The combined pipelined-flash ADC provides an optimum balance of speed and resolution, with respect to the power dissipation and the chip size. Therefore, this ADC type becomes increasingly attractive in data conversion. To optimize the pipelined ADC design, performance extraction is necessary as the first step of the evaluation procedure. For this purpose, we developed a powerful Virtual Testing Environment (VTE) [13]. The VTE proposed is

implemented in Maple™ and consists of program procedures to extract ADC errors expressed in term of integral and differential non-linearity (INL and DNL). To extract the ADC errors, an innovative variant of Servo-Loop method was developed – refer to Section 2. In Section 3, we follow the concept of an a priori ADC modeling with an emphasis to the error source identification and simulation. Subsequently, the design decomposition procedure with respect to the extracted error sources and error sources determination is applied in Section 4. Finally, the work conclusions are drawn in Section 5.

2. Advanced Servo-Loop Algorithm for Parameter Extraction

The method concerned is the Servo-Loop, being the core of the proposed virtual testing engine. In our work we apply an innovative approach developed on assumptions discussed in [7]. Consequently, the loop convergence is significantly accelerated, together with the reduced number of iterations. The implementation is shown in Fig. 1.

Compared to the standard solution [8], the asset of our Servo-Loop implementation is following: Cumsum circuit applies a priori known values to the input signal. Convergence process is assisted by an initial condition and by adaptive step refinement of the cumsum block. At this point, adjustment of the step size helps to accelerate the search for the loop equilibrium point as there is less iteration needed to maintain the same INL accuracy. The search complexity is changed from linear to logarithmic. Further details about the novel Servo-Loop algorithm are given in [7].
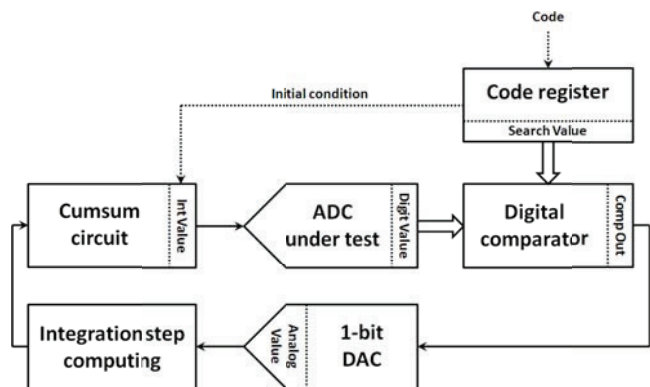

Fig. 1. Servo-Loop block diagram.

3. Pipelined ADC Modeling

3.1 Pipelined ADC Model Description

The ADC model under verification is a pipelined-flash structure proceeding stage-by-stage conversion algorithm corresponding to the scheme shown in Fig. 2.
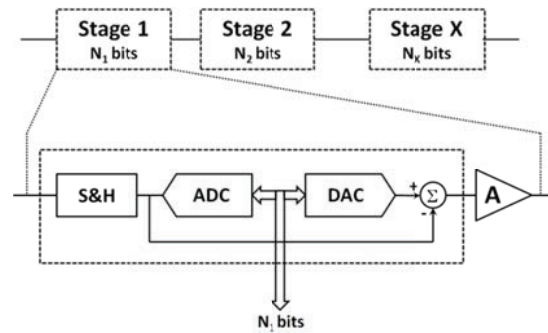

Fig. 2. Block diagram of pipelined A/D converter.

The behavioral pipelined flash ADC model consists of n stages, where each stage consists of a N_X-bit A/D sub-converter, D/A sub-converter, summing block and an interstage gain block (A). An N-bit conversion is accomplished by using at least two or more steps of sub-ranging (in this sense called pipelining), starting with the most significant bit (MSB). First, the analog input signal is converted in stage 1 providing N_1-bit resolution. Then, using a DAC with at least N_1-bit accuracy, the result is converted back to analog voltage and subtracted from the input voltage. Next, the difference is multiplied by 2^{N_1} and subsequently, the algorithm continues in the same way down to least significant bit (LSB). The main accuracy requirements are stressed on Sample&Hold, A/D converter threshold and interstage gain error. The flash A/D sub-converter used in our implementation is depicted in Fig. 3.
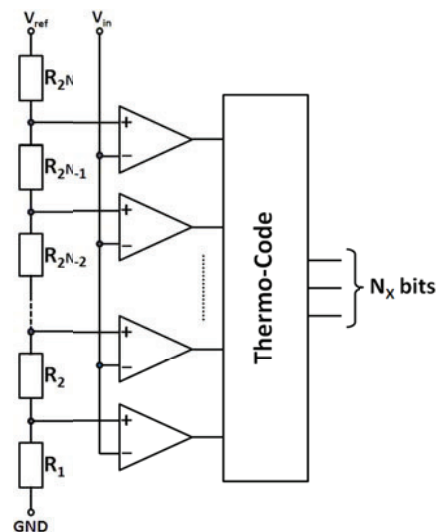

Fig. 3. Flash ADC stage.

Here, an ADC stage with N_X-bit resolution contains 2^N-1 comparators connected in parallel, with reference voltages V_{ref} set by a resistor network. Note that for the possible CMOS VLSI implementation, the resistive divider can be replaced by equation string of pseudo-resistors consisting of MOS operating in weak inversion region. This chip area saving simplification is possible under the condition that $N_X < 4$ for each sub-converter stage. The next section deals with the identification of the major a priori known error mechanisms occurring in the ADC architecture.

3.2 Identification of Architectural Error Sources

In the pipelined flash ADCs, errors can be classified into two main groups; systematic ADC error and code-specific ADC error [11]. In our work, we are concerned in code-specific errors from which the dominant ones are: *resistance error*, *comparator offset*, *inter-stage gain error* and finally, the *settling time*. The mechanism of resistance error (labeled as res_error) originates in the voltage divider and can be described by the formula (1a).

$$R_x' = R_x \cdot \left(1 - \frac{\text{res\_error[ppm]}}{10^6}\right) \qquad (1a)$$

where R_x' is the resistance value with resistance error, R_x is the ideal resistance value and res_error is the resistance error expressed in ppm.

The offset error labeled as off_error acts at each separate comparison level and occurs under condition given in (1b).

$$u_{in} - u_{ref} \cdot \frac{\sum\limits_{i=0}^{k} R_i}{\sum\limits_{j=0}^{2^N-1} R_j} \cdot \left(1 + \frac{\text{off\_error[ppm]}}{10^6}\right) > 0 \qquad (1b)$$

where u_{in} is the input voltage, u_{ref} is the reference voltage value, R_i and R_j are resistors in the voltage divider and off_error is the offset error expressed in ppm.

Finally, the inter-stage gain error, in (1c) denoted as ig_error acts between two converter stages and its occurrence is specific to the signal direction.

$$K' = 2^N \cdot \left(1 - \frac{\text{ig\_error[ppm]}}{10^6}\right) \qquad (1c)$$

where K' is the non-ideal interstage gain, N is the number of bits of this section and ig_error is the interstage gain error expressed in ppm.

The error sources described by (1a,b,c) exhibit a linear deviation or scaling with respect to its typical values usually expressed in ppm or absolute units. Beside these sources, a *signal distortion* can occur, caused by nonlinear device characteristic of the ADC components. A typical example is the *"tanh-shaped" distortion* of the inter-stage gain block (see amplifier A in Fig. 2) caused by the internal stages of the transistor-level OpAmp. The distorted characteristic of the inter-stage gain block ($K'= 1$ is assumed) can be described as:

$$y = C_1 \tanh\left(\frac{x}{C_2}\right) \qquad (2)$$

where x, y are the transfer function co-ordinates and C_1, C_2 are constants. Here, the C_2 constant is chosen upon the desired relative error level and the C_1 constant is calculated so that the transfer function endpoints are [0, 0] and [1, 1]. In Tab. 1, the distorted transfer characteristic is described by the *error_level* parameter varying from 1 to 3, deter-

mining the scale of relative and absolute errors. The resulting waveforms are illustrated in Fig.4a,b.

	Absolute error	Relative error
Error_level=1, defined as $y = 4{,}082988 \cdot \tanh(\frac{x}{4})$	< 0,008	< 0,025
Error_level=2, defined as $y = 8{,}041623 \cdot \tanh(\frac{x}{8})$	< 0,002	< 0,006
Error_level=3, defined as $y = 18{,}27384687 \cdot \tanh(\frac{x}{18{,}25559128})$	< 0,0005	< 0,0015

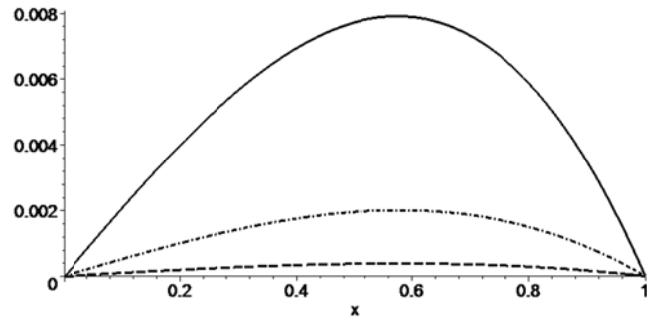**Tab. 1.** Error levels for tanh-shaped distortion.

Fig. 4a. Tanh-shaped distortion of the transfer characteristic (K'=1), absolute error $y = y_2 - y_1$ (Error level 1: dashed line, Error level 2: dot and dashed line, Error level 3: solid line).
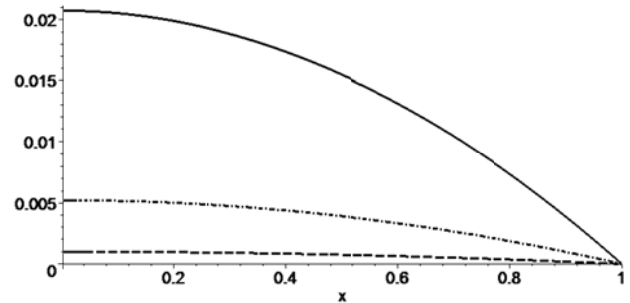

Fig. 4b. Tanh-shaped distortion of the transfer characteristic (K'=1), relative error $y = (y_2 - y_1)/y_1$ (Error level 1: dashed line, Error level 2: dot and dashed line, Error level 3: solid line).

3.3 Error Mechanism Simulation

In the previous section, most important error sources occurring in the pipelined ADC architecture were identified. The subsequent step in systematic design decomposition is to recognize the influence of the error sources to the INL characteristic. This can be done by simulating individual error mechanisms so as to sort-out the shape of the corresponding INL waveform and measure its peak-to-peak magnitude.

The VTE was running on the 8-bit ADC with pipelined-flash architecture (2+3+3 bits) from Fig. 2 and Fig. 3, focusing on the INL contributions of the inter-stage gain and offset error. On the shape of the error waveforms, a specific dependency of the pulse length on the ADC error magnitude can be observed.

From the simulated patterns [12] it is obvious that the ADC system response to the error mechanisms can be classified into two basic groups. In the first error group, the principle of linear scaling and superposition is valid, i.e. the magnitude of the INL and DNL characteristic is directly proportional to the error level [5]. In the second group of error sources represented by the inter-stage gain error, the linear superposition principle is violated. This is back-grounded by the quantization of INL contributions from the ADC stages, induced by a set of specific threshold values of error sources. Particularly, if the error source magnitude exceeds a specific value, a significant change of the corre-sponding INL contribution is invoked.

The INL response of the tanh-shaped distortion of the inter-stage gain block belongs to a special category in the error mechanism simulation. Since this error mechanism describes a non-linear process, the particular influence of other error sources has also to be taken into account; in our case, we consider two values of the inter-stage gain error [12]. Apparently, the non-linear distortion creates a mask-ing effect, breaking down the dependency of INL response on the ig_error level. However, for the tanh-shaped error level being sufficiently low, the ig_error influence is still well observable. Because of the masking effect, the tanh-shaped distortion has to be kept at a sufficiently low level in practical design considerations. In such a case, the non-linear effects can be separated in a systematical way so as to allow further decomposition process.

4. Design Decomposition and Performance Fitting

4.1 Decomposition Algorithm Background

This section introduces the innovative design decom-position flow carried out to the end of this article. Based on the simulated INL contribution of particular error sources present in the ADC model, we will demonstrate how the error sources and their combination will affect the total INL error. Specifically, the design decomposition will be understood in the sense of identification of the major com-ponents and their magnitudes in a simulated ADC device characteristic. As the "real" measured or simulated INL characteristic of a transistor-level ADC device was not available at the time of writing this article, a set of "pseudo-real" characteristics generated by the ADC model was used instead. Despite this fact, the decomposition pro-cedure described below provides a valuable feedback to the modeling procedure.

Applying the linear superposition principle (proven for an ADC response e.g. in [9], [10]), the resulting INL characteristic can be decomposed into a weighted sum of INL characteristics associated with individual error mecha-nisms. It is important to note that in our work, we demon-strate a suitable extent of the superposition principle to the set of linearly independent INL contributors which are

generated by magnitude variation of a single error source. Particularly, it is the case of the ig_error source which clearly violates the linearity assumption, but nevertheless can be attached into the decomposition flow. Fulfilling the conditions defined in Section 3.2, we arrange the remaining error contributors into the *model matrix* $\mathbf{B}_{mod}$:

$$\mathbf{B}_{\mathrm{mod}} = \begin{bmatrix} INL_{g1} & INL_{g2} & INL_{g3} & INL_{g4} & INL_{g5} & INL_{g6} & INL_{t1} & INL_{t2} & INL_{t3} & INL_{off} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ INL_{g1} & INL_{g2} & INL_{g3} & INL_{g4} & INL_{g5} & INL_{g6} & INL_{t1} & INL_{t2} & INL_{t3} & INL_{off} \end{bmatrix} \quad (3)$$

Apparently from (3), the model matrix contains one column per each error source contributor. Note that INL_{g1} to INL_{g6} correspond to the INL contribution generated by various magnitudes (100 ppm, 200 ppm, 500 ppm, 1000 ppm, 2000 ppm, 5000 ppm) of the inter-stage gain error in the first stage, as it is defined by (1c). Analogously, INL_{t1} to INL_{t3} correspond to the INL contribution generated by various magnitudes (500 ppm, 2000 ppm, 8000 ppm) of the tanh-shaped error, as it is defined by (2) and INL_{off} denotes the offset error contribution as it is defined by (1b). The decomposition of the device characteristic INLmod is given by:

$$INL_{\mathrm{mod}} = \mathbf{B}_{\mathrm{mod}}\mathbf{x} + \Delta_{LACK} \quad (4)$$

where $INL_{mod} \in R^{2^N}$ is the total characteristic of the pipelined ADC model, $\mathbf{x}$ is the vector of weights of individual error sources, $\Delta_{LACK} \in R^{2^N}$ denotes the lack-of-fit underlying error mechanisms not captured by the model matrix $\mathbf{B}_{mod}$. As the first design decomposition step, we estimate the vector of weights as:

$$\widetilde{\mathbf{x}} = LeastSquares(\mathbf{B}_{\mathrm{mod}}, INL_{\mathrm{mod}}) \quad (5)$$

Subsequently, the lack-of-fit is calculated as follows:

$$\Delta_{LACK} = INL_{\mathrm{mod}} - \mathbf{B}_{\mathrm{mod}}\widetilde{\mathbf{x}} \quad (6)$$

4.2 Practical Algorithm Implementation

For practical use with pipelined ADC, the design de-composition procedure established by (3)-(5) needs to be enhanced by determination of error source magnitudes from the components of the vector $\widetilde{\mathbf{x}}$. With respect to the simulation result, the offset error fulfills the linear superpo-sition principle with respect to the INL response.

For the gain error source, the situation is a bit more complicated, as we need an iteration search procedure to find the error source magnitude. This can be done by the following algorithm:

$$x := LeastSquares(\mathbf{B}_{\mathrm{mod}})\}. \quad (7)$$

The algorithm body (7) described above is repeated in a loop until $x([i_{\mathrm{iter}}]-1)^2 < \varepsilon$. Here, $\mathbf{B}_{mod}$ is the model matrix with selected INL components INL_{gain}, INL_{offset} and INL_{tanh}.

The concrete asset of the practical algorithm imple-mentation is apparent from Fig. 5 (reduced for IG error to

1000 ppm). Here, the x[1] to x[4] are the error weighs plotted versus the ig_error parameter. Obviously, the global maxima of the x[1] to x[4] curves indicate the concrete values of the ig_error level present in the ADC INL response. In such a way, the inter-stage gain error level can be determined by "filtering-out" the response of the tested device-under-test.
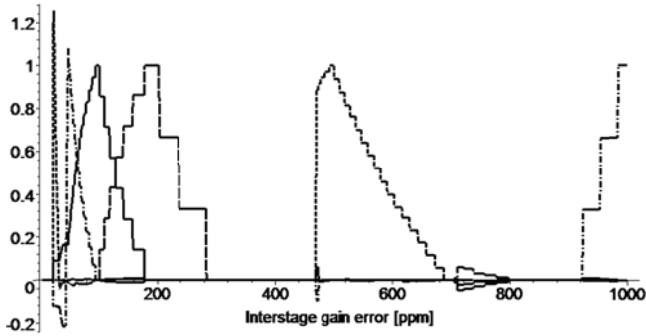

Fig. 5. Decomposed model vector coefficients for ig_error parameter (x[1] solid, x[2] short-dash, x[3] long-dash, x[4] dot-and-dash line).

4.3 Error Sources Determination

First, the transfer characteristic of a real ADC is decomposed following equation (5) and the Offset error (Temperature) is determined following equation:

$$Temperature = 300 + (Temp_{Reference} - 300) \cdot x[10] \quad (8)$$

where $x[10]$ is the ratio between the INL curve of a pseudoreal ADC and INL curve given by the offset reference $Temp_{Reference}$.
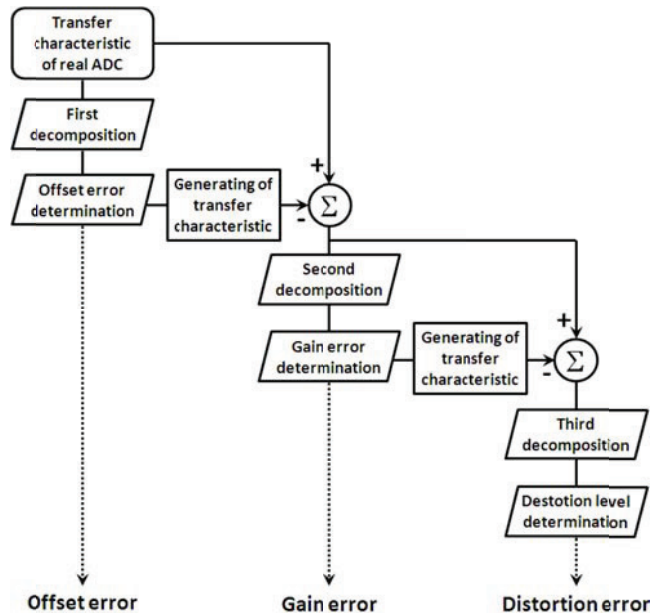

Fig. 6. Flowchart of successive error determination.

Then, using the determined Offset error, the Transfer characteristic of a virtual ADC with only Offset error is created following equation (1b). Finally, the transfer char-

acteristic of pseudo-real ADC is subtracted from the transfer characteristic of ADC with only Offset error.

According to this process, the gain and distortion error are determined (see Fig. 6).

4.4 Decomposition Example

As the "real" measured or simulated INL characteristic of a transistor-level ADC device was not available at the time of writing this article, a set of "pseudo-real" characteristics generated by the ADC model was used for production line emulation.

These results were proven by decomposition algorithm and evaluated the result accuracy. After finishing of the algorithm according to Fig.6, we received very accurate results (see Tab. 2).

No.	Pseudoreal ADC	Decomposed results
1	T = 240 K, IGE = 1400 ppm	T = 236 K, IGE = 1596 ppmm
2	T = 260 K, IGE = 1400 ppm	T = 258 K, IGE = 1279 ppm
3	T = 300 K, IGE = 2400 ppm	T = 301 K, IGE = 2394 ppm
4	T = 300 K, IGE = 4400 ppm	T = 300 K, IGE = 4241 ppm
5	T = 320 K, IGE = 1000 ppm	T = 321 K, IGE = 674 ppm
6	T = 320 K, IGE = 3200 ppm	T = 320 K, IGE = 3291 ppm
7	T = 320 K, IGE = 4400 ppm	T = 320 K, IGE = 4476 ppm

Tab. 2. Comparison of values of real ADC and determined results.

5. Conclusions

The main contribution of this work is the development of a systematical design evaluation methodology suitable for Nyquist-rate A/D converters. Particularly, the decomposition flow was solved and demonstrated for pipelined ADC devices frequently used in IC design solutions. Compared to prior approaches [5], [9], [10], the proposed decomposition algorithm can also proceed the ADC error sources which violate linearity assumption. Practical asset of the decomposition algorithm is expected namely in the custom ADC design with an emphasis on the optimization proceed on behavioral or full transistor-level.

Acknowledgements

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Pravoslav MARTINEK was born in Ústí nad Labem on September 6, 1936. He received the Electrical Engineering degree (Ing.) and PhD (CSc.) degree from the Czech Technical University in Prague, Faculty of Electrical Engineering in 1967 and 1974, respectively. In 1968 he joined the Department of Circuit Theory at CTU and has been an Associate Professor since 1984. His primary research interest is analog signal processing, continuous- and discrete-time analog filters and current-mode electronic circuits. He has been a member of the European Circuit Society (ECS) since 1995.