Tunable Versatile High Input Impedance Voltage-Mode Universal Biquadratic Filter Based on DDCCs

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Abstract. *A high input impedance voltage-mode universal biquadratic filter with three input terminals and seven output terminals is presented. The proposed circuit uses three differential difference current conveyors (DDCCs), four resistors and two grounded capacitors. The proposed circuit can realize all the standard filter functions, namely, lowpass, bandpass, highpass, notch and allpass, simultaneously. The proposed circuit offers the features of high input impedance, using only grounded capacitors, and orthogonal controllability of resonance angular frequency and quality factor.*

Keywords

Current conveyor, biquadratic filter, active circuit, voltage-mode.

1. Introduction

The differential difference current conveyors (DDCC) [1] or differential voltage current conveyors (DVCC) [2], [3] have received considerable attention on realizing multifunction filters and oscillators. This is due to the fact that the addition and subtraction operations for voltage signals can be performed easily.

High input impedance voltage-mode active filters are of great interest because several cells of this kind can be directly connected in cascade to implement higher order filters [4]-[6]. Besides the use of only grounded capacitors and resistors are beneficial from the point of view of integrated circuit fabrications [7]-[9].

Several high input impedance voltage-mode universal biquads each with multi-input terminals were presented in [5], [10]-[14]. Five kinds of standard filter functions can be derived by the selections of different input voltage terminals in these circuits. However, only one standard filter function can be obtained in each realization of [5], [10]-[12]. Moreover, four kinds of standard filter functions at most can be obtained, simultaneously, in each circuit realization of [13], [14]. Moreover, the resonance angular frequencies and quality factors of these circuits cannot be orthogonally controllable. Three multi-inputs and one output universal biquads were presented in [15]-[17]. Although the resonance angular frequencies and quality factors of these circuits can be orthogonally controllable, they require passive components matching conditions in the realizations of some filter functions. Two high input impedance three-inputs and one output universal biquads were presented in [18]. However, the resonance angular frequency and quality factor of the first proposed circuit cannot be orthogonally controllable and both circuits require passive components matching conditions in the realization of allpass filter functions.

The circuits that consist of more filter functions mean more applications they can be used. Therefore, many high input impedance circuits that can realize all of the standard filter functions; namely highpass, bandpass, lowpass, notch and allpass from the same circuit configuration simultaneously were presented in the literatures [15], [19]-[25]. However, the resonance angular frequencies and quality factors of the circuits in [15], [19], [20] cannot be orthogonally controllable. The circuits in [21]-[25] have the feature of orthogonally controllable of resonance angular frequencies and quality factors but they use floating resistors.

In this paper, a new high input impedance voltage-mode universal biquadratic filter with three input terminals and seven output terminals using three DDCCs is presented. The proposed circuit uses four resistors and two grounded capacitors. The proposed circuit has the following features: (i) high input impedance, (ii) using only grounded capacitors, (iii) five kinds of standard filter functions can be obtained simultaneously from the same circuit configuration, and (iv) orthogonal controllability of resonance angular frequency and quality factor. Moreover, if one of the output terminals at the proposed circuit is not required (deleted), five kinds of filter functions still can be obtained from the circuit by appropriate selecting the input terminals. This circuit configuration needs not passive component matching condition in the realization of all filter types and using only grounded passive components. With respect to the multi-inputs universal biquads in [5], [10]-[14], the resonance angular frequency and quality factor can be orthogonally controllable in the proposed circuit. With respect to the three inputs universal biquads in [15]-[18], the proposed circuit needs no passive compo-

nents matching conditions in the realization of allpass filter functions. Comparisons of some multi-inputs biquads are given in Tab. 1. Tab. 1 shows the features of the proposed circuit in orthogonally controllable of resonance angular frequency and quality factor and using only grounded passive components. Comparisons of some multi-outputs biquads that can realize all of the standard filter functions simultaneously are given in Tab. 2.

2. Circuit Description

Using standard notation, the port relations of an ideal DDCC can be characterized by

$$\begin{bmatrix} v_x \\ i_{y_1} \\ i_{y_2} \\ i_{y_3} \\ i_{z1} \\ \dots \\ i_{zk} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 & 0 & \dots & 0 \\ 0 & 0 & 0 & 0 & 0 & \dots & 0 \\ 0 & 0 & 0 & 0 & 0 & \dots & 0 \\ 0 & 0 & 0 & 0 & 0 & \dots & 0 \\ 0 & 0 & 0 & \pm 1 & 0 & \dots & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \pm 1 & 0 & \dots & 0 \end{bmatrix} \begin{bmatrix} v_{y1} \\ v_{y2} \\ v_{y3} \\ i_x \\ v_{z1} \\ \dots \\ v_{zk} \end{bmatrix} \quad (1)$$

where the plus and minus signs indicate whether the conveyor is configured as a non-inverting or inverting type circuit, termed DDCC+ or DDCC-.

The proposed configuration is shown in Fig. 1. The output voltages can be expressed as:

$$V_{out1} = \frac{(s^2C_1C_2G_1 + G_1G_2G_3)V_{in1} - sC_1G_2G_3V_{in2} - s^2C_1C_2G_3V_{in3}}{s^2C_1C_2G_1 + sC_1G_2G_3 + G_1G_2G_3} \quad (2)$$

$$V_{out2} = \frac{-sC_1G_1G_2V_{in1} - sC_1G_1G_2V_{in2} + (sC_1G_2G_3 + G_1G_2G_3)V_{in3}}{s^2C_1C_2G_1 + sC_1G_2G_3 + G_1G_2G_3} \quad (3)$$

$$V_{out3} = \frac{G_1G_2G_3V_{in1} + G_1G_2G_3V_{in2} + sC_2G_1G_3V_{in3}}{s^2C_1C_2G_1 + sC_1G_2G_3 + G_1G_2G_3} \quad (4)$$

$$V_{out4} = \frac{sC_1G_2G_3V_{in1} + sC_1G_2G_3V_{in2} + s^2C_1C_2G_3V_{in3}}{s^2C_1C_2G_1 + sC_1G_2G_3 + G_1G_2G_3} \quad (5)$$

$$V_{out5} = \frac{s^2C_1C_2G_1V_{in1} + s^2C_1C_2G_1V_{in2} - (s^2C_1C_2G_3 + sC_2G_1G_3)V_{in3}}{s^2C_1C_2G_1 + sC_1G_2G_3 + G_1G_2G_3} \quad (6)$$

$$V_{out6} = \frac{-sC_1G_1G_2V_{in1} - sC_1G_1G_2V_{in2} - s^2C_1C_2G_1V_{in3}}{s^2C_1C_2G_1 + sC_1G_2G_3 + G_1G_2G_3} \quad (7)$$

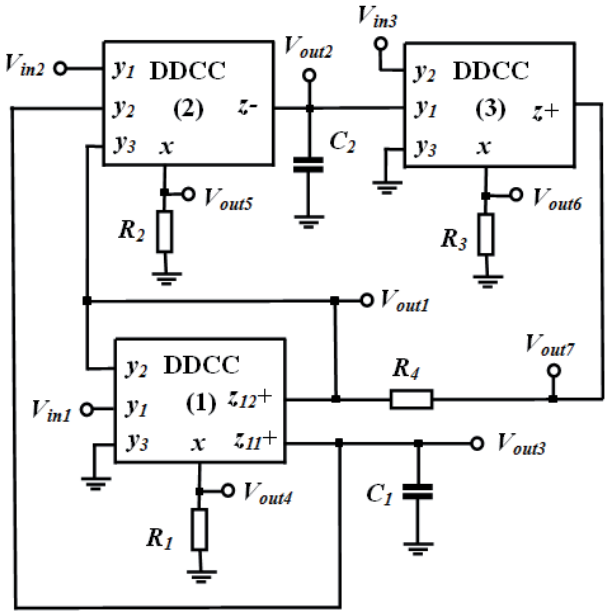


Fig. 1. The proposed universal filter.

$$V_{out7} = \frac{\begin{aligned}&(s^2C_1C_2G_1 - sC_1G_1G_2G_3R_4 + G_1G_2G_3)V_{in1} \\ &-(sC_1G_2G_3 + sC_1G_1G_2G_3R_4)V_{in2} \\ &-(s^2C_1C_2G_3 + s^2C_1C_2G_1G_3R_4)V_{in3}\end{aligned}}{s^2C_1C_2G_1 + sC_1G_2G_3 + G_1G_2G_3} \quad (8)$$

From (2)–(8), we can see that six circuit types can be obtained from Fig. 1:

(1) If $V_{in2} = V_{in3} = 0$ (grounded); V_{in1} = input voltage signal, a notch filter can be obtained at V_{out1}, three bandpass filters can be obtained at V_{out2}, V_{out4} and V_{out6}, a lowpass filter can be obtained at V_{out3}, a highpass filter can be obtained at V_{out5} and and if $R_4 = R_1$, an allpass filter can be obtained at V_{out7}.

(2) If $V_{in1} = V_{in3} = 0$ (grounded); V_{in2} = input voltage signal, five bandpass filters can be obtained at V_{out1}, V_{out2}, V_{out4}, V_{out6} and V_{out7}, a lowpass filter can be obtained at V_{out3}, and a highpass filter can be obtained at V_{out5}.

(3) If $V_{in1} = V_{in2} = 0$ (grounded); V_{in3} = input voltage signal, four highpass filters can be obtained at V_{out1}, V_{out4}, V_{out6} and V_{out7} and a bandpass filter can be obtained at V_{out3}.

(4) If $V_{in3} = 0$ (grounded), then $V_{in1} = V_{in2}$ = input voltage signal, an allpass filter can be obtained at V_{out1}, three bandpass filters can be obtained at V_{out2}, V_{out4} and V_{out6}, a lowpass filter can be obtained at V_{out3} and a highpass filter can be obtained at V_{out5}.

(5) If $V_{in2} = 0$ (grounded), then $V_{in1} = V_{in3}$ = input voltage signal and $R_3 = R_1$, two lowpass filters can be obtained at V_{out1} and V_{out2} and a bandpass filter can be obtained at V_{out5}.

(6) If $V_{in1} = 0$ (grounded), then $V_{in2} = V_{in3}$ = input voltage signal and $R_3 = R_1$, a lowpass filter can be obtained at V_{out2} and a bandpass filter can be obtained at V_{out5}.

	Active device	Needs inverting inputs	Grounded passive components	Floating passive components	Matching constraints	High input impedance	ω_o/Q orthogonal controllability	Kinds of filter functions simultaneously
[5]	three CCIIs	yes	0	4	no	yes	no	1
[10]	three DDCCs	no	4	0	no	yes	no	1
[11]	one DDCC one FDCCII	no	4	0	no	yes	no	1
[12]	three DDCCs	no	5	0	yes	yes	no	1
[13]	three DDCCs	no	4	0	no	yes	no	4
[14]	One DDCC one FDCCII	no	4	0	no	yes	no	4
[15] Fig. 3	three DVCCs	no	5	0	yes	yes	yes	1
[16]	four CFAs	no	3	4	yes	yes	yes	1
[17]	three CFAs	no	4	3	yes	yes	yes	1
[18], Fig. 1	three DVCCs	no	5	1	yes	yes	no	1
[18], Fig. 2	two DVCCs one DDCC	no	6	0	yes	yes	yes	1
New circuit	three DDCCs	no	5	0	no	yes	yes	4

Tab. 1. Comparisons of some multi-inputs biquads (The resistor R_4 in the proposed circuit is shorted).

	Active device	Grounded passive components	Floating passive components	Matching constraints	High input impedance	ω_o/Q orthogonal controllability
[15], Fig. 2	three DVCCs	5	0	yes	yes	no
[19], Fig. 1	two FDCCIIs	4	0	no	yes	no
[20]	three DDCCs	3	1	no	yes	no
[21]	five CFAs	5	3	yes	yes	yes
[22]	two DVCCs	3	2	yes	no	yes
[23]	three DVCCs	3	2	yes	yes	yes
[24]	three DDCCs	4	1	no	yes	yes
[25]	three DVCCs	4	2	yes	yes	yes
New circuit	three DDCCs	5	1	yes	yes	yes

Tab. 2. Comparisons of some biquads that can realize all of the standard filter functions simultaneously.

The resonance angular frequency ω_0 and quality factor Q are obtained by

$$\omega_o = \sqrt{\frac{G_2 G_3}{C_1 C_2}}, \tag{9}$$

$$Q = G_1 \sqrt{\frac{C_2}{C_1 G_2 G_3}}. \tag{10}$$

In first circuit type, all standard filter functions can be simultaneously obtained from the same circuit configuration. If the output terminal V_{out7} is not required, the floating resistor R_4 is not needed and can be shorted. Note that if the output terminal V_{out7} is not needed, five kinds of filter functions still can be realized by appropriate selecting the input terminals without component matching condition and using only grounded passive components.

The proposed circuit uses grounded capacitors, which are attractive for integrated circuit implementation [7]. Due to the three input signals, V_{in1}, V_{in2} and V_{in3}, are connected to the high input impedance input nodes of the three DDCCs (the y port of the DDCC), respectively, the proposed circuit enjoys the feature of high input impedance. From (9), (10), the resonance angular frequency can be controlled by R_2 or R_3. The quality factor can be independently controlled by R_1. Therefore, the resonance angular frequency and quality factor can be orthogonally controllable.

3. Sensitivities Analysis

Taking the non-idealities of the DDCC into account, the relationship of the terminal voltages and currents can be rewritten as

$$\begin{bmatrix} v_x \\ i_{y1} \\ i_{y2} \\ i_{y3} \\ i_z \end{bmatrix} = \begin{bmatrix} \alpha_{k1}(s) & -\alpha_{k2}(s) & \alpha_{k3}(s) & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm\beta_k(s) \end{bmatrix} \begin{bmatrix} v_{y1} \\ v_{y2} \\ v_{y3} \\ i_x \end{bmatrix} \tag{11}$$

where $\alpha_{k1}(s)$, $\alpha_{k2}(s)$, and $\alpha_{k3}(s)$ represent the frequency transfer functions of the internal voltage followers and $\beta_k(s)$ represent the frequency transfer function of the internal current follower of the k-th DDCC. They can be approximated by first order lowpass functions, which can be considered to have a unity value for frequencies much lower than their corner frequencies [2]. If the circuit is working at frequencies much lower than the corner frequencies of $\alpha_{k1}(s)$, $\alpha_{k2}(s)$, $\alpha_{k3}(s)$ and $\beta_k(s)$, then $\alpha_{k1}(s) = \alpha_{k1} = 1 - \varepsilon_{k1v}$ and ε_{k1v} ($|\varepsilon_{k1v}| << 1$) denotes the voltage tracking error from y_1 terminal to x terminal of the k-th DDCC, $\alpha_{k2}(s) = \alpha_{k2} = 1 - \varepsilon_{k2v}$ and ε_{k2v} ($|\varepsilon_{k2v}| << 1$) denotes the voltage tracking error from y_2 terminal to x terminal of the k-th DDCC, $\alpha_{k3}(s) = \alpha_{k3} = 1 - \varepsilon_{k3v}$ and ε_{k3v} ($|\varepsilon_{k3v}| << 1$) denotes the voltage tracking error from y_3 terminal to x terminal of the k-th DDCC and $\beta_k(s) = \beta_k = 1 - \varepsilon_{ki}$ and ε_{ki} ($|\varepsilon_{ki}| << 1$) denotes the current tracking error of the k-th DDCC. The denominator of the non-ideal output voltage function for Fig. 1 becomes

$$\begin{aligned} D(s) = {} & s^2 C_1 C_2 G_1 \alpha_{12}\beta_{12} + sC_1 G_2 G_3 \alpha_{23}\alpha_{31}\beta_2\beta_3 \\ & + G_1 G_2 G_3 \alpha_{12}\alpha_{22}\alpha_{31}\beta_{11}\beta_2\beta_3 \end{aligned}. \tag{12}$$

The resonance angular frequency ω_0 and quality factor Q become

$$\omega_o = \sqrt{\frac{G_2 G_3 \alpha_{22}\alpha_{31}\beta_{11}\beta_2\beta_3}{C_1 C_2 \beta_{12}}}, \tag{13}$$

$$Q = \frac{G_1 \alpha_{12}}{\alpha_{23}} \sqrt{\frac{C_2 \alpha_{22}\beta_{11}\beta_{12}}{C_1 G_2 G_3 \alpha_{31}\beta_2\beta_3}}. \tag{14}$$

The active and passive sensitivities of ω_0 and Q are shown as

$$S^{\omega_o}_{\alpha_{22},\alpha_{31},\beta_{11},\beta_2,\beta_3} = -S^{\omega_o}_{\beta_{12}} = S^{\omega_o}_{G_2,G_3} = -S^{\omega_o}_{C_1,C_2} = \frac{1}{2};$$

$$S^{Q}_{\alpha_{12}} = -S^{Q}_{\alpha_{23}} = S^{Q}_{G_1} = 1;$$

$$S^{Q}_{\alpha_{22},\beta_{11},\beta_{12}} = -S^{Q}_{\alpha_{31},\beta_2,\beta_3} = \frac{1}{2};$$

$$S^{Q}_{C_2} = -S^{Q}_{C_1,G_2,G_3} = \frac{1}{2}.$$

All the active and passive sensitivities are no larger than 1.

4. Influence of Parasitic Elements

A non-ideal DDCC model is shown in Fig. 2 [26]. It is shown that the real DDCC has parasitic resistors and capacitors from the y_1, y_2, y_3 and z terminals to the ground, and also, a series resistor at the input terminal x. Taking into account the non-ideal DDCCs and assuming the circuits are working at frequencies much lower than the corner frequencies of $\alpha_i(s)$, and $\beta_j(s)$, namely, $\alpha_i \cong \beta_j \cong 1$. Moreover, in practical DDCCs, the external resistors can be chosen to be much smaller than the parasitic resistors at the y and z terminals of DDCCs and much greater than the parasitic resistors at the x terminals of DDCCs, i.e. R_y, $R_z >> R_k >> R_x$. The external capacitances C_1 and C_2 can be chosen to be much greater than the parasitic capacitors at the y and z terminals of DDCCs, i.e. C_y, $C_z << C_1$, C_2. Furthermore, assuming that the resistances $R_4 = R_1$ and the parasitic capacitances at the y terminals and z terminals of the DDCCs are equal, i.e. $C_y \cong C_z$.

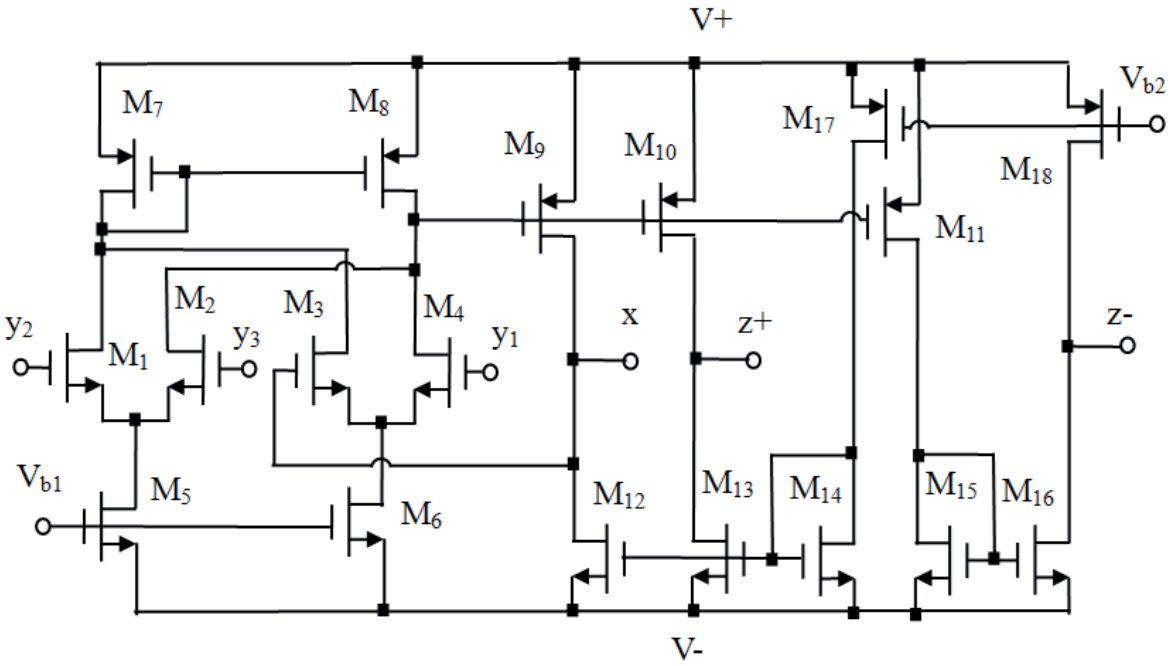


Fig. 3. The CMOS realization of the DDCC.

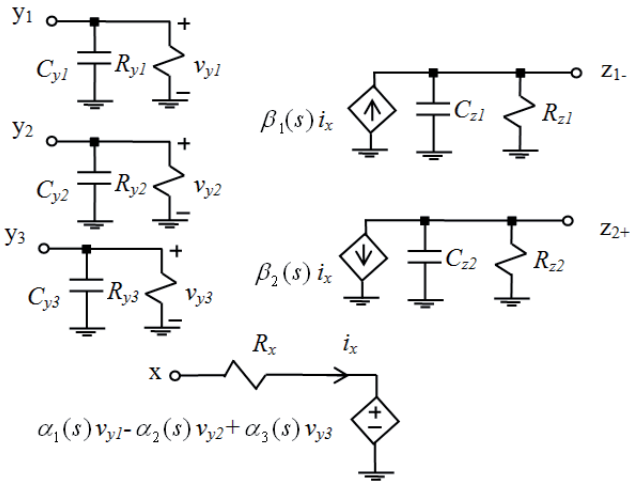


Fig. 2. The non-ideal DDCC model.

Under these conditions, the denominator of Fig. 1 becomes

$$D(s) \cong 2s^4 C_1'C_2'C_z^{\,2} + 4s^3 C_1'C_2'C_z G_1' + s^2 C_1'C_2'G_1'^2 + sC_1'G_1'G_2'G_3' + G_1'^2 G_2'G_3' \quad (15)$$

where

$$C_1' = C_1 + C_{z11} + C_{y22},\quad C_2' = C_2 + C_{z2} + C_{y31},$$
$$R_1' = R_1 + R_{x1},\quad R_2' = R_2 + R_{x2},\quad R_3' = R_3 + R_{x3}.$$

In (15), undesirable factors are yielded by the non-idealities of the DDCCs. The capacitance C_z becomes effective at very high frequency. To minimize the effects of the DDCCs' non-idealities, the operation angular frequency should be restricted to the following conditions

$$\omega << \min\{\frac{1}{\sqrt{2}R_1'C_z}, \frac{1}{2}\sqrt{\frac{1}{C_2'C_zR_2'R_3'}}\}. \quad (16)$$

Moreover, application of the Routh-Hurwitz test to the denominator of (15) shows that C_z may cause instability. According to this test, the transfer functions is stable if

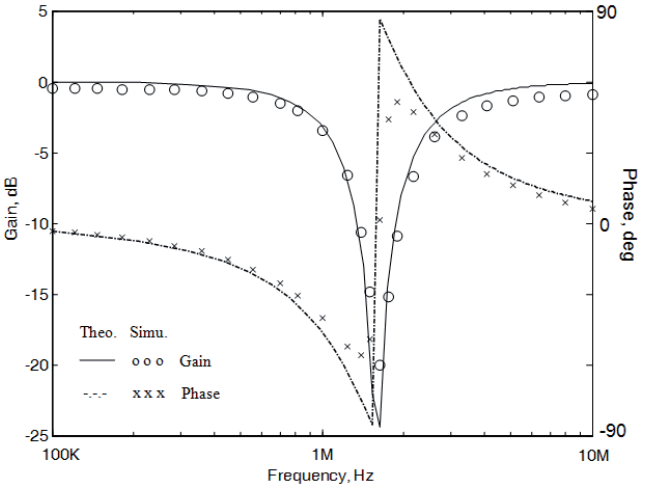
$$C_2' > \max\{C_z(\frac{G_2'G_3'}{2G_1'^2}), C_z\frac{8C_2'G_1'^2 + C_1'G_2'G_3'}{2C_1'G_1'^2}\}. \quad (17)$$

It is not difficult to satisfy this condition, since the external capacitance C_2 can be chosen very much greater than C_z.

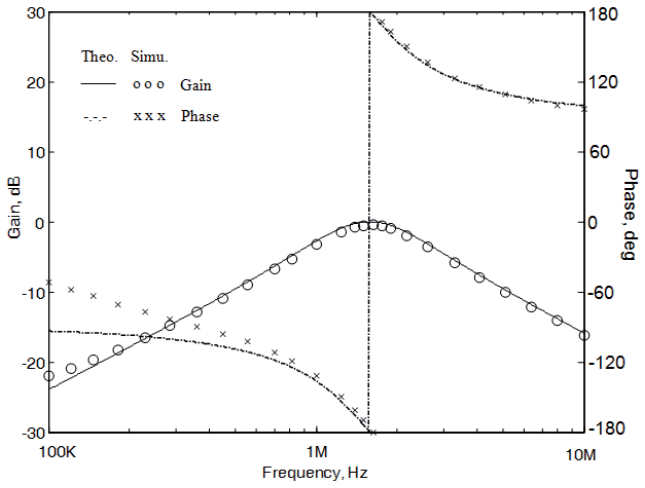
5. Simulation Results

HSPICE simulations were carried out to demonstrate the feasibility of the proposed circuit in Fig. 1. The DDCC was realized by the CMOS implementation of Elwan and Soliman [2] (by ungrounding the gate of MOSFET M_2 and treating this as the third y-input y_3) and is redrawn in Fig. 3. The simulations use TSMC (Taiwan Semiconductor Manufacturing Company, Ltd.) 0.18μm level 49 CMOS technology process parameters. The supply voltages are $V+ = +1.25$ V, $V- = -1.25$ V, $V_{b1} = -0.45$ V and $V_{b2} = 0.3$ V. The dimensions of the NMOS transistors in the DDCC are set to be W = 4.5 μm and L = 0.9 μm. The dimensions of the PMOS transistors in the DDCC are set to be W = 9 μm and L = 0.9 μm. Fig. 4 (a)-(g) represent the simulated frequency responses for the notch (V_{out1}), inverting bandpass (V_{out2}), lowpass (V_{out3}), bandpass (V_{out4}), highpass (V_{out5}), inverting bandpass (V_{out6}) and allpass (V_{out7}) filters of

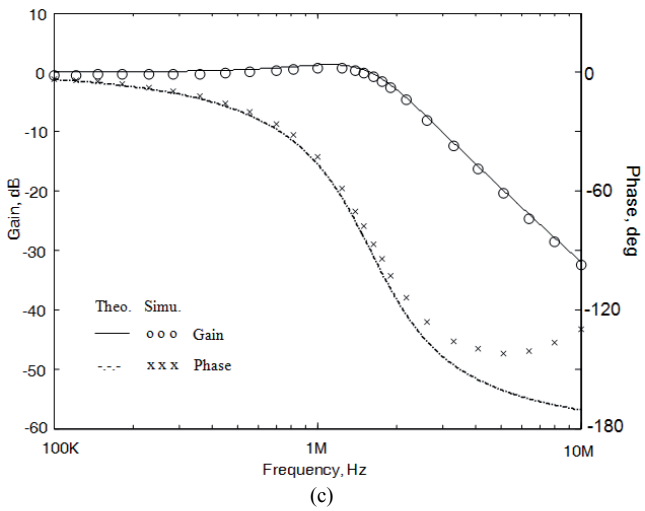
Fig. 1, respectively, designed with $V_{in2} = V_{in3} = 0$ (grounded), V_{in1} = input voltage signal, $Q = 1$ and $f_o = 1.5915$ MHz: $C_1 = C_2 = 10$ pF and $R_1 = R_2 = R_3 = R_4 = 10\ \text{k}\Omega$. Fig. 5 represents the INOISE and ONOISE simulation results of the bandpass filter at V_{out4}. Fig. 6 shows the the total harmonic distortion (THD) of the V_{out2} and V_{out4} output voltages (bandpass signals). They are given at 1.5915 MHz operation frequency with V_{in1} = input voltage signal, $V_{in2} = V_{in3} = 0$ (grounded) and $Q = 1$: $C_1 = C_2 = 10$ pF and $R_1 = R_2 = R_3 = R_4 = 10\ \text{k}\Omega$. Fig. 6 shows that the THDs of V_{out2} and V_{out4} are less than 3 percent at 1000 mV output voltages (peak to peak).



(a)



(b)



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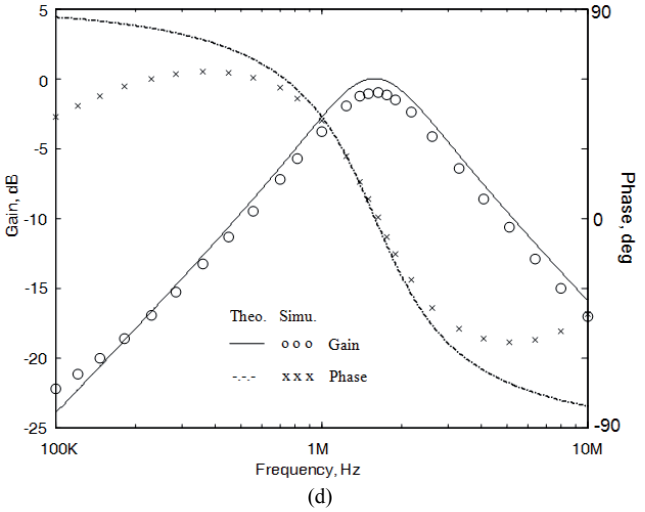

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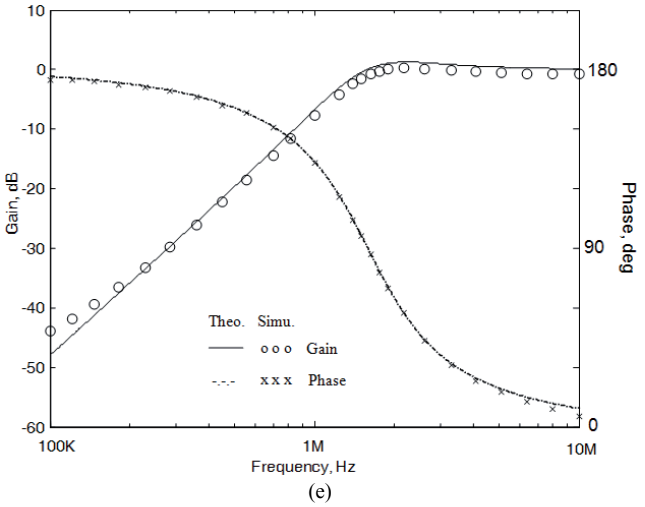

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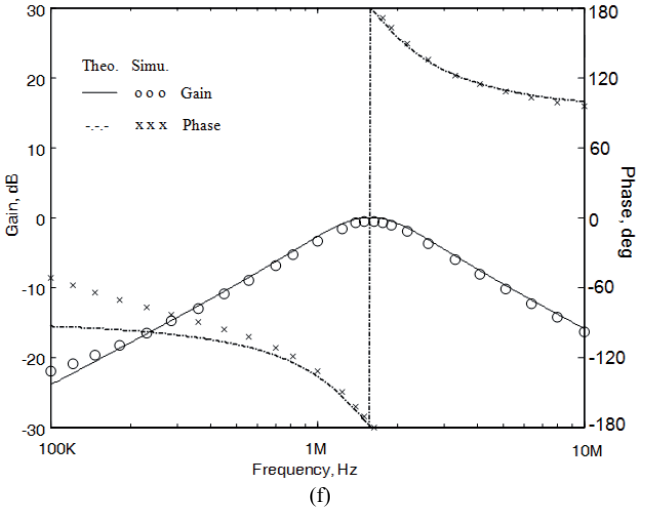
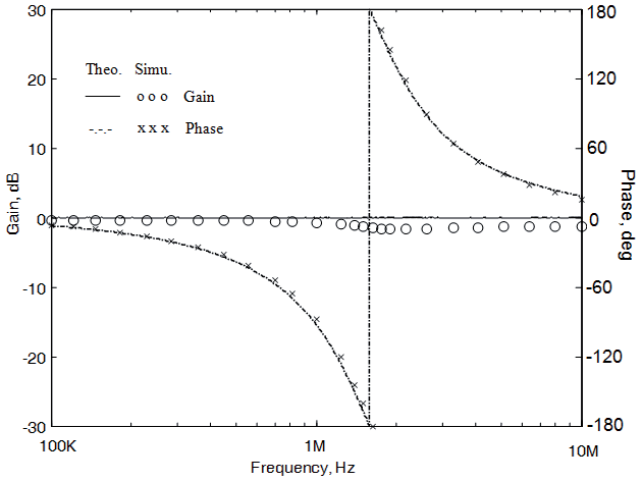


(f)



(g)

Fig. 4. Simulated frequency responses of Fig. 1 designed with $V_{in2} = V_{in3} = 0$ (grounded), V_{in1} = input voltage signal: (a) notch filter (V_{out1}), (b) inverting bandpass filter (V_{out2}), (c) lowpass filter (V_{out3}), (d) bandpass filter (V_{out4}), (e) highpass filter (V_{out5}), (f) inverting bandpass filter (V_{out6}), (g) allpass filter (V_{out7}).

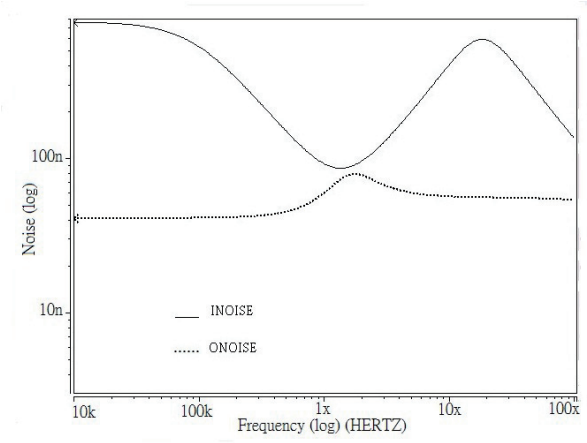


Fig. 5. INOISE and ONOISE simulation results of the proposed bandpass filter at V_{out4}.

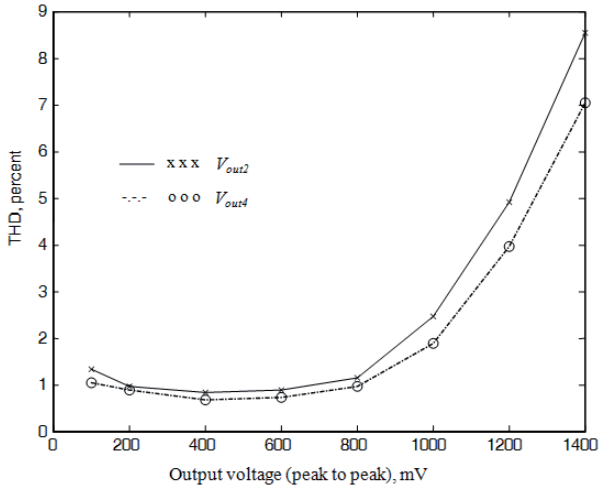


Fig. 6. THD analysis results of the proposed bandpass filters at V_{out2} and V_{out4}.

Fig. 7 represents the simulated frequency responses for the allpass (V_{out1}) filter of Fig. 1, designed with $V_{in3} = 0$ (grounded), $V_{in1} = V_{in2}$ = input voltage signal, $Q = 1$ and $f_o = 1.5915$ MHz: $C_1 = C_2 = 10$ pF and $R_1 = R_2 = R_3 = R_4 = 10$ kΩ. Fig. 8 represents the simulated gain responses for the inverting highpass (V_{out1}) filter of Fig. 1, designed with $V_{in1} = V_{in2} = 0$ (grounded); V_{in3} = input voltage signal, $Q = 1$ and $f_o = 1.5915$ MHz: $C_1 = C_2 = 10$ pF and $R_1 = R_2 = R_3 = R_4 = 10$ kΩ. Fig. 9 represents the simulated frequency responses for the inverting bandpass (V_{out2}) filter of Fig. 1 as the resistor R_1 in Q is varied designed with $V_{in2} = V_{in3} = 0$ (grounded) and V_{in1} = input voltage signal: $C_1 = C_2 = 10$ pF and $R_2 = R_3 = R_4 = 10$ kΩ. The quality factor was found to vary as 3.157, 1.988, 1.468 and 0.994 for four values of R_1 as 2 kΩ, 4 kΩ, 6 kΩ and 10 kΩ, respectively. All the simulation results are coherent and support the theoretical analyses.

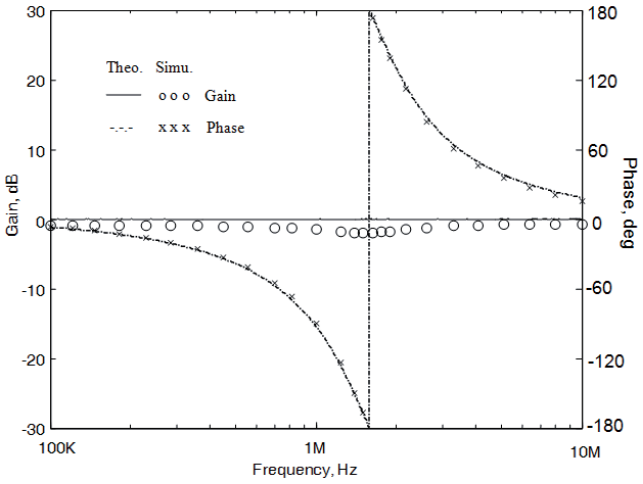


Fig. 7. Simulated frequency responses for the allpass filter (V_{out1}) of Fig. 1 designed with $V_{in3} = 0$ (grounded), $V_{in1} = V_{in2}$ = input voltage signal, $C_1 = C_2 = 10$ pF, and $R_1 = R_2 = R_3 = R_4 = 10$ kΩ.

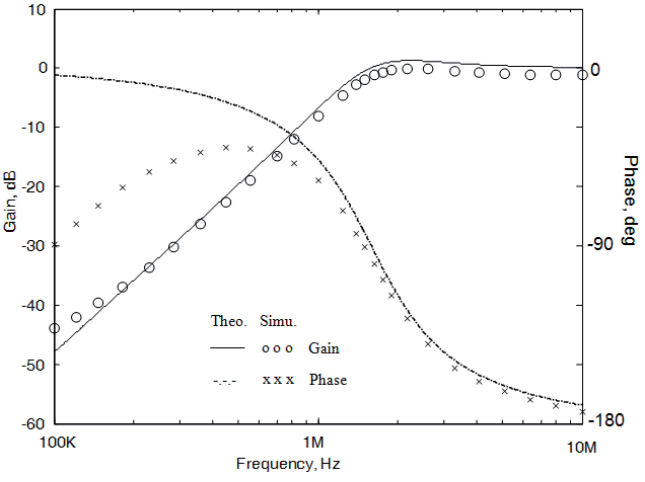


Fig. 8. Simulated gain responses for the highpass filter (V_{out1}) of Fig. 1 designed with $V_{in1} = V_{in2} = 0$ (grounded); V_{in3} = input voltage signal, $C_1 = C_2 = 10$ pF, and $R_1 = R_2 = R_3 = R_4 = 10$ kΩ.

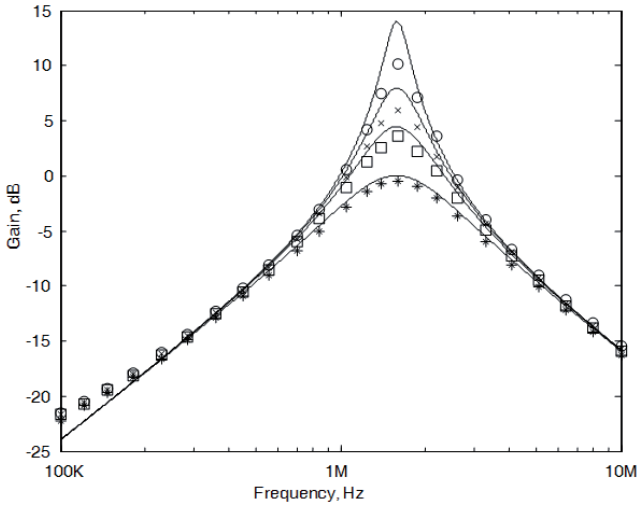


Fig. 9. Simulated frequency responses for the inverting bandpass filter of Fig. 1 designed with $C_1 = C_2 = 10$ pF and $R_2 = R_3 = R_4 = 10$kΩ.
____ , ideal curve; o o o, $R_1 = 2$ kΩ; x x x, $R_1 = 4$ kΩ; □ □ □ , $R_1 = 6$ kΩ; * * *, $R_1 = 10$ kΩ.

The DDCC has parasitic resistor from the z terminal to the ground (R_z) [26]. When the z terminal load of the DDCC is a capacitor (C), it introduces a pole produced by R_z and C at low frequency. This can explain why Fig. 4(b), 4(d), 4(f) and Fig. 8 have non-ideal phase responses at low frequencies. This effect can be minimized by using larger loading capacitors.

6. Conclusion

In this paper, a new high input impedance voltage-mode universal biquadratic filter with three input terminals and seven output terminals is presented. The proposed circuit uses three DDCCs, four resistors and two grounded capacitors and offers the following advantages: high input impedance, the use of only grounded capacitors, the versatility to synthesize lowpass, bandpass, highpass, notch, and allpass responses, simultaneously and orthogonal controllability of resonance angular frequency and quality factor.

Finally, it should be mentioned that if the output terminal V_{out7} at the proposed circuit is not required, the floating resistor R_4 can be deleted. Note that five kinds of filter functions still can be obtained from this circuit by appropriate selecting the input terminals. This circuit configuration needs not passive component matching condition in the realizations of all filter functions and using only grounded passive components.

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