Modified Level Restorers Using Current Sink and Current Source Inverter Structures for BBL-PT Full Adder

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Abstract. *Full adder is an essential component for the design and development of all types of processors like digital signal processors (DSP), microprocessors etc. In most of these systems adder lies in the critical path that affects the overall speed of the system. So enhancing the performance of the 1-bit full adder cell is a significant goal. In this paper, we proposed two modified level restorers using current sink and current source inverter structures for branch-based logic and pass-transistor (BBL-PT) full adder [1]. In BBL-PT full adder, there lies a drawback i.e. voltage step existence that could be eliminated in the proposed logics by using the current sink inverter and current source inverter structures. The proposed full adders are compared with the two standard and well-known logic styles, i.e. conventional static CMOS logic and Complementary Pass transistor Logic (CPL), demonstrated the good delay performance. The implementation of 8-bit ripple carry adder based on proposed full adders are finally demonstrated. The CPL 8-bit RCA and as well as the proposed ones is having better delay performance than the static CMOS and BBL-PT 8-bit RCA. The performance of the proposed BBL-PT cell with current sink & current source inverter structures are examined using PSPICE and the model parameters of a 0.13 μm CMOS process.*

Keywords

Full adders, high-speed, current sink inverter, current source inverter, CMOS digital integrated circuits, performance analysis.

1. Introduction

Full adder is the fundamental gate in many arithmetic circuits, such as adders and multipliers. Thus, enhancing the performance of the full adder block leads to enhancement of overall system of performance. In addition to its main task, i.e. adding two binary numbers, it has been evolved as the most important block involving in multiple operations such as subtraction, multiplication, division, address-calculation, etc. In most of these systems the adder is a part of the critical path that determines the overall performance of the system [1-3].

Adders play significant role in the final phase of signal processing in some advanced architectures of high-speed analog-to-digital converters. Accordingly, extensive research is being carried out to develop novel architectures, circuit configurations, layouts, design styles, and design methodologies with the aim of improving adder speed and energy efficiency [4]-[8]. The performance parameter of the full adder seems to be delay, power consumption and power-delay product. The logic style used in the logic gates basically influences the speed, size, power dissipation and the wiring complexity of a circuit. The circuit delay is determined by number of inversion levels, the number of transistors in series, their sizes (i.e. channel widths) and intra-cell wiring capacitances etc. Circuit size depends on the number of transistors, their sizes and on their wiring complexity. Some of them use one logic style for the whole full adder, whereas, others use more than one logic style for their implementation. Recently, building the low-power VLSI systems has gained momentum because of the fast growth of technologies in mobile communication and computation. However, the battery technology doesn't exhibit faster growth compared to microelectronics technology. There is however a limited amount of power availability for the mobile systems. So designers are faced with more constraints such as high speed, high throughput, small silicon area and at the same time low-power consumption. So building low-power, high-performance adder cells is an important factor in today's growing VLSI Technologies [9]-[12].

There are standard implementation methods for the full-adder cells such as:

1. The conventional CMOS full adder [13] circuit has 28 transistors and is based on the regular CMOS structure composed of pull-up PMOS and pull-down NMOS networks.

2. The complementary pass-transistor logic (CPL) full adder [13], [14] based circuit has 32 transistors. In CPL two different parts are used for implementing sum and carry outputs.

3. The transmission-gates CMOS (TG-CMOS) based full adder [15] circuit has 20 transistors.

4. The low power implementation of the full adder cell which has 14 transistors (14T) [16]. This cell is based on transmission gates and the low power XOR design.

5. The transmission function full-adder (TFA) cell [17] is based on the transmission function theory and it has 16 transistors.

Though these full adders are performing the same function, but their style of design is different from each other i.e. the loads on the inputs and intermediate nodes are different, and the transistor count varies significantly.

The conventional CMOS full adder circuit has 28 transistors and is based on the regular CMOS structure composed of pull-up PMOS and pull-down NMOS networks. Every PMOS transistor has its gate connected to NMOS transistor to form a complementary pair. The advantage of conventional CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operations at low voltages and arbitrary transistor sizes. Moreover, the layout of CMOS circuit is straightforward and area-efficient due to the complementary transistor pairs and smaller number of interconnecting wires. But it has more number of transistors to implement the full adder that causes large chip area and large input capacitance but could not provide high speed operation.

The CPL uses pass-transistors to select between possible inverted output values of the logic, the output of which drives an inverter to generate the non-inverted output signal. Its dual rail structure uses 32 transistors. The basic difference between the pass-transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines. The advantage is that one pass-transistor network (either PMOS or NMOS) is sufficient to implement the logic function which results in smaller number of transistors and smaller input load. However, pass-transistor logic has an inherent threshold voltage drop problem. The output is a weak logic "1" when "1" is passed through a NMOS and is a weak logic "0" when "0" is passed through a PMOS. Therefore, output inverters are also used to ensure the drivability. The CPL logic style is a high speed and full swing design, but due to the presence of a lot of internal nodes and static inverters, there is a large amount of power dissipation.

Transmission gate full adder (TG-CMOS) is introduced for its low power dissipation but it lacks driving capability. Transmission gate logic circuit is a special kind of pass-transistor logic circuit; it is built by connecting one PMOS transistor and one NMOS transistor in parallel, which are controlled by complementary control signals. Both the PMOS and NMOS transistors would provide the path to the input logic "1" or "0," respectively, while they are turned on simultaneously. Thus, there will be no voltage drop problem whether the 1 or the 0 is passed through it. The main disadvantage of transmission gate logic is that it requires double the number of transistors of the standard pass-transistor logic or more to implement the same circuit.

A transmission function full adder (TFA) generate $A \oplus B$ and use it and its complement as a select signal to generate the outputs; while CMOS generates C_{out} through a single static CMOS gate and finally CPL generates many intermediate nodes and their complement in order to generate the final outputs. The problem in these designs is overloading of inputs (especially with oversized transistor gates), produces high capacitance values for these nodes. This problem is appropriate with CPL and CMOS, and not exactly with TG-CMOS, TFA, and 14T. The speed of the 14T adder decreases substantially with supply voltage scaling than the other full adders. This is due to voltage drop problem and lack of level restoration problem. Moreover, the 14T cell has shown negative results at low voltage. Another problem that is unique in CMOS is that it generates the sum using the C_{out} signal as an input, which produces an unwarranted additional delay.

The full adders TG-CMOS, TFA and 14T have an added advantage of lower transistor count, intermediate nodes and provide better performance than CMOS and CPL designs. The above logics show good behavior when implementing with a 1-bit full adder cell but they may end up with low level performance when used to implement more complex structures. The proposed full adders reduce some of the problems such as driving capability, delay, threshold voltage drop and layout complexity etc.

In this paper, we have brought to light two modified level restorers using current sink inverter and current source inverter structures (within the circle shown in Fig. 1 and 2) for BBL-PT full adder [1]. The proposed circuits eliminate the voltage step in the existing full adder and have good delay performance i.e. high operating speed.

The remaining section of the paper is organized as follows. In Section 2, we proposed full adder's structure implementations and Section 3 explains simulation results. The implementation of an 8-bit RCA based on the proposed full adder is described in Section 4 and finally in Section 5 ended up with conclusion.

2. Proposed Full Adder Implementation

A Full Adder (FA) cell is a three-input and two-output block in which the outputs are obviously the addition of three inputs. This has three 1-bit inputs (A, B, and C) and two 1-bit outputs (sum and carry). The relations between the inputs and the outputs are expressed as

$$Sum = ABC_{in} + \overline{A}\overline{B}C_{in} + \overline{A}B\overline{C_{in}} + A\overline{B}\overline{C_{in}} \ , \qquad (1)$$

$$Carry = AB + BC_{in} + AC_{in} \ . \qquad (2)$$

For the low power design, a cell schematic must be implemented with few transistors and intra-cell node connections as far as possible. The branch-based design technique meets these requirements while ensuring robustness with respect to voltage and device scaling. Here, logic cells are designed exclusively with branches composed of transistors connected in series between a supply line and the gate output. The advantages of transistor branches are higher layout regularity and simpler characterization (i.e., branch instead of gate modeling) [18]. Branch based design is having the advantage of no diffusion interruption, common drain for two branches, a minimal number of contacts and few metal connections. This branch-based technique is first introduced to reduce parasitic capacitances for achieving low power and is also beneficial for high-speed logic such as fast adders in SOI technology [19].

The disadvantage of BBL-PT full adder implementation lies in the discharge of weak high output level in pass transistors used in the sum block that can be realized by the feedback pull-up PMOS transistor. In order to restore the weak logic "1" (i.e. $V_{dd} \cdot V_{tn}$) caused by the pass transistors, it has provided sufficient drive to the successive stages. However, the level restoration implemented this way causes a voltage step at the output node "S_{out}" during a $0 \rightarrow 1$ transition. This voltage step is due to the threshold voltage drop in the pass transistors and the delay needed by the level restorer to restore the weak logic "1" level. If the voltage step exists, the ON time period (t_{ON}) and OFF time period will not be equal. To make it equal we proposed two level restorers using current sink and current source inverter structures.

2.1 1-Bit FA Based on Current Sink Inverter

The current sink inverter structure (within the circle shown in Fig. 1) in which current sink load is used. The current sink is a common gate configuration using an N-channel transistor with gate connected to a fixed bias supply; on account of this, the N-transistor is always in ON condition; while the P-transistor serves as a pull-up network. This inverter achieves higher voltage gain than active load inverters.

The carry can be implemented [1] with branch structure, using the simplification method given [18] as shown in Fig. 1(b). In branch-based design, the networks are composed only of branches, i.e., series connections of transistors between the output node and the supply rail. The carry circuit is the same for the both the proposed full adders. The NMOS and PMOS networks are represented as sum of products and are obtained from Karnaugh maps. The equations for the NMOS and PMOS are given by

$$C_P = C_N = \overline{A}\,\overline{C}_{in} + \overline{B}\,\overline{C}_{in} + \overline{A}\,\overline{B}. \qquad (3)$$

In order to prevent the voltage step that appears in $0 \rightarrow 1$ transition on the sum output signal [1], we proposed current sink inverter based full adder sum circuit as shown in Fig. 1 (a).

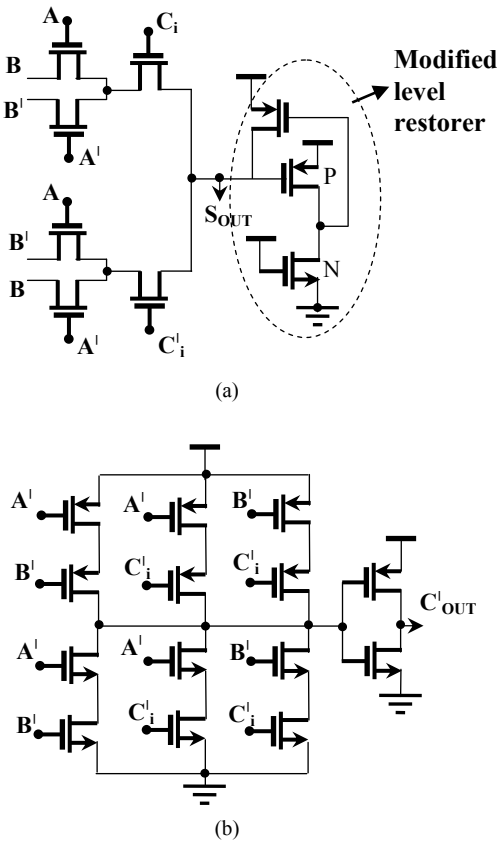

Fig. 1. Proposed full adder circuit with current sink inverter structure (within the dashed circle).

In Fig. 1 (a) NMOS transistors are used to implement the full adder sum circuit. In general, NMOS transistors have stronger 0's & weaker 1's, when input is applied. When logic "1" is applied to the input of NMOS network, it is passed through the NMOS network and the node "S_{out}" is to be charged to a weak logic "1". When the voltage at node "S_{out}" is < $V_{dd}/2$, the P-transistor in the current sink inverter reaches switching threshold and turned ON. The resultant output of inverter is logic "1". This logic "1" is input to the pull-up PMOS and the pull-up PMOS is turned OFF. The node "S_{out}" is charged with an effective drive current that equals the current of the NMOS network.

When the voltage at node "S_{out}" reaches to $V_{dd}/2$, the PMOS transistor in the current sink inverter is turned OFF. Then, the P-transistor is turned OFF while the N-transistor is always kept in ON condition irrespective of input, thus it reduces the delay during the $0 \rightarrow 1$ transition. Finally, the output of the current sink inverter is logic "0", it is applied to the input of pull-up PMOS. Then, the pull-up PMOS is turned ON and the effective drive current charging the capacitance at node "S_{out}" becomes the sum of the current flowing through the NMOS network and the pull-up PMOS currents.

2.2 1-Bit FA Based on Current Source Inverter

The current source inverter structure (within the circle shown in Fig. 2) in which current source load is used. The current source is a common gate configuration using a p-channel transistor with gate connected to a fixed bias supply; due to this the P-transistor is always in ON condition; while the N-transistor serves as a pull-down network. This inverter achieves higher voltage gain than active load inverters.

In order to prevent the voltage step that appears in $0 \rightarrow 1$ transition on the sum output signal [1], we proposed another current source inverter based full adder sum circuit as shown in Fig. 2. And the carry circuit is shown in Fig. 1(b).

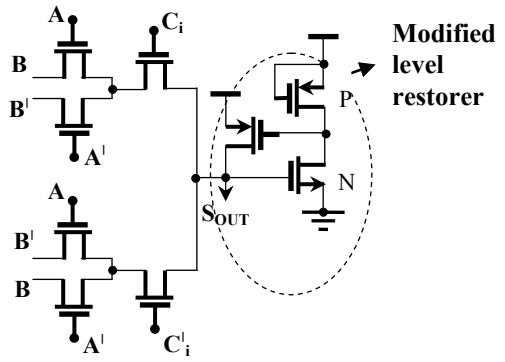

Fig. 2. Proposed full adder sum circuit with current source inverter (within the dashed circle).

When logic "1" is applied to the input of NMOS network then the logic "1" is passed through the NMOS network, the node "S_{out}" is to be charged to a weak logic "1". When the voltage at node "S_{out}" is $< V_{dd}/2$, the N- transistor in the current source inverter is turned OFF the P-transistor is always in ON condition irrespective of the applied input; then the output of inverter is logic "1". The output of the inverter is logic "1", it is applied to the input of pull-up PMOS, then the pull-up PMOS is turned OFF, and the node "S_{out}" is charged with an effective drive current that equals the current of the NMOS network.

When the voltage at node "S_{out}" reached $V_{dd}/2$, the N-transistor in the current source inverter also reaches switching threshold, and turned ON, i.e. the voltage at node "S_{out}" reaches $V_{dd}/2$ i.e. logic 1 is the input to the current source inverter. When, the N-transistor is turned ON the P-transistor is always left in ON condition irrespective of the input, thus it reduces the delay during the $0 \rightarrow 1$ transition. Finally, the output of the current source inverter is logic "0", it is applied to the input of pull-up PMOS. Then, the pull-up PMOS is turned ON, and the effective drive current charging the capacitance at node "S_{out}" becomes the sum of the current flowing through the NMOS network and the pull-up PMOS current.

The modified level restorer with current sink inverter, current source inverter structures and pull-up PMOS transistor within the circle is shown in Fig.1 (a) and 2. The pull-up PMOS transistor, must have a high ON resistance in order to restore the high logic level without affecting the low logic level at the output node i.e. node S_{out}.

2.3 Transistor Sizes

In order to increase the switching speed, and thus to reduce the delay times, would be to increase the W/L ratios of all transistors in the circuit. However, increase in the transistor W/L ratios also increases the gate, source and drain areas that results into subsequent increase in the parasitic capacitances of loading the logic gates [12]. Hence, the resizing of transistors is an iterative process to improve the performance of the full adder cell. All the transistor sizes (in μm) for the proposed full adder and conventional full adders (CMOS and CPL) are given by

$W = 0.4$ μm and $L = 0.13$ μm for PMOS,
$W = 0.2$ μm and $L = 0.13$ μm for NMOS.

The pull-up PMOS transistor in the proposed level-restorers, considered minimum W/L ratios i.e. $W = 0.18$ μm and $L = 0.18$ μm. For this purpose the SPICE level 3 model of MOS transistors with $V_{tn} \cong 0.5$ V and $V_{tp} \cong -0.6$ V were used. The pull-up PMOS transistor, which must have high ON resistance, in order to restore the high logic level without affecting the low logic levels at the output node "S_{out}".

2.4 Static Power in the BBL-PT

R. X. Gu and M. I. Elmasry have introduced in [20] an analytical model of the leakage current for a series of stacked transistors. This analytical model has shown that the leakage current decreases with the number of transistors in the stack, i.e., the comparison of the current in the cases of one transistor (I_{S1}), two stacked transistors (I_{S2}), and three stacked transistors (I_{S3}), gives $I_{S3} < I_{S2} < I_{S1}$ respectively. The stack effect thus contributes to static power reduction. The leakage current becomes negligible when the number of stacked devices is more than three [20], whereas the leakage current for transistors in parallel equals the sum of currents through each transistor. Branch-based design, for which the number of stacked transistors per branch is > 2, exploits the stack effect and helps to reduce leakage power. The proposed circuit is designed with combination of two logic styles and offers high speed, low static power consumption and low count of transistors. Lowering the supply voltage appears to be well known means to reduce the power consumption. However, lowering the supply voltage also increases the circuit delay and degrades the system performance.

3. Simulation Results

The proposed full adders and the other conventional adders (CMOS, CPL and BBL-PT) are simulated using the

PSPICE and the model parameters of a 0.13 µm CMOS process. The simulations were carried out with supply voltage V_{dd} = 1.2 V and frequency of 100 MHz. A comparison with existing or already reported designs is included which shows the advantage of the proposed designs, good delay performance and the results are shown in Tab. I.

Serial Number	Design	Delay (ps)	Transistor count
1.	CMOS Full Adder	124	28
2.	CPL Full Adder	91	32
3.	BBL-PT Full Adder	110	23
4.	Proposed Current Sink Inverter Full Adder	85	23
5.	Proposed Current Source Inverter Full Adder	83	23

Tab. 1. Performance comparisons of the proposed and alternative implementations of one-bit full adder cell with V_{dd} = 1.2 V and f = 100 MHz.

For each transition, the delay is measured from 50% of the input voltage swing to 50% of the output voltage swing. The maximum delay is taken as the cell delay. It is apparent that amongst the existing conventional full adders, the proposed ones are having lower delays as shown in Tab. 1.

While optimizing the transistor sizes of full adders are considered, it is possible to reduce the delay of all adders without significantly increasing the power consumption. The branch-based logic, in combination with pass-transistor logic, allows a simple implementation of the full-adder gate, namely, the BBL-PT full adder, with only 23 transistors. This compares favorably with the 28-transistor static CMOS full adder and the 32-transistor CPL full adder (CPL FA). The proposed full adder occupies the minimum silicon area on the chip among the ones (except BBL-PT FA) reported in this paper. The small silicon area of the proposed full adder makes it potentially useful for building compact VLSI circuits on a small area of a chip.

The simulated input and output waveforms of the existing (BBL-PT) ones are shown in Fig. 3 and the proposed full adders for sum and carry are shown in Fig. 4 and 5. In the BBL-PT full adder, there exist a voltage step in the SUM output waveform during $0 \rightarrow 1$ transition as shown in Fig. 3 and the same can be eliminated in the proposed full adder designs using current sink inverter shown in Fig. 4 and current source inverter as shown in Fig. 5. The voltage step in BBL-PT is due to the delay needed by the level restorer to restore the weak logic "1" level. The proposed level restorers don't require delay to restore the weak logic "1" level. In Fig. 5, the inputs (A, B & C) applied for all possible combinations i.e. 000 to 111.

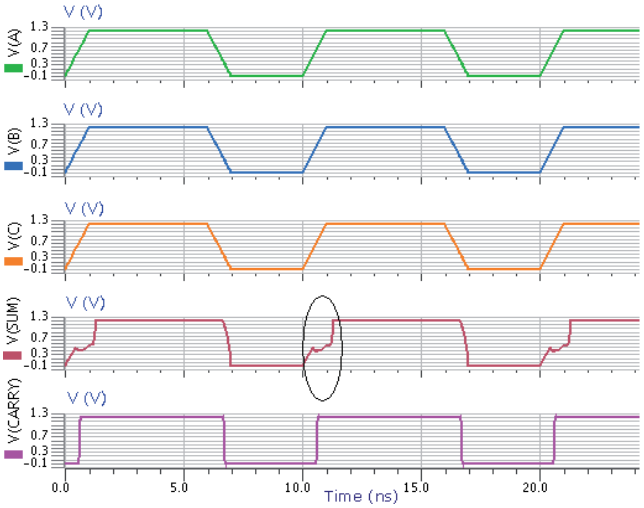

Fig. 3. The BBL-PT full adder output waveforms.

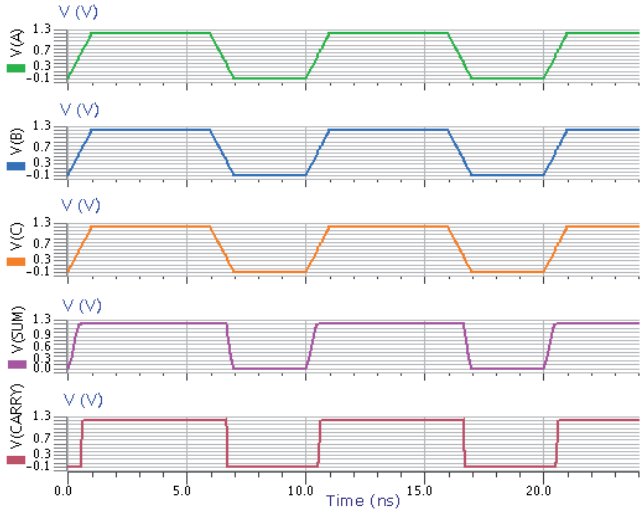

Fig. 4. Simulated input & output waveforms of the proposed adder using current sink inverter.

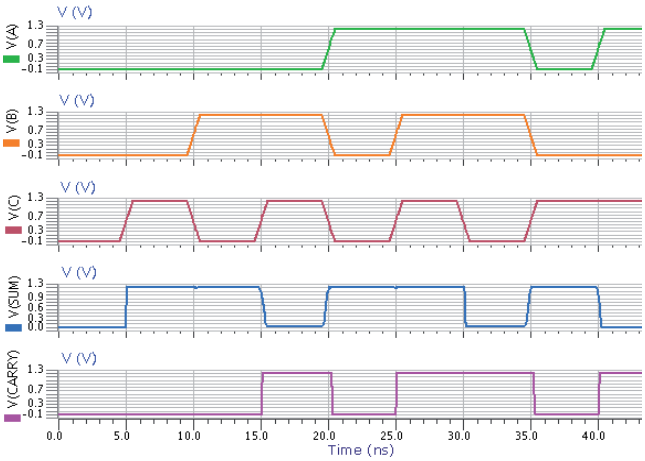

Fig. 5. Simulated input & output waveforms of the proposed adder using current source inverter.

4. 8-BIT RCA Implementation

We have selected 8-bit RCA as a benchmark implementation to fairly compare five 1-bit full adders. The full adder circuits designed in this paper can now be used as the basic building block of an 8-bit ripple carry adder, which accepts two 8-bit binary numbers as input and produces the binary sum and carry at the output. The simplest such adder can be constructed by a cascade-connection of eight full adders, where as each adder stage performs a two-bit addition, produces the corresponding sum bit, and passes the carry output on to the next stage. Hence, this cascade-connected adder configuration is called the ripple carry adder as shown in Fig. 6. The overall speed of the ripple carry adder is obviously limited by the delay of the carry bits rippling through the carry chain. Therefore, a fast carry-out response is essentially required for the overall performance of the adder chain.

The proposed adders and CPL 8-bit ripple carry adders having lower delay when increasing the supply voltage and results are plotted in Fig.7. Simulated delay results are summarized in Tab. 2.

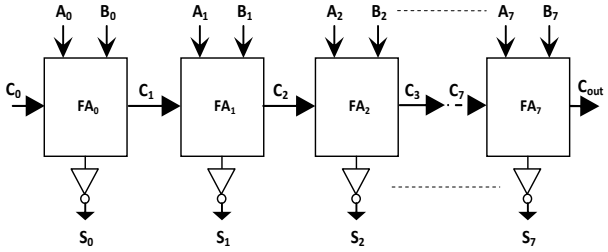

Fig. 6. Proposed 8-bit RCA based modified level restorer full adder cell.

S.No	Design	Delay (ps)	Transistor count
1.	CMOS Full Adder	833	224
2.	CPL Full Adder	514	256
3.	BBL-PT Full Adder	845	184
4.	Proposed Current Sink Inverter Full Adder	514	184
5.	Proposed Current Source Inverter Full Adder	520	184

Tab. 2. Performance comparison of the proposed and alternative implementations of 8-bit RCA with V_{dd} = 1.2 V and f = 100 MHz.

It can thus be seen that the first proposed current sink inverter based 8-bit RCAs and CPL 8-bit RCA [1] shows the best delay performance than CMOS and BBL-PT based 8-bit RCAs. The results are enunciated in Fig. 8.

And also, it can be seen that the second proposed current source inverter based 8-bit RCA and CPL 8-bit RCA [1] shows the best delay performance than CMOS and BBL-PT based 8-bit RCAs. These results are plotted as shown in Fig. 9.

Since, both the proposed circuits having good driving capability are achieved through the level restoration circuit

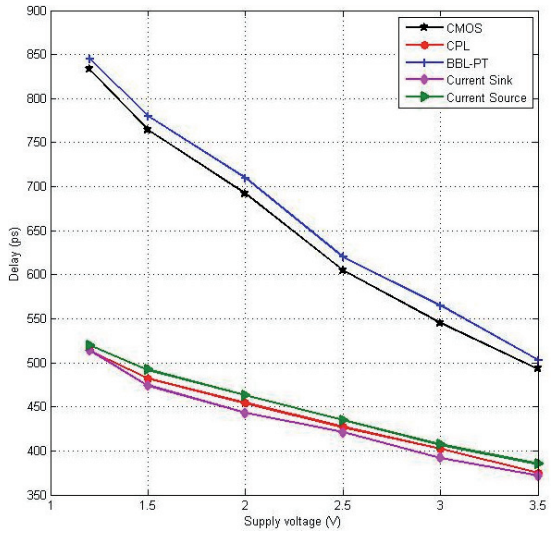

Fig.7. Delay vs. Supply voltage comparison of 8-bit ripple carry adders.

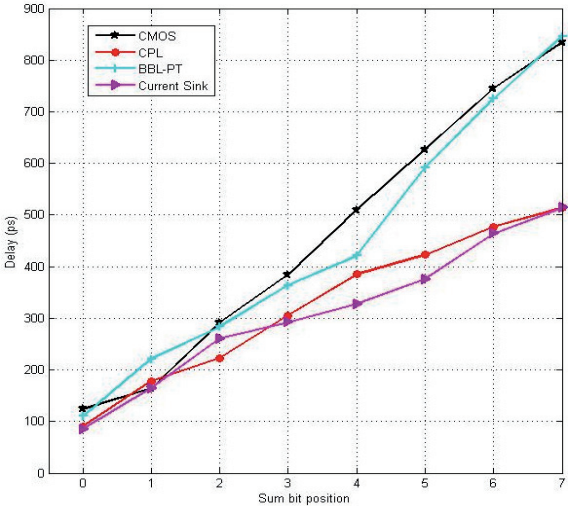

Fig. 8. Delay vs. Sum bit position comparison for the proposed current sink and other 8-bit ripple carry adders.

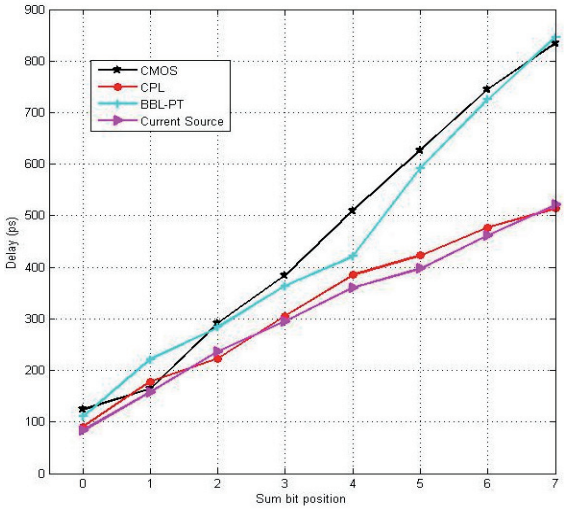

Fig. 9. Delay vs. Sum bit position comparison for the proposed current source and other 8-bit ripple carry adders.

using current sink & current source inverter structures. And also, the CPL 8-bit RCA has good driving capability. But, CPL based FA has high transistor count and it consumes more power. The BBL-PT 8-bit RCA shows a higher delay than the CPL 8-bit RCA which in turn exhibits slightly higher delay than the CMOS 8-bit RCA.

The proposed designs i.e. current sink & current source inverter based full adders having the best delay in comparison with the other designs and the results are plotted as shown in Fig. 10. Among all the full adder circuits, current sink inverter based full adder has good delay performance.

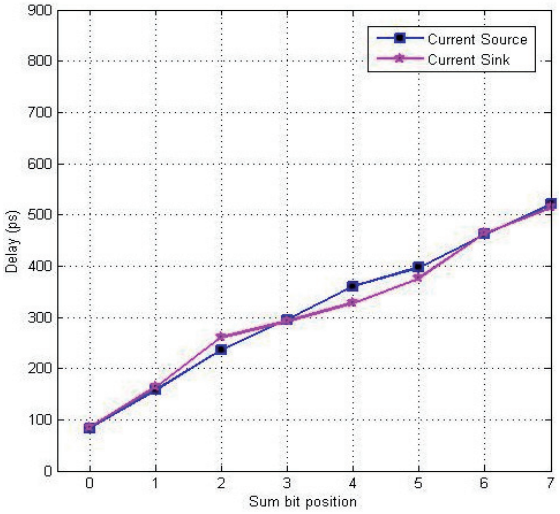

Fig. 10. Delay vs. Sum bit position comparison for the proposed 8-bit ripple carry adders.

5. Conclusion

In this paper, we have focused on two modified level restorers using current sink inverter and current source inverter structures for BBL-PT full adder. These circuits provide regular and compact layout structures that reduce the diffusion capacitances (since it eases diffusion sharing). The proposed level restorers are to eliminate the voltage step in the existing full adder design and to achieve good delay performance. Nextly, the 8-bit RCA circuits based on the proposed ones achieve 40% lower delay than the static CMOS and BBL-PT full adders. Comparison of both the proposed ones, current sink inverter based full adder is graded high. Finally, while implementing high performance complex structures, such as multipliers, ALU (arithmetic logic unit), counters and mobile communications, the intrinsic benefits of proposed ones could be fully exploited.

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