High Current Matching over Full-Swing and Low-Glitch Charge Pump Circuit for PLLs

De-zhi WANG, Ke-feng ZHANG, Xue-cheng ZOU

School of Optical and Electronic Information, Huazhong University of Science and Technology Wuhan, P.R. China

dzjcwang@gmail.com, kfzhan@gmail.com, extxczou@gmail.com

Abstract. *A high current matching over full-swing and low-glitch charge pump (CP) circuit is proposed. The current of the CP is split into two identical branches having one-half the original current. The two branches are connected in source-coupled structure, and a two-stage amplifier is used to regulate the common-source voltage for the minimum current mismatch. The proposed CP is designed in TSMC 0.18μm CMOS technology with a power supply of 1.8 V. SpectreRF based simulation results show the mismatch between the current source and the current sink is less than 0.1% while the current is 40 μA and output swing is 1.32 V ranging from 0.2 V to 1.52 V. Moreover, the transient output current presents nearly no glitches. The simulation results verify the usage of the CP in PLLs with the maximum tuning range from the voltage-controlled oscillator, as well as the low power supply applications.*

Keywords

Charge pump, two current branches, source-coupled, voltage regulate, low-glitch, full-swing.

1. Introduction

The charge pump (CP) based phase-locked loop (PLL) shown in Fig. 1 includes a phase frequency detector (PFD), a CP, a low pass filter (LPF), a voltage controlled oscillator (VCO), and a divider (DIV) [1]. The PFD detects phase error between reference clock f_{REF} and feedback clock f_{DIV}. The CP converts the detection errors *UP* (*DN*) into current I_{CP} to charge (discharge) the LPF until a target frequency f_{VCO}. Then, tuning voltage V_{tune} keeps constant and the phase error is close to zero, which means the loop in lock.

One of the most important design issues of the CP-PLL is spurious tones dominated by non-idealities of the CP including static current mismatch and dynamic glitches. Static current mismatch could be improved by increasing output resistance of the CP [2] or by using replica biasing technique [3]-[4]. However, dynamic glitches are difficult to be fully removed since they are created by time-varying effects such as charge sharing. Several works tried to reduce dynamic glitches as far as possible [5]-[9]. A differential CP circuit proposed in [5] needs four voltage buffers and large capacitors, which unavoidably consumes large area and power, and so do the CPs in [6] and [7]. A technique proposed in [8] eliminates dynamic glitches at the price of decreasing operational frequency of the CP. Though a very simple and effective CP circuit is suggested in [9], output resistance of the CP may be not enough so that static current mismatch is deteriorated when output swing of the CP comes to full swing. Based on the disadvantages, a high current matching over full swing and low-glitch CP circuit is proposed. This paper is organized as follows. In Section 2, non-idealities of the CP upon spurious tones are analyzed. The proposed CP circuit is introduced in Section 3. In Section 4, simulation results are presented. Finally, this work is concluded in Section 5.

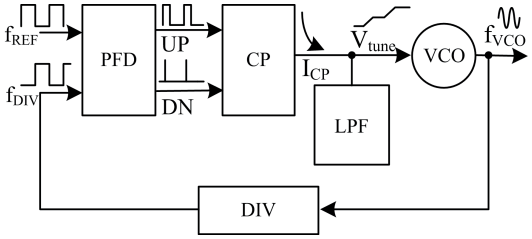

Fig. 1. The common structure of CP based PLL.

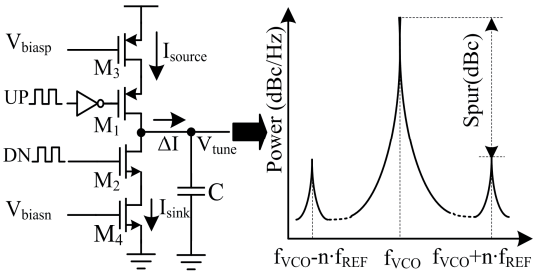

Fig. 2. Non-idealities of CP upon spurious tones.

2. Non-idealities of the CP

A standard CP and its non-idealities upon spurious tones are shown in Fig. 2 with the assumption that the LPF is substituted by a capacitor C. Transistors M_1, M_2 act as switches controlled by *UP* and *DN* respectively, and M_3 and M_4 act as current source of I_{source} and current sink of I_{sink} biased by V_{biasp} and V_{biasn}. When the CP-PLL is in lock,

UP and *DN* present short pulses with a width of τ_{delay} and a period of τ_{REF} used to remove dead-zone of the PFD [10]. Then, static current mismatch and dynamic glitches cause an output current of ΔI to inject into capacitor C, and hence result in output spectrum of the PLL presenting spurious tones at $\pm n \cdot f_{REF}$, where n is positive integer.

2.1 Static Current Mismatch

Assuming current source of I_{source} is smaller than current sink of I_{sink} with a mismatch of I_{mis}, and the average current of the CP is I_{CP}. Then

$$I_{mis} = \left(I_{sink} - I_{source}\right), \qquad I_{sink} \approx I_{source} = I_{CP} . \tag{1}$$

When CP-PLL is in lock, average value of the V_{tune} would keep constant. Thus the average charge injecting into the C is zero, which leads to a timing mismatch of τ_{mis} between the *UP* and the *DN*. As shown in Fig. 3, the τ_{mis} should meet

$$\tau_{mis} \cdot I_{CP} = I_{mis} \cdot (\tau_{delay} - \tau_{mis}) . \tag{2}$$

As the I_{mis} is very small (e.g., 0.4%), the τ_{mis} is ignorable compared with the τ_{delay}. Then, the value of the τ_{mis} is

$$\tau_{mis} \approx I_{mis} \cdot \tau_{delay} / I_{CP} . \tag{3}$$

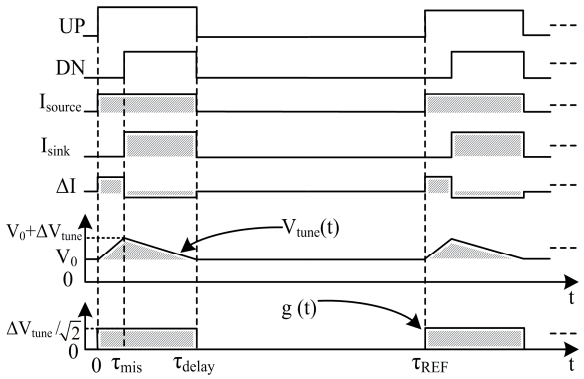

Fig. 3. Static current mismatch upon tuning voltage.

Therefore, the V_{tune} suffers ripples in a period of τ_{REF}. For instance, from 0 to τ_{mis}, the ΔI equaling I_{source} charges the C which causes the V_{tune} to rise from the stable value V_0, and to reach its peak $V_0 + \Delta V_{tune}$ at the time τ_{mis}. Then the ΔI equaling the I_{mis} discharges the C from τ_{mis} to τ_{delay}, which result in the V_{tune} decreasing to the stable value V_0 again at the time τ_{delay}. The periodical ripples of the V_{tune} would directly modulate the oscillation frequency of a VCO.

In s-domain, when a step current of $I_{CP} \cdot u(t)$ injects into the C, the V_{tune} would be

$$V_{tune}(s) = \frac{I_{CP}}{s} \cdot \frac{1}{s \cdot C} . \tag{4}$$

The initial value of the V_{tune} is $V_{tune}(0) = V_0$. By use of inverse Laplace transforms, the peak value of the V_{tune} is

$$V_{tune,peak} = V_{tune}(\tau_{mis}) = \frac{I_{CP}}{C} \cdot \tau_{mis} + V_0 . \tag{5}$$

According to (3) and (5), the magnitude of the ripples ΔV_{tune} is

$$\Delta V_{tune} = V_{tune,peak} - V_{tune}(0) = \frac{I_{CP}}{C} \cdot \tau_{mis} = \frac{I_{mis} \cdot \tau_{delay}}{C} . \tag{6}$$

The τ_{delay} is so small that the ripples could be regarded as a pulse function of $g(t)$ having average amplitude: $\Delta V_{tune}/\sqrt{2}$ from $(n - 1) \cdot \tau_{REF}$ to $(n - 1) \cdot \tau_{REF} + \tau_{delay}$. The DC and the fundamental component of the $g(t)$ are calculated as

$$g_{DC} = \frac{1}{\tau_{REF}} \cdot \int_0^{\tau_{REF}} g(t) \cdot dt = \frac{I_{mis} \cdot \tau_{delay}^2}{\sqrt{2} \cdot C \cdot \tau_{REF}} , \tag{7}$$

$$g_{\tau_{REF}} = \frac{\sqrt{2} \cdot I_{mis} \cdot \tau_{delay}^2}{C \cdot \tau_{REF}} \cos \omega_{REF} \cdot t \cdot \tag{8}$$

Thus, the output of the VCO could be approximated as

$$V_{VCO}(t) = A \cos\left[2\pi K_{VCO}(V_0 + g_{DC})t + 2\pi K_{VCO} g_{\tau_{REF}} t\right] \tag{9}$$

where A is the amplitude of the output of the VCO. According to (9), the frequency offset Δf_{VCO} and the spurious tones at $(f_{VCO} + \Delta f_{VCO}) \pm f_{REF}$ are

$$\Delta f_{VCO} = \frac{K_{VCO} I_{mis} \cdot \tau_{delay}^2}{\sqrt{2} \cdot C \cdot \tau_{REF}} , \tag{10}$$

$$Spur[(f_{VC0} + \Delta f_{VC0}) \pm f_{REF}] = 20 \cdot \log \frac{\sqrt{2}\pi \cdot I_{mis} \cdot \tau_{delay}^2 K_{VCO}}{C \cdot \tau_{REF}} \tag{11}$$

and, spurious tones at $\pm n \cdot f_{REF}$ could be obtained by calculating the n^{th} harmonic component of the $g(t)$ [11].

Based on the discussions, the spur level of the CP-PLL is proportional to the I_{mis}. Low level of the spur makes the design of the CP challengeable, especially when the output voltage of the CP comes to full-swing. Moreover, the I_{mis} could affect the oscillation frequency of a VCO, which leads to the phase noise being deteriorated. Besides, low value of the τ_{delay} is preferred for low spur level. However, as the affection of the dynamic glitches, low value of the τ_{delay} may affect the stability of the CP-PLLs.

2.2 Dynamic Glitches

Ideal output current of the CP during phase lock is shown in Fig. 4(a) when static mismatch is considered. In fact, the ΔI undergoes glitches at the moment when the M_1 (M_2) is switched on or off, as is shown in Fig. 4(b). The dynamic glitches could decrease current matching of the CP. Besides, the τ_{delay} is so small that the dynamic glitches may increase the gain of the CP and hence result in the CP-PLL unstable [12]. There are two mechanisms that cause the ΔI to present glitches. The first is the charge injection from the charge stored in the channels of M_1 and M_2, and the second is charge sharing from nodes A_1 and A_2 when M_1 and M_2 is switched on or off. At the moment 0, the *UP* is changed to high logic, and hence M_1 is turned on. A downward current glitch of $I_{glitch1}$ is firstly generated by

charge being pulled off from the node B, namely, from the drain to the gate of M_1, in order to form the inversion layer. Assuming the amount of the charge is Q_1, the gate-drain capacitor and voltage of M_1 are $C_{GD,M1}$ and $V_{GD,M1}$. Then

$$I_{glitch1} = dQ_1/dt = C_{GD,M_1} \cdot dV_{GD,M_1}/dt . \quad (12)$$

As the capacitor at the node B is very larger than that at the drain of M_1, the $dV_{D,M1}/dt$ could be ignored compared with the $dV_{G,M1}/dt$. Thus, equation (12) is approximated as

$$I_{glitch1} = C_{GD,M_1} \cdot dV_{G,M_1}/dt . \quad (13)$$

Since the $dV_{G,M1}/dt$ is large at the rising edge of the *UP*, the $I_{glitch1}$ is large. Then, an upward glitch follows the $I_{glitch1}$ caused by charge sharing. Before the time 0, M_1 is off and $V_{A1} \approx V_{DD}$. Once the M_1 is on, V_{A1} is pulled down to V_B. Thus, charge sharing occurs and the glitch is proportional to dV_{A1}/dt. Assuming the gate-source capacitor of the M_1 and the capacitor at the node A_1 are $C_{GS,M1}$ and C_{A1}. Then

$$dV_{A1}/dt = \left(dV_{G,M_1}/dt\right) \cdot C_{GS,M_1} \Big/ \left(C_{GS,M_1} + C_{A1}\right). \quad (14)$$

This glitch is large as $C_{GS,M1}$ nearly equals $C_{GD,M1}$. Dynamic glitches at the other moments are the same as the moment 0.

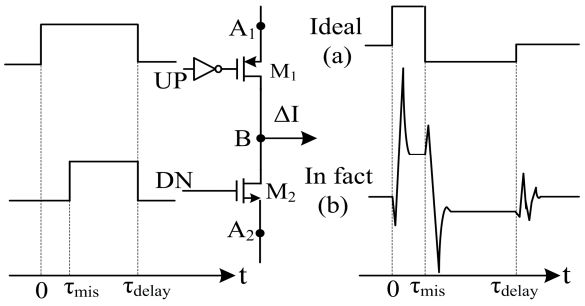

Fig. 4. Qualitative description of dynamic current glitches.

Giving the voltage variation caused by the dynamic glitches is ΔV. Then, equation (6) could be rewritten as

$$\Delta V_{tune} = \frac{I_{mis} \cdot \tau_{delay}}{C} + \Delta V = K \cdot \tau_{delay} + \Delta V \quad (15)$$

where K is the gain of the CP without the dynamic glitches. Then, the gain K_e considering the dynamic glitches is

$$K_e = \Delta V_{tune}/\tau_{delay} = K + \Delta V/\tau_{delay} . \quad (16)$$

Equation (16) indicates the K_e caused by dynamic glitches could be very large with a small value of the τ_{delay}. As loop bandwidth is proportional to the gain of the CP, the stability of the CP-PLL may be broken.

In summary, non-idealities of the CP are discussed in this section. The spur level is proportional to I_{mis}, τ_{delay}, and dynamics glitches. Dynamic glitches caused by switching actions are proportional to voltage derivation at the gate of the M_1 (M_2) during rising (falling) edge. Moreover, the glitches in CP could result in the CP-PLL unstable. All of these above discussed demonstrate the significance of a CP with high current matching and low-glitch characteristics.

3. Proposed Charge Pump Circuit

An existing CP circuit proposed in [9] could improve the dynamic glitches by using resistors, which is simply presented in Fig. 5(a) and explained by combining with the proposed CP circuit in this section. However, as the current matching is proportionally to the output resistor of the CP as shown in Fig. 5(b), the static current mismatch of this CP may be serious when the output voltage comes to the rails since the output resistor is even lower than a classical cascade structure. For instance, when *UPb*=0 and *DN*=0

$$R_{OUT} = R_{M4} + R_{IB} \left\| \left(R + R_{IB}\right) \right. . \quad (17)$$

As the R_{M4} and the R is ignorable compared with R_{IB}. then,

$$R_{OUT} \approx R_{IB}/2 . \quad (18)$$

R_{IB} is the resistor of the I_B, which is realized by cascade current mirror. The contribution of this study is to widen the output swing of this CP circuit to full swing.

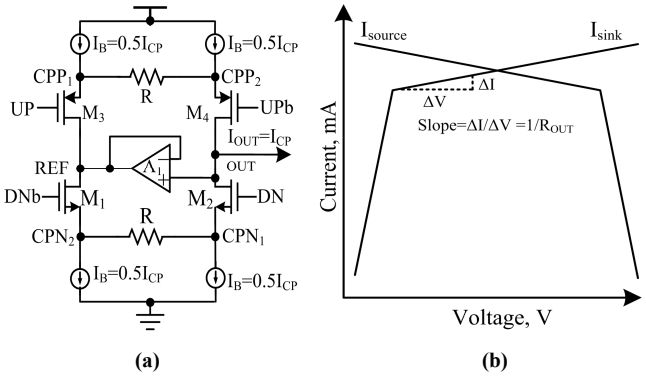

Fig. 5. The existing low glitch CP **(a)** circuit, and **(b)** static current mismatch.

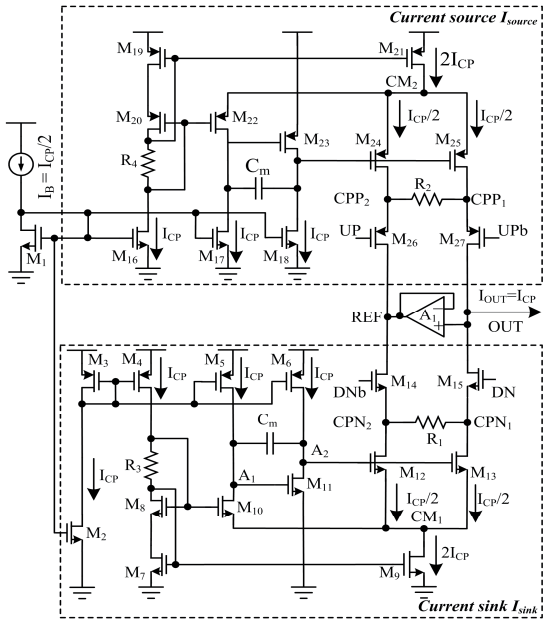

Fig. 6. The proposed high current matching and low-glitch CP circuit.

The complete circuit diagram of the proposed CP is shown in Fig. 6, which is driven by a differential PFD with complementary outputs of *UP* (*UPb*) and *DN* (*DNb*). We describe the principle of the current sink I_{sink} only, and the principle of the current source I_{source} is the same as the I_{sink}.

The reference bias current I_B equals $I_{CP}/2$. Transistor M_2 is two times the M_1, and $M_{4,5,6}$ are two times the M_3. Hence, mirror current in branches of $M_{2,4,5,6}$ is I_{CP}. As M_9 is two times the M_7, the current in branch of M_9 is $2 \cdot I_{CP}$. I_{sink} is split into two identical branches realized by $M_{12,13}$ connected in source-coupled structure, and each branch has a current of 0.5 I_{CP}. Thus, I_{sink} equals I_{CP} which flows out through the node OUT when I_{sink} conducts. A voltage buffer A_1 connected between the nodes OUT and REF is used to set V_{OUT} equaling V_{REF}, and a resistor R_1 is connected between the nodes CPN_1 and CPN_2. How the proposed CP circuit to solve the dynamic glitches and the static current mismatch is explained by

- Dynamic glitches suppression

When M_{14} is switched on, V_{CPN2} and V_{CPN1} are driven to $V_{REF} - V_{DS,M14}$ and $V_{REF} - V_{DS,M14} - 0.5\, I_{CP}R_1$ respectively. When M_{15} is switched on, V_{CPN1} is driven to $V_{OUT} - V_{DS,M15}$ while V_{CPN2} is dropped to $V_{OUT} - V_{DS,M15} - 0.5\, I_{CP}R_1$. Thus, $\Delta V_{CPN1} = V_{OUT} - V_{REF} - V_{DS,M15} + V_{DS,M14} + 0.5\, I_{CP}R_1$. As V_{OUT} equals V_{REF} by use of the voltage buffer A_1, and $V_{DS,M15}$ is well matched with $V_{DS,M14}$, ΔV_{CPN1} becomes $0.5\, I_{CP}R_1$ independent of the pulse signals of *DN* and *DNb*. So does ΔV_{CPN2}. Therefore, the affections of the dynamic sources such as charge sharing are suppressed.

- Static current mismatch reduction

A common-gate and common-source amplifier realized by M_{10} and M_{11} is used to regulate V_{CM1} for large output resistor R_{OUT}. Assuming the gain of the two-stage amplifier is A, then R_{OUT} of the CP is

$$R_{OUT} \approx A \cdot (2g_{M13}) \cdot r_{o13} \cdot r_{o9} = 2A \cdot \left(g_{M13} \cdot r_{o13} \cdot r_{o9}\right). \quad (19)$$

R_{OUT} based on (19) is increased by $2 \cdot A$ times than that of the cascade structure. Thus, the current mismatch is reduced. For instance, when V_{CM1} increases, I_{sink} would be larger than I_{CP}. However, the amplifier would decrease the gate voltage of both M_{12} and M_{13} to force down the V_{CM1}. By well-designing of the CP, the high current matching property over full-swing could be obtained as discussed as follows.

Two issues should be concerned in design of the CP circuit. In order to maximize the output swing, when no load connected to the node OUT, V_{CM1}, after running a DC simulation, should be set as low as possible while not drive M_9 to work in linear region. Then, V_{OUT} of a voltage source connected to the node OUT could be very low at the moment of I_{sink} decreasing. As is shown in Fig. 7, when the overdrive voltage V_{DR} of the M_9 is 0.12 V, V_{OUT} has the minimum voltage of 0.21 V when V_{CM1} is decreased from 0.3 V to 0.16 V, which means the CP has the maximum output swing. Fortunately, a low value of V_{CM1} is allowed since it is feedback to the source of the M_{10} rather than the gate as proposed in [2]. On the other hand, as a negative feedback loop is formed, stability of the CP should be cared. In I_{sink}, there are three high resistance nodes along the feedback path: the nodes CM_1, A_1 and A_2. The pole at CM_1 is high frequency pole, and the poles at A_1 and A_2 are dominant poles as the resistance at the node CM_1 is very smaller. A Miller capacitor C_m with value of 0.3 pF connected between A_1 and A_2 is used to realize pole splitting. Consequently, I_{sink} with only a dominant pole is stable. Transient curves of I_{sink} with and without C_m are shown in Fig. 8. I_{sink} without C_m presents ripples which are effective to the current glitches.

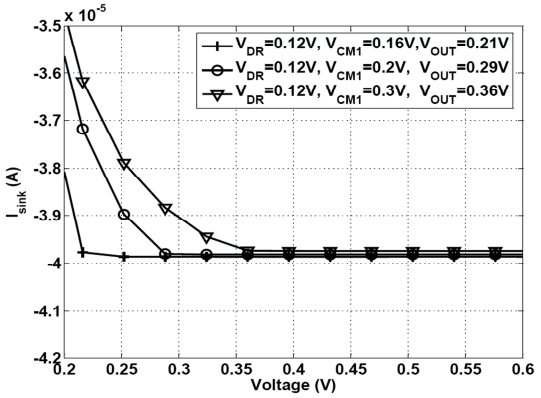

Fig. 7. The cross voltage of V_{OUT} when I_{sink} decreases.

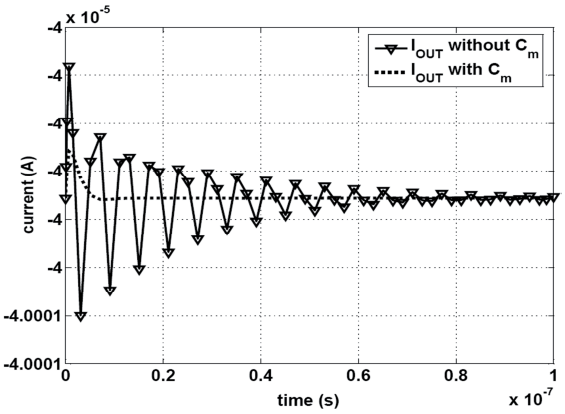

Fig. 8. Transient current sink I_{sink} with and without C_m.

Comp.	Sizes(μm)	Comp.	Sizes(μm)	Comp.	Sizes(μm)
M_1	2·4/4	M_{11}	10·4/1	M_{23}	64·4/1
$M_{2,16,17,18}$	4·4/4	$M_{12,13}$	2/1	$M_{24,25}$	4·2/1
$M_{3,4,5,6}$	30·4/1	$M_{14,15}$	2/0.18	$M_{26,27}$	2·2/0.18
M_7	5·2/1	M_{19}	16·4/1	$R_{1,2}$	1 (kΩ)
$M_{8,9,10}$	10·2/1	$M_{20,21,22}$	32·4/1	$R_{3,4}$	4 (kΩ)

Tab. 1. Sizes of components used in Fig. 6 (C_m = 0.3 pF, I_B = 20 μA).

4. Simulation Results

In this section, the CP shown in Fig. 6 is implemented in TSMC 0.18μm CMOS technology. Sizes of components used in Fig. 6 are shown in Tab. 1. The performances of the CP with 40μA output current are simulated and discussed by SpectreRF, which include the static current mismatch over full-swing, the transient output current, and the working principle during locking process.

- Static current mismatch

An ideal voltage source is connected at the node OUT. The UP and the DN are set to high logic. Then, the static current mismatch could be tested by simulating the current at the drains of M_{15} and M_{27} while V_{OUT} is changed from 0 to 1.8 V. The simulation results shown in Fig. 9 indicate the maximum current mismatch between I_{source} and I_{sink} is less than 40 nA when V_{OUT} ranges from 0.2 V to 1.52 V. Thus, the output swing of the CP could be as high as 1.32 V while the mismatch is within 0.1%.

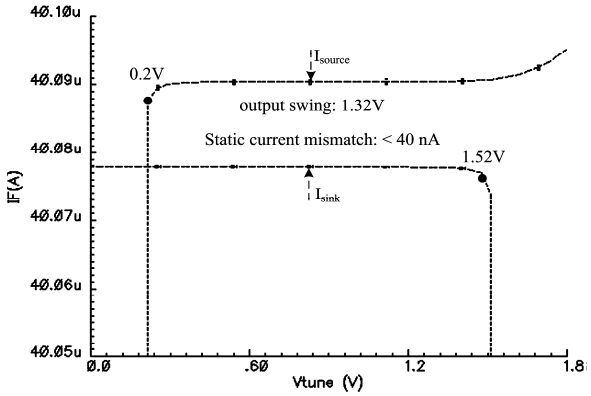

Fig. 9. SpectreRF simulated static current mismatch.

- Transient output current

We simulate the transient I_{sink} only and the case in the I_{source} is the same. The UP (*UPb*) is set to low (high) logic, and the DN (*DNb*) is with 2 ns pulse width in a frequency of 100 MHz. Besides, the rising time and the falling time of the DN (DNb) is 100 ps. Then, the transient I_{sink} is evaluated by simulating the current in the transistor M_{15}. The simulation results shown in Fig. 10 indicate that the transient current glitches are less than 20 μA, which is much less the existing CPs as highlighted in [7]. Moreover, the proposed CP circuit is with the switches at the drains of the current mirror transistors and the transient current is always conducted, which is steered from the left to the right based on the status of DN (DNb) [13], [14]. Thus, this structure gives faster switching time while it has low glitches in comparison with the works in [2], [3], [7].

- Simulated working principle

A load capacitor connected to the node OUT is used to simulate the function of the CP circuit, which has the initial voltage of 0.9 V and the value of 10 pF. Firstly, both the UP (UPb) and the DN (DNb) are set with the same pulse width 2 ns and the frequency of 100 MHz, the simulation result presented in Fig. 11 shows the voltage on capacitor holds on the level of initial voltage 0.9 V. While the UP (UPb) leads to the DN (DNb) 2 ns, the output current equaling I_{source} 40 μA charges the capacitor and leads to the voltage on the capacitor rising step by step. The maximum voltage is 1.756 V. On the other hand, while the UP (UPb) lags behind the DN (DNb) 2 ns, the output current equaling I_{sink} discharges through the capacitor. Hence, the voltage would decrease step by step and the minimum voltage is 50 mV. These simulation results verify the usage of the proposed CP circuit in PLLs.

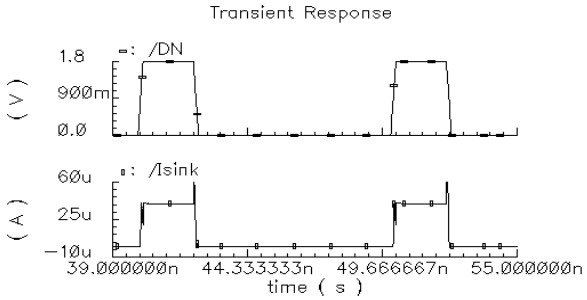

Fig. 10. SpectreRF based simulated transient I_{sink}.

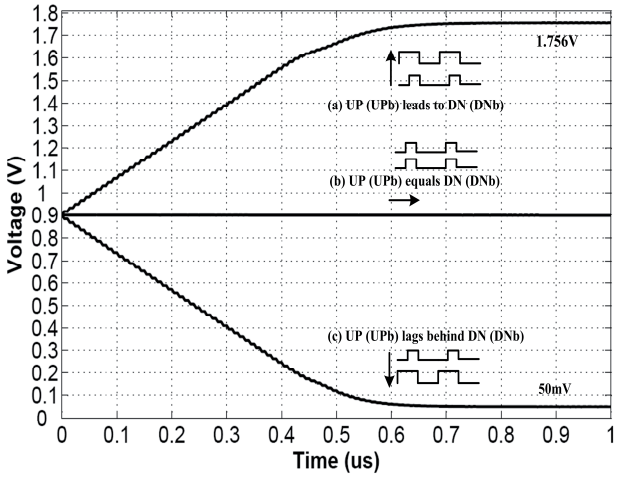

Fig. 11. Output voltage of the charge pump.

Ref.	Tech (μm)	Power (V)	Output Swing (V)	Current Mismatch	Dynamic glitches	Speed
[2]	0.18	1.8	0.5~1.2	0.1%	Medium	Medium
[3]	0.25	2.5	0.25~2.2	1%	Medium	Medium
[4]	0.18	1.2	0.1~1.1	0.5%	Medium	Medium
[5]	0.35	3.3	0.2~3	3%	Low	Fast
[9]	0.13	1.2	—	—	Low	Fast
This	0.18	1.8	0.2~1.52	< 0.1%	Low	Fast

Tab. 2. Comparisons between this design and the existing ones.

In summary, this section proposes a high performance CP circuit. Then, the simulation results are given to dem-

onstrate the design. By the way, a comparison between this work and the others is shown in Tab. 2, in which the medium switch speed is because the CP circuits are based on the source-switching structure [15]. The medium glitch is because charge sharing or charge injection is still existed.

5. Conclusion

A high performance CP circuit is proposed in this paper. The proposed CP circuit benefits perfectly current matching and dynamic glitches suppression. The affections of the non-idealities of the CP upon spurious tones have been theoretically analyzed with the assumption that the LPF is based on a capacitor. The complete CP circuit is designed in TSMC 0.18μm CMOS technology and is verified by SpectreRF simulator. The state-of-the-art in Tab. 2 shows this design may be useful for high current matching over full-swing, low glitch, and fast switching CPs.

References

[1] ŠIMKA, M., DRUTAROVSKÝ, M., FISCHER, V. Testing of PLL-based true random number generator in changing working conditions. *Radioengineering*, 2011, vol. 20, no. 1, p. 94-101.

[2] CHOI, Y. S., HAN, D. H. Gain-boosting charge pump for current matching in phase-locked loop. *IEEE Transactions on Circuits and Systems II*, 2006, vol. 53, no. 10, p. 1022-1025.

[3] LEE, J. S., KEEL, M. S., LIM, S. I., et al. Charge pump with perfect current matching characteristics in phase-locked loops. *Electronics Letters*, 2000, vol. 36, no. 11, p. 1907-1908.

[4] SUN, Y., SIEK, L., SONG, P. Y. Design of a high performance charge pump circuit for low voltage phase-locked loops. In *IEEE International Symposium on Integrated Circuits*. Singapore, 2007, p. 271-274.

[5] CHENG, S. F., TONG, H. T., et al. Design and analysis of an ultra high-speed glitch-free fully differential charge pump with minimum output current variation and accurate matching. *IEEE Transactions on Circuits and Systems*, 2007, vol. 53, no. 9, p. 843 to 847.

[6] TSITOURAS, A., PLESSAS, F., BIRBAS, B., et al. A 1V CMOS programmable accurate charge pump with wide output voltage range. *Microelectronics Journal*, 2011, vol. 42, no. 9, p. 1082 to 1089.

[7] CHARLES, C. T., ALLSTOT, D. J. A buffered charge pump with zero charge sharing. In *IEEE International Symposium on Circuits and Systems*. Seattle (USA, WA), 2008, p. 2633-2636.

[8] BAHREYNI, B., FILANOVSKY, I. M., SHAFAI, C. A novel design for deadzone-less fast charge pump with low harmonic content at the output. In *IEEE Midwest Symposium on Circuits and Systems*. Oklahoma, 2002, p. 397-400.

[9] HWANG, I. C., BAE, S. G. Low-glitch, high-speed charge-pump circuit for spur minimization. *Electronics Letters*, 2009, vol. 45, no. 28, p. 1273-1274.

[10] LEE, H. I., AHN, T. W., JUNG, D. Y., et al. Scheme for no dead zone, fast PFD design. *Korean Physical Society*, 2002, vol. 40, no. 4, p. 543-545.

[11] BANERJEE, D. *PLL Performance, Simulation and Design*. National Semiconductor, 2006.

[12] FENG, K. D., LEE, J. C. Spark current in charge pump of phase lock loop. In *IEEE Custom Integrated Circuits Conference*. Santa Clara, 2005, p. 199-202.

[13] YOUNG, I. A PLL clock generator with 5 to 110 MHz of lock range for microprocessors. *IEEE J. Solid-State Circuits*. 1992, vol. 27, no. 2, p. 1599-1607.

[14] JALALI, M. S., BAKHTIAR, S., MIRABBASI, S. A charge-pump with a high output swing for PLL and CDR applications. In *IEEE International Conference on NEWCAS*. Montreal (QC, Canada), 2010, p. 297-300.

[15] RHEE, W. Design of high-performance CMOS charge pump in phase-locked loops. In *IEEE Custom Integrated Circuits Conference*. Santa Clara, 1999, p. 545-548.

About Authors ...

De-zhi WANG was born in Hubei province, P. R. China in 1983. He received his B.Sc. from Wuhan University of Technology, Wuhan, P. R. China, in 2006, and the M. Sc. and the Ph. D. degree from School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, P.R. China. His researches focus on wideband low noise synthesizers for peer to peer (P2P) mobile terminal, and his research interests include wideband quadrature VCO, fast lock PLLs and variable bandwidth low pass filter (LPF).

Ke-feng ZHANG was born in Shangxi province, P. R. China in 1960. He received his Ph. D. from School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, P.R. China, in 2003. In the same year, he was promoted to the rank of Associate Professor. His research interests include ultra-large-scale integrated circuits, P2P mobile terminal, and next generation mobile communication systems.

Xue-cheng ZOU was born in Hubei province, P. R. China in 1964. He received the B.S, M.S, and Ph.D degrees in Solid State Electronics from Huazhong University of Science and Technology, Wuhan, P. R. China in 1985, 1988, and 1995, respectively. In 1993, he was promoted to the Associate Professor and he was engaged in post-doctoral research in the Department of Electronic Engineering, City University of Hong Kong in 1996. He is currently a professor in School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan, P.R. China. His research interests include VLSI, RFID, information security, SoC, etc.