

# Implementation of a Two-Channel Maximally Decimated Filter Bank using Switched Capacitor Circuits

Jiří NÁHLÍK<sup>1</sup>, Jiří HOSPODKA<sup>1</sup>, Pavel SOVKA<sup>1</sup>, Bohumil PŠENIČKA<sup>2</sup>

<sup>1</sup>Dept. of Circuit Theory, CTU FEL, Technická 2, 166 27 Prague, Czech Republic

<sup>2</sup>Dept. of Telecommunication, University National Autonomous of Mexico, Av. Universidad 3000 Mexico D.F., Mexico

{nahlijir, hospodka, sovka}@fel.cvut.cz, pseboh@servidor.unam.mx

**Abstract.** *The aim of this paper is to describe the implementation of a two-channel filter bank (FB) using the switched capacitor (SC) technique considering real properties of operational amplifiers (OpAmps). The design procedure is presented and key recommendations for the implementation are given. The implementation procedure describes the design of two-channel filter bank using an IIR Causer filter, conversion of IIR into the SC filters and the final implementation of the SC filters. The whole design and an SC circuit implementation is performed by a PraCAn package in Maple. To verify the whole filter bank, resulting real property circuit structures are completely simulated by WinSpice and ELDO simulators. The results confirm that perfect reconstruction conditions can be almost accepted for the filter bank implemented by the SC circuits. The phase response of the SC filter bank is not strictly linear due to the IIR filters. However, the final ripple of a magnitude frequency response in the passband is almost constant, app. 0.5 dB for a real circuit analysis.*

## Keywords

Filter bank realization, SC circuit, filter synthesis.

## 1. Introduction – State of the Art

Analog or digital filter banks have been frequently used in signal processing for decades. Digital filter banks with multi-rate digital signal processing are commonly used in various applications of signal processing, e.g. [2]–[4]. These filter banks often use decimation factor equal to the number of channels, and thus they are referred to as maximally decimated filter banks. The methods for the synthesis of two-channel filter banks have been studied either in digital [6] or hybrid digital/analog forms [7]. In this case the problem of aliasing arises. One interesting idea how to suppress aliasing in the analog two-channel filter bank can be found in [7]. The accuracy demands placed on the analog filters can be neglected if the aliasing is decreased not by the gain cancellation as commonly used in the digital maximally decimated

filter banks, but by a stopband attenuation of the individual filters. In parallel, the circuit design techniques for the SC filters have been also applied. The design of basic SC blocks, e.g. filters, modulators and oscillators are presented in [8]. It is known that not only the IIR and FIR filters could be realized by an SC technique [9] but they can also be realised by the filters integrated into the analysis filter bank; e.g., the 20-channel analysis filter bank for the spectral analysis of the speech [12], or the analysis SC filter bank simulating the cochlea [10]. One solution to the problems connected with a great number of OpAmps needed for an SC implementation of the analysis filter bank is described in [11]. But so far, the SC filter bank with a perfect reconstruction has not been described yet for the discrete-time analog signal processing.

This paper suggests the procedure for the implementation of the SC filter bank based on the conversion of the digital filters into SC filters. Therefore the resulting aliasing must be suppressed by the gain cancellation and not by the stopband attenuation of the filters. In order to simplify the whole implementation process, the two-channel IIR filter bank is used in the first step (see Fig. 1). The analysis filter bank consists of the low-pass filter  $H_0(z)$  and high-pass filter  $H_1(z)$ . Both filters split an input signal  $x[n]$  which is consequently decimated by the factor of 2. After being transmitted, these subband signals are interpolated and then combined by the synthesis filters  $G_0(z)$  and  $G_1(z)$ , which gives an output signal  $\hat{x}[n]$ .

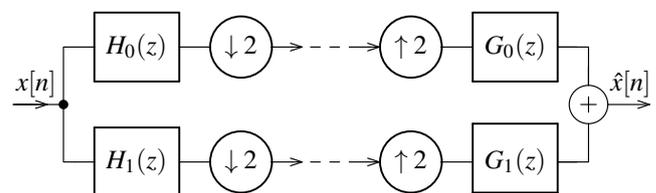


Fig. 1. Basic structure of two-channel filter bank.

## 2. Design of the Filter Bank

The power symmetric IIR filters, i.e.  $|H_0(z)|^2 + |H_1(z)|^2 = 1$  satisfy the condition  $\delta_2^2 = 4\delta_1(1 - \delta_1)$ , where  $\delta_1$  and  $\delta_2$  are the passband and stopband ripples, respectively.

Using perfect reconstruction conditions [4, 5] and a power symmetric property of the IIR filters, high-pass and low-pass filters in both the synthesis and analysis sections of the filter bank can be determined [1]

$$H_1(z) = H_0(-z), \quad (1)$$

$$G_0(z) = 2H_1(-z) = 2H_0(z), \quad (2)$$

$$G_1(z) = -2H_0(-z) = -2H_1(z). \quad (3)$$

The transfer functions of the filters ensure that the output signal  $\hat{x}[n]$  is a delayed replica of the input signal  $x[n]$  without any signal distortion and aliasing.

Equations (1)-(3) indicate that for the digital filter bank only one transfer function  $H_0(z)$  needs to be designed. Other filters can be simply derived from  $H_0$  using (1)-(3). To realize transfer functions  $H_0(z)$  and  $H_1(z)$  in the SC technique, it is necessary to design two different circuits, see the following section. An IIR third order power symmetric elliptic filter is chosen for the realization of  $H_0(z)$ . The third order is the lowest order satisfying power symmetry conditions, i.e. this filter can be derived as the sum of the first and second order all-pass filters

$$H_0(z) = \frac{1}{2} \left( \frac{\alpha + z^{-2}}{1 + \alpha z^{-2}} + z^{-1} \right). \quad (4)$$

The disadvantage of using the third order of the IIR filter is evident, therefore it is necessary to use a SC differentiator, even though it can cause problems in the SC filter bank implementation. A resulting form of  $H_0(z)$  is given by<sup>1</sup>

$$H_0(z) = \frac{1}{2} G_0(z) = \frac{1}{2} \frac{\alpha z^3 + z^2 + z + \alpha}{z(z^2 + \alpha)} \quad (5)$$

where the parameter  $\alpha$  controls the positions of the filter poles and zeros. The poles lie on the imaginary axis while the zeros lie on the unit circle.

Magnitude frequency responses of  $H_0$  for different values of  $\alpha$  are demonstrated in Fig. 2 (for a clock frequency of 16 kHz).

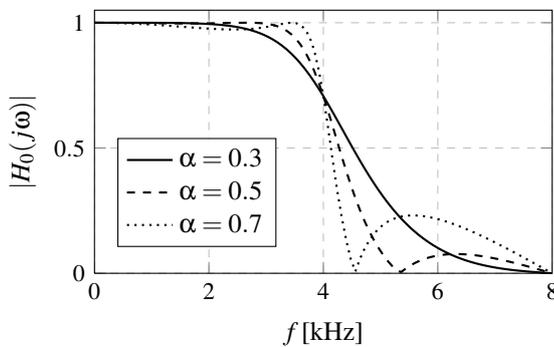


Fig. 2. Magnitude frequency responses of  $H_0$  for various  $\alpha$ .

Using conditions (1)-(3), the transfer function  $H_1(z)$  can be derived from  $H_0(z)$  as follows

$$H_1(z) = -\frac{1}{2} G_1(z) = -\frac{1}{2} \frac{-\alpha z^3 + z^2 - z + \alpha}{z(z^2 + \alpha)}. \quad (6)$$

A transfer function  $TF(z)$  of the whole filter bank can be expressed as

$$TF(z) = \frac{H_0(z)G_0(z) + H_1(z)G_1(z)}{2} = \frac{z^2\alpha + 1}{z(z^2 + \alpha)}. \quad (7)$$

A frequency response of the resulting filter bank corresponds to an all-pass filter with a nonlinear phase response caused by the implemented IIR filters. Whereas a magnitude response is constant for all values of  $\alpha \in (0, 1)$ , the phase responses are nonlinear and are dependent on the parameter  $\alpha$  (see Fig. 3). The group delay of the filter bank is given in Fig. 4. Thus it is evident that the IIR filters cannot fully meet the conditions for a perfect reconstruction due to their nonlinear phase characteristic. Nevertheless, perfect reconstruction conditions are fully satisfied for the magnitude response regardless the coefficient of an  $\alpha$  value, which, is anyway, sufficient for many applications.

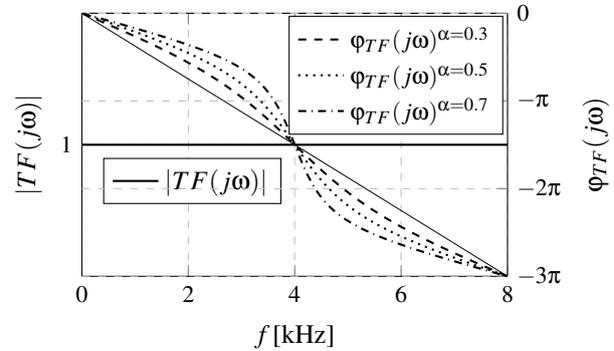


Fig. 3. Frequency responses of the whole filter bank. Magnitude responses are constant for  $\alpha \in (0, 1)$ . Phase responses are not linear as shown for  $\alpha = 0.3, 0.5,$  and  $0.7$ .

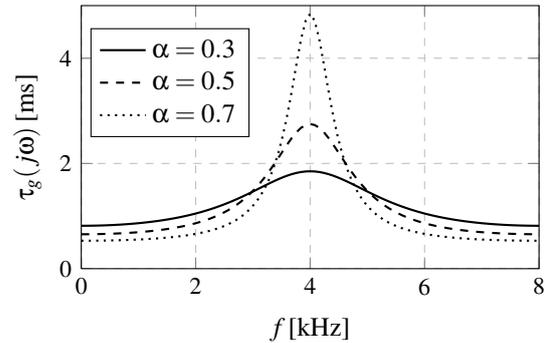


Fig. 4. Group delays of the whole filter bank for various  $\alpha$ .

As expected, the linearity of the phase characteristics is better for smaller values of  $\alpha$ . The transition filter band is narrower for higher values of  $\alpha$  but the ripple in the stop-band is greater (see Fig. 5), where the magnitude frequency responses in the stopband of the low-pass branch of the filter bank ( $H_0G_0$ ) is shown for various  $\alpha$ . Therefore,  $\alpha$  should be taken as a compromise between the slope of the magnitude response in the transition band and the ripple in the stop-band. The determination of  $\alpha$  is described in the following subsection.

<sup>1</sup>Positive powers of  $z$  are used in all following relations according to [13].

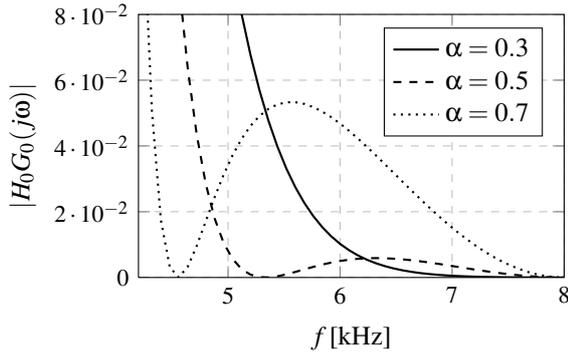


Fig. 5. Magnitude frequency responses in the stopband of the transfer function  $H_0G_0$  for various  $\alpha$ .

## 2.1 Determination of $\alpha$ Parameter

Parameter  $\alpha$  changes the positions of the poles and zeros of the transfer function  $H_0(z)$ . In this way, the magnitude and phase frequency responses of the corresponding filters are changed as shown in the previous section. A perfect signal reconstruction requiring a simultaneous constant magnitude and linear phase responses is feasible only for  $\alpha = 0$ , which leads to the degradation of the filters. For nonzero  $\alpha$ , the phase response is not linear, which causes a signal distortion (see Section 4).

An optimal value of the parameter  $\alpha$  can be determined by minimizing the energy of the signal passed through the stopband of the filter bank branch. The transfer function of the low-pass branch is expressed by

$$TF_{LP}(z) = H_0(z)G_0(z) = \frac{1}{4} \frac{(\alpha z^3 + z^2 + z\alpha)^2}{z^2(z^2 + \alpha)^2}. \quad (8)$$

The energy of the signal passed through the stopband of this branch can be expressed as

$$E_{SLP}(\Theta_s, \alpha) = \int_{\Theta_s}^{\pi} TF_{LP}(z = e^{j\Theta}) TF_{LP}(z = e^{-j\Theta}) d\Theta \quad (9)$$

where  $\Theta$  is the normalized frequency and  $\Theta_s$  is the normalized stopband frequency of the filter. Unfortunately, the determination of the minimum of  $E_{SLP}(\Theta_s, \alpha)$  is a highly nonlinear problem because of a  $\Theta_s$  dependence on  $\alpha$ . Thus there is no analytical solution for  $\arg \min_{\alpha} E_{SLP}$ . The suboptimal three-step procedure can be used for determining  $\alpha$ . First, the stopband frequency  $\Theta_s$  is estimated. Second, for given  $\Theta_s$ , the  $\arg \min_{\alpha} E_{SLP}$  is evaluated giving the optimal  $\alpha_{id}$ . Third, the numerical evaluation of the  $\alpha_{id}$  on various  $\Theta_s$  values is performed to determine a sensitivity of the  $\alpha_{id}$  on the  $\Theta_s$  value. The whole procedure is illustrated in Figs. 5-7. The estimate  $\Theta_s = \frac{3}{5}\pi$  comes from the reasonable compromise between the transition bandwidth and the stopband ripple (see Fig. 5). The energy of the signal passed through the low-pass branch is then calculated analytically according to (9) for  $\Theta_s = \frac{3}{5}\pi$  (or  $f_s = 4.8$  kHz for the clock frequency  $f_c = 16$  kHz). The resulting expression is too complicated to be written down here. To determine the optimal  $\alpha_{id}$  ensuring the minimum of the energy  $E_{SLP}$  (see Fig. 6), the dependence of the energy  $E_{SLP}$  on  $\alpha$  is evaluated together with its differentiation.

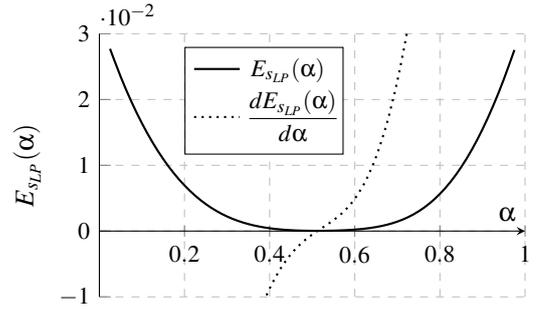


Fig. 6. Energy of the signal passed through the filter stopband varying with  $\alpha \in (0, 1)$  and its differentiation. The stopband frequency was set to  $\Theta_s = 3\pi/5 = 4.8$  kHz for  $f_c = 16$  kHz.

An Optimal value is  $\alpha_{id} \doteq 0.51$ . It should be noted that the estimate of this  $\alpha_{id}$  is biased due to the fixed value of the stopband frequency  $\Theta_s$ . Therefore the  $\alpha_{id}$  is verified also numerically for various values of the stopband frequency  $\Theta_s$  (see Fig. 7).

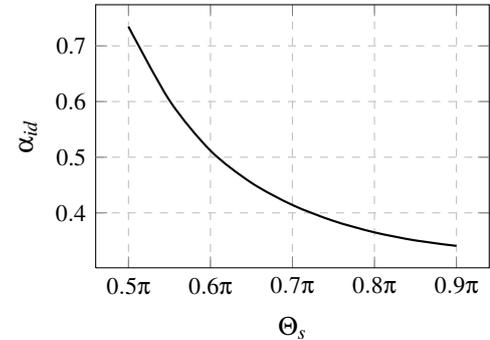


Fig. 7. Parameter  $\alpha_{id}$  versus  $\Theta_s$ .

The sensitivity of  $\alpha$  on  $\Theta_s$  is not critical (see Fig. 7). Moreover, the minimum of the energy  $E_{SLP}$  is rather flat for a wide range of  $\alpha$  values (see Fig 6). Thus, for the implementation of the filters in the filter bank, the coefficient  $\alpha = 0.5$  has been chosen. This estimate of  $\alpha$  also ensures good ratios of the capacitors in the implementation of the SC circuits, which will be seen in the following section.

## 3. SC Filter Bank Implementation

The approach used in this paper extends the methods suggested in [9], [10]. First, due to the cascade synthesis for the filter implementation, it is necessary to factorize the transfer functions  $H_0$  and  $H_1$

$$H_0(z) = H_{01}(z) \cdot H_{02}(z) = \frac{z+1}{2z} \cdot \frac{z^2\alpha + z - z\alpha + \alpha}{z^2 + \alpha}, \quad (10)$$

$$H_1(z) = H_{11}(z) \cdot H_{12}(z) = \frac{z-1}{2z} \cdot \frac{z^2\alpha - z + z\alpha + \alpha}{z^2 + \alpha}. \quad (11)$$

Similarly,  $G_0$  and  $G_1$  functions should be factorized:  $G_0(z) = G_{01}(z) \cdot H_{02}(z)$  where  $G_{01}(z) = \frac{z+1}{z}$  and  $G_1(z) = G_{11}(z) \cdot H_{12}(z)$  where  $G_{11}(z) = \frac{z-1}{z}$ .

Each of the functions is composed of one first order section and one biquadratic section. For an effective implementation, the cascading is made, so that the biquadratic section were followed by the first order section. It is necessary to note that the input signal of the biquadratic section should be sampled in the first phase and held during the second phase for a proper function (see Fig. 9). In order to maximize a dynamic range, the gain of both transfer functions of the cascaded filters should be divided in the rate  $K \doteq 1.23$  for  $\alpha = 0.5$ . Thus, the first order transfer functions ( $H_{01}$ ,  $H_{11}$ ) should be multiplied by the factor  $K$ , while the second order functions ( $H_{02}$ ,  $H_{12}$ ) should be divided by this factor [1].

The  $-H_{01}$  and  $-G_{01}$  functions can be realized by the network in Fig. 8 which has been newly synthesized. The  $-H_{11}$  and  $-G_{11}$  functions are the transfer functions of a differentiator which can be implemented according to [14] by the circuit presented in Fig. 8. Biquadratic functions are realized by a simplified Fleischer-Laker biquad [14] shown in Fig. 8.

The transfer functions and normalized values of the capacitors were derived in [1]. The block diagram of the filter bank implementation is shown in Fig. 9. The control signals of all the switches are derived from the main clock signal<sup>2</sup>  $f_c$ :  $f_s = f_c \cdot f_{c2}$ , where  $f_{c2} = f_c/2$ ,  $f'_s = \overline{f_c + f_{c2}}$ , consequently the frequencies of the signals  $f_s$  and  $f'_s$  are one half of the  $f_c$  signal frequency [1].

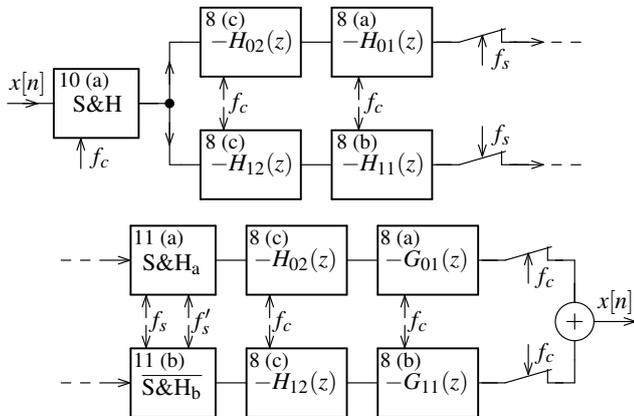


Fig. 9. The block diagram of an implemented SC filter bank.

The circuit structure starts with a common S&H circuit illustrated in Fig. 10 (a) (see the reference number in the upper left corner of the blocks) which is necessary for getting proper transfer functions of the biquads ( $-H_{02}(z)$ ,  $-H_{12}(z)$ ). These blocks are followed by the first order sections ( $-H_{01}(z)$ ,  $-H_{11}(z)$ ) and downsampling circuits realized by the switches. All these blocks represent the analysis filter bank.

The synthesis filter bank can be realized similarly to the analysis filter bank. Up-sampling circuits are combined with the S&H circuits to get proper transfer functions of the

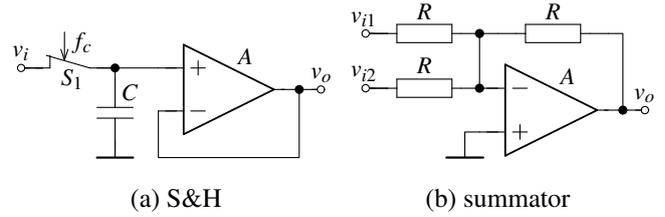


Fig. 10. Input S&H (a) and output summing (b) realization circuits.

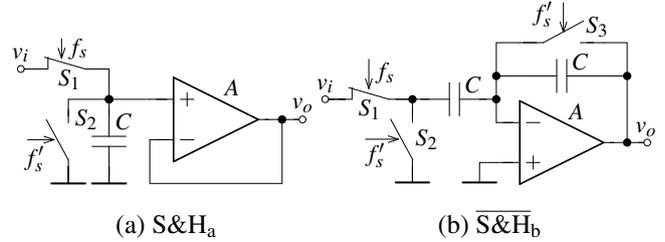


Fig. 11. Noninverting (a) and inverting (b) S&H circuits.

biquads ( $-H_{02}(z)$ ,  $-H_{12}(z)$ ). The structures of these S&H circuits are given in Fig. 11. An inverting S&H circuit is necessary for  $G_1(z)$  realization (see a minus sign in (3)). Switch  $S_3$  in Fig. 11(b) does not affect a proper function of the idealized circuit, but it is necessary for minimizing the influence of an OpAmp input voltage offset.

Output switches presented in the block diagram of the filter bank (Fig. 9) provide the sampling of the output signals in the first phase, for which the transfer functions were derived. The summator at the end of the block diagram can be realized by the circuit in Fig. 10 (b). A symbolic analysis and all derivations were made in Maple™ program with a PraCAN package [15].

## 4. Implementation Results

The designed filter bank was realized by the above mentioned circuit diagrams. The part values for the implementation are used in the following tables.

	$C_1$	$C_2, C_3, C_4$		$C_1$	$C_2$
$H_{01}$	61.5	100	$H_{11}$	61.5	100
$G_{01}$	123	100	$G_{11}$	123	100

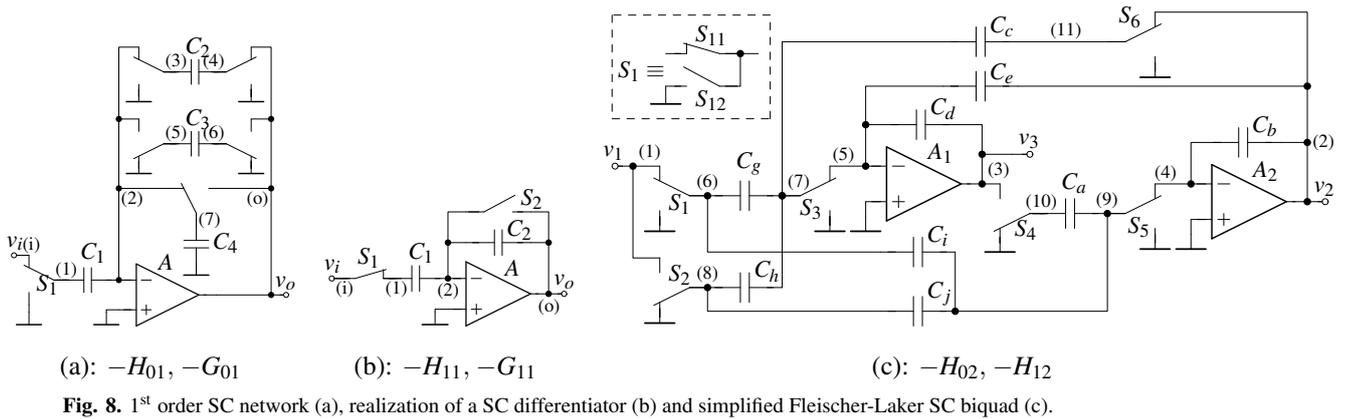
(a) (b)

Tab. 1. Capacitance values for the implementation of the transfer functions  $-H_{01}$  and  $-G_{01}$  according to Fig. 8 (a) in Tab. (a) and for the transfer functions  $-H_{01}$  and  $-G_{01}$  according to Fig. 8 (b) in Tab. (b). The values are given in pF.

	$C_a, C_d$	$C_b$	$C_c$	$C_e$	$C_g$	$C_i, C_j$
$H_{02}$	100	75	112.5	37.5	91.5	30.5
$H_{12}$	100	75	112.5	37.5	30.5	30.5

Tab. 2. Capacitance values for the implementation  $-H_{02}$  and  $-H_{12}$  according to Fig. 8 (c). The values are given in pF,  $C_h = 0$ .

<sup>2</sup>Operators "." and "+" are used as binary operations.



The component values of the S&H and output summator circuits (Figs. 10 and 11) are:  $C = 100$  pF for the capacitor and  $R = 10$  k $\Omega$  for the resistances.

The resulting structure of the filter bank was verified by the analysis performed by the WinSpice program [17], [16] and the ELDO simulator of Mentor Graphics development environment [18].

The simulation of the filter bank was provided by the transient analysis followed by the Discrete Fourier Transform (DFT), as stated in [16]. The simulations were provided with the following simulator settings:  $reltol = 1e-1$ ,  $trtol = 4$ ,  $chgtol = 1e-16$  and  $method = gear$ . The capacitances were modeled by the ideal capacitors with leakage resistors. The switches were modeled by their resistances both in on-state and off-state. The charge injections of the switches were modeled by the overlapping capacitors.

The simulated impulse response obtained by the ELDO simulator with LT1055 OpAmp models is shown in Fig. 12.

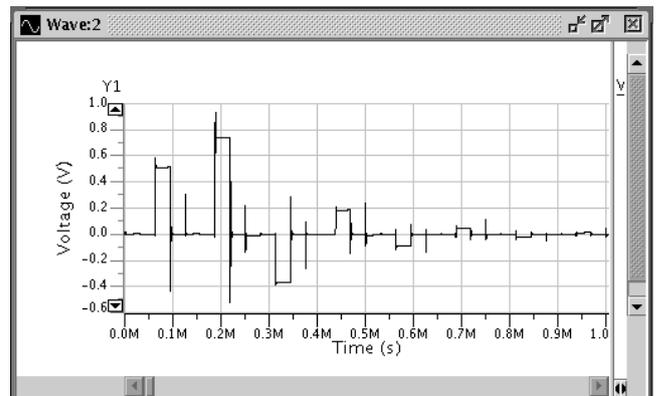
The impulse response corresponds to the ideal impulse response given by the inverse  $Z$  transform of the whole filter bank transfer function  $TF(z)$  according to relation (7)

$$h(n) = 2\delta(n-1)(n) - \frac{3}{\sqrt{2}} \left(\frac{1}{2}\right)^n 2^{\frac{n}{2}} \sin\left(\pi\frac{n}{2}\right) \quad (12)$$

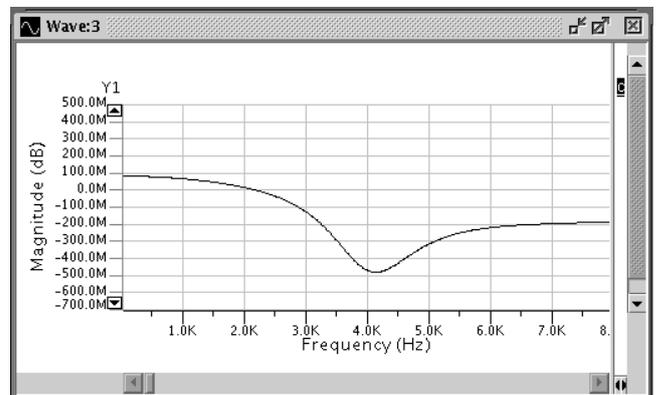
where  $n$  is a natural number and  $\delta(n-1)$  is the unit impulse delayed by one sample.

The differences from the ideal response are evident especially during the switching. The glimmers in the time response are caused by the dynamic properties of the OpAmp used in this case. These errors show the influence on the computed frequency response. The frequency response of the filter bank is calculated from the impulse response using DFT. The setting of the transient analysis and DFT parameters are pivotal for the validity of the whole analysis [16]. The simulations were realized by means of various spice models of OpAmp in order to show the impact of its properties on the frequency response. However, many OpAmp models cause a non-convergence of the simulation.

From our experience, big influence on the convergence of the simulation is caused by the OpAmp model. The simu-



**Fig. 12.** Initial part of the impulse response of the filter bank analysed with the help pf LT1055 OpAmp models in the ELDO simulator.



**Fig. 13.** Analysed magnitude frequency response of the filter bank in the ELDO simulator.

lations with the help of OpAmp models based on the Boyle model [19] usually converge. The models based on [22] must be usually modified. Most problems with the simulation convergence are caused by the noise sources usually located in series in input pins. For low-noise OpAmps, the noise sources can be neglected.

The frequency response of the filter bank with LT1055 [21] OpAmp model [21] is shown in Figs. 4 and 14. The results obtained from the ELDO simulator and the Winspice program are nearly the same.

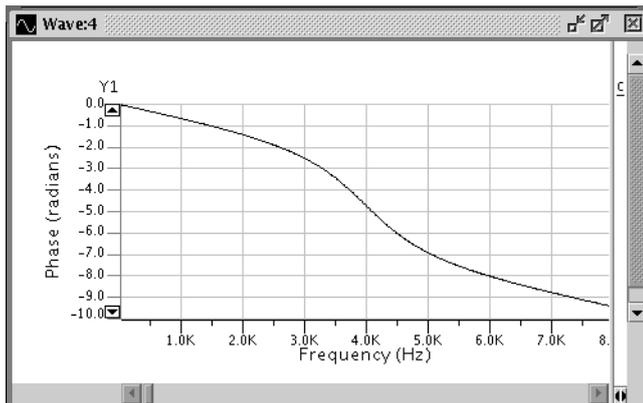


Fig. 14. Analysed phase frequency response of the filter bank in the ELDO simulator.

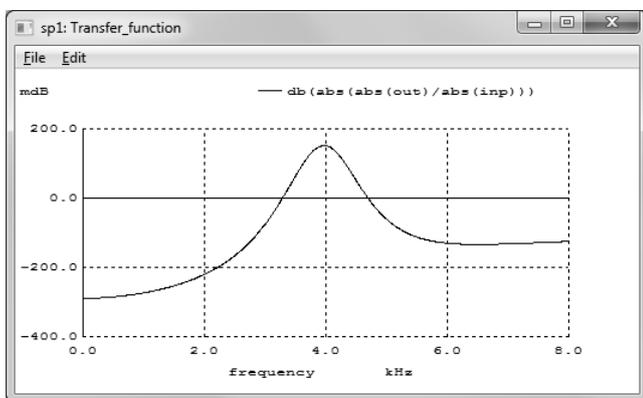


Fig. 15. Analysed magnitude frequency response of the filter bank in the WinSpice simulator.

The differences between the ideal and the simulated magnitude frequency responses are less than 0.5 dB.

The magnitude frequency response of the filter bank calculated by the WinSpice program with the help of AD8033 OpAmp model [24], [23] is shown in Fig. 15. The shape of the frequency response is dependent on the used OpAmp, as shown in Figs. 4 and 15. Significant differences are evident at the frequency near 4 kHz, where the transfer functions of both branches are the most sensitive.

Complete analyses were realized by real models affecting all the essential nonlinearities (including nonlinearities of the OpAmp and dynamic characteristics, a charge injection of the switches etc.). The analyses confirm a filter bank design and the possibility of the SC implementation with a special type of an integrated circuit.

## 5. Conclusion

This paper presents a design of a two-channel maximally decimated IIR filter bank and its implementation by SC circuits. The implementation confirms that the main characteristics of the digital filter bank are preserved. The SC filter bank uses the decimation of a discrete-

time analog signal similarly to the original digital filter bank. Appropriate transfer functions of the third-order elliptic IIR filters and their implementation using an SC technique is described. Used SC circuits were simulated with real characteristics of the used components.

The simulations and all derivations were performed by the Maple program, the simulations of the idealized circuits with a PraCAN package. The analysis of real circuit structures was performed by the WinSpice program and the ELDO simulator of Mentor Graphics development environment. The comments on the simulation convergence and here used OpAmp model structures are presented. Obtained results are in agreement with the theoretical derivations. The suggested approach enables a low-cost and robust implementation of the filter bank by means of the SC circuits.

## Acknowledgements

The work has been supported by the research project PAPIIT IN 114012-3 of the Universidad Nacional Autónoma de México and by the grant No. SGS12/143/OHK3/2T/13 of the CTU in Prague.

Maple is a registered trademark of Waterloo Maple Inc. All other trademarks are property of their respective owners.

## References

- [1] HOSPODKA, J., SOVKA, P., PŠENIČKA, B. Design and realization of a filter bank by switched capacitor technique. In *20<sup>th</sup> European Conference on Circuit Theory and Design (ECCTD 2011)*. Linköping (Sweden), 2011, p. 782 - 785.
- [2] MADISETTI, V. K., WILLIAMS, D. B. (eds.) *The Digital Signal processing Handbook*. Boca Raton (USA): CRC Press 1998.
- [3] CROCHIERE, R. E., RABINER, L. R. *Multirate Digital Signal Processing*. New Jersey (USA): Prentice-Hall, 1983.
- [4] FLIEGE, N. J. *Multirate Digital Signal Processing*. New York (USA): Wiley, 1994.
- [5] VAIDYANATHAN, P. P. *Multirate Systems and Filter Bank*. New Jersey (USA): Prentice-Hall, 1993.
- [6] PHOONG, S., KIM, C. W., VAIDYANATHAN, P. P., ANSARI, R. A new class of two-channel biorthogonal filter banks and wavelet bases. *IEEE Transactions on Signal Processing*, 1995, vol. 43, no. 3, p. 649 - 665.
- [7] LOWENBERG, P., JOHANSON, H., WANHAMMER, L. Two-channel hybrid analog/digital filter banks with alias-free subbands. In *Proceedings of the 43<sup>rd</sup> IEEE Midwest Symposium on Circuits and Systems*. Lansing (USA), 2000, vol. 3, p. 1162 - 1165.
- [8] GREGORIAN, R., MARTIN, K. W. Switched-capacitor circuit design. *Proceedings of the IEEE*, 1983, vol. 71, no. 8, p. 941 - 966.
- [9] TSAI-CHUNG YU, CHUNG-YU WU, SHIN-SHI CHANG Realizations of IIR/FIR and  $N$ -path filters using a novel switched-capacitor technique. *IEEE Transactions on Circuits and Systems*, 1990, vol. 37, no. 1, p. 91 - 406.

- [10] LIN, J., SHAMMA, S. A., EDWARDS, T. G. *Cochlear Filter Bank with Switched-Capacitor Circuits*. United States Patent No. US005331222A, 1994.
- [11] BOSSHART, P. W. A multiplexed switched capacitor filter bank. *IEEE Journal of Solid-State Circuits*, 1980, vol. sc-15, no. 6, p. 939 - 945.
- [12] KURAIISHI, Y., NAKAYAMA, K., MIYADERA, K., OKAMURA, T. A single-chip 20-channel speech spectrum analyser using a multiplexed switched-capacitors filter bank. *IEEE Journal of Solid-State Circuits*, 1984, vol. sc-19, no. 6, p. 964 - 970.
- [13] VICH, R. Z *Transform Theory and Applications*. Boston (USA): D. Reidel Publishing Company, 1987.
- [14] ANANDA MOHAN, P. V., RAMACHANDRAN, V., SWAMY, M. N. S. *Switched Capacitor Filters: Theory, Analysis and Design*. New Jersey (USA): Prentice Hall, 1995.
- [15] BICAK, J., HOSPODKA, J. PraCA<sub>n</sub> – Maple package for symbolic circuit analysis. In *Digital Technologies*. Žilina (Slovakia), 2008.
- [16] BICAK, J., HOSPODKA, J. Frequency response of switched circuits in SPICE. In *The 16<sup>th</sup> European Conference on Circuits Theory and Design (ECCTD)*. Kraków (Poland), 2003, vol. I, p. 333 - 336.
- [17] SMITH, M. *WinSpice User's Manual* [Online] 2009. Cited 2012-10-06. Available at: <http://www.winspice.com> .
- [18] *Mentor Graphics Corp*. Available at: <http://www.mentor.com> .
- [19] JUNG, W. *Using the LTC OpAmp Macromodels*, AN48 [Online] 1991, Cited 2012-10-06. Available at: <http://cds.linear.com/> .
- [20] Linear Technology, *LT1055 Datasheet* [Online], 2004. Cited 2012-10-06. Available at: <http://cds.linear.com/> .
- [21] Linear Technology, *LT1055 Spice model* [Online], 2005. Cited 2012-10-06. Available at: <http://cds.linear.com/> .
- [22] ALEXANDER, M., BOWERS, D. F. *Spice-Compatible Op Amp Macro-Models*. [Online], 1990. Cited 2012-10-06. Available at: <http://www.analog.com/> .
- [23] Analog devices, Inc., *AD8033 Data Sheet*, Rev C. [Online], 2008. Cited 2012-10-06. Available at: <http://www.analog.com/> .
- [24] Analog devices, Inc., *AD8033 Spice Macro-model*, Rev E [Online], 2012. Cited 2012-10-06. Available at: <http://www.analog.com/> .

## About Authors...

**Jiří NÁHLÍK** was born in 1987. He graduated from the Czech Technical University in Prague in 2011. Since then, he has been in a Ph.D. study program at the Department of Circuit Theory at the same university. His research interests deal with the design of modern analog circuits, as well as their optimization.

**Jiří HOSPODKA** was born in 1967. He received his Master's and Ph.D. degrees, from the Czech Technical University in Prague in 1991 and 1995, respectively. Since 2007 he has been working as associate professor at the Department of Circuit Theory at the same university. Research interests: circuit theory, analogue electronics, filter design, switched-capacitor, and switched-current circuits.

**Pavel SOVKA** received his Master's and Ph.D. degrees in electrical engineering at the Faculty of Electrical Engineering (FEE), the Czech Technical University in Prague (CTU), in 1981 and 1986, respectively. From 1985 to 1991 he worked in the Institute of Radioengineering and Electronics of the Czech Academy of Sciences, Prague. In 1991 he joined the Department of Circuit Theory, FEE CTU. He worked on the application of adaptive systems to the noise and echo cancellation, speech analysis, changepoint detection and signal separation. At present, he is engaged in the research of biomedical signal processing and selective spectral transforms.

**Bohumil PŠENIČKA** was born in 1933. He received his doctoral degree from the Czech Technical University in Prague in 1962. Since 1970 he has been working as an associate professor at the Department of Circuit Theory at the same university and in 1993 he was appointed Professor titular C at the University National Autonomous of Mexico. Research Interests: circuit theory, analog and digital filter design, digital signal processing.