Implementation of a Two-Channel Maximally Decimated Filter Bank using Switched Capacitor Circuits

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Abstract. The aim of this paper is to describe the implementation of a two-channel filter bank (FB) using the switched capacitor (SC) technique considering real properties of operational amplifiers (OpAmps). The design procedure is presented and key recommendations for the implementation are given. The implementation procedure describes the design of two-channel filter bank using an IIR Cauer filter, conversion of IIR into the SC filters and the final implementation of the SC filters. The whole design and an SC circuit implementation is performed by a PraCan package in Maple. To verify the whole filter bank, resulting real property circuit structures are completely simulated by WinSpice and ELDO simulators. The results confirm that perfect reconstruction conditions can be almost accepted for the filter bank implemented by the SC circuits. The phase response of the SC filter bank is not strictly linear due to the IIR filters. However, the final ripple of a magnitude frequency response in the passband is almost constant, app. 0.5 dB for a real circuit analysis.

Keywords
Filer bank realization, SC circuit, filter synthesis.

1. Introduction – State of the Art

Analog or digital filter banks have been frequently used in signal processing for decades. Digital filter banks with multi-rate digital signal processing are commonly used in various applications of signal processing, e.g. [2]–[4]. These filter banks often use decimation factor equal to the number of channels, and thus they are referred to as maximally decimated filter banks. The methods for the synthesis of two-channel filter banks have been studied either in digital [6] or hybrid digital/analog forms [7]. In this case the problem of aliasing arises. One interesting idea how to suppress aliasing in the analog two-channel filter bank can be found in [7]. The accuracy demands placed on the analog filters can be neglected if the aliasing is decreased not by the gain cancellation as commonly used in the digital maximally decimated filter banks, but by a stopband attenuation of the individual filters. In parallel, the circuit design techniques for the SC filters have been also applied. The design of basic SC blocks, e.g. filters, modulators and oscillators are presented in [8]. It is known that not only the IIR and FIR filters could be realized by an SC technique [9] but they can also be realised by the filters integrated into the analysis filter bank; e.g., the 20-channel analysis filter bank for the spectral analysis of the speech [12], or the analysis SC filter bank simulating the cochlea [10]. One solution to the problems connected with a great number of OpAmps needed for an SC implementation of the analysis filter bank is described in [11]. But so far, the SC filter bank with a perfect reconstruction has not been described yet for the discrete-time analog signal processing.

This paper suggests the procedure for the implementation of the SC filter bank based on the conversion of the digital filters into SC filters. Therefore the resulting aliasing must be suppressed by the gain cancellation and not by the stopband attenuation of the filters. In order to simplify the whole implementation process, the two-channel IIR filter bank is used in the first step (see Fig. 1). The analysis filter bank consists of the low-pass filter $H_0(z)$ and high-pass filter $H_1(z)$. Both filters split an input signal $x[n]$ which is consequently decimated by the factor of 2. After being transmitted, these subband signals are interpolated and then combined by the synthesis filters $G_0(z)$ and $G_1(z)$, which gives an output signal $\hat{x}[n]$.

![Fig. 1. Basic structure of two-channel filter bank.](image)

2. Design of the Filter Bank

The power symmetric IIR filters, i.e. $|H_0(z)|^2 + |H_1(z)|^2 = 1$ satisfy the condition $\delta_2 = 4\delta_1(1 - \delta_1)$, where $\delta_1$ and $\delta_2$ are the passband and stopband ripples, respectively.
Using perfect reconstruction conditions [4, 5] and a power symmetric property of the IIR filters, high-pass and low-pass filters in both the synthesis and analysis sections of the filter bank can be determined [1]

\[ H_1(z) = H_0(-z), \quad G_0(z) = 2H_1(-z) = 2H_0(z), \quad G_1(z) = -2H_0(-z) = -2H_1(z). \]

The transfer functions of the filters ensure that the output signal \( \hat{x}[n] \) is a delayed replica of the input signal \( x[n] \) without any signal distortion and aliasing.

Equations (1)-(3) indicate that for the digital filter bank only one transfer function \( H_0(z) \) needs to be designed. Other filters can be simply derived from \( H_0 \) using (1)-(3). To realize transfer functions \( H_0(z) \) and \( H_1(z) \) in the SC technique, it is necessary to design two different circuits, see the following section. An IIR third order power symmetric elliptic filter is chosen for the realization of \( H_0(z) \). The third order is the lowest order satisfying power symmetry conditions, i.e. this filter can be derived as the sum of the first and second order all-pass filters

\[ H_0(z) = \frac{1}{2} \left( \frac{\alpha + z^{-2}}{1 + \alpha z^{-2}} \right) \]  

(4)

The disadvantage of using the third order of the IIR filter is evident, therefore it is necessary to use a SC differentiator, even though it can cause problems in the SC filter bank implementation. A resulting form of \( H_0(z) \) is given by

\[ H_0(z) = \frac{1}{2} G_0(z) = \frac{1}{2} \frac{\alpha z^2 + z^3 + z + \alpha}{z(\alpha^2 + 1)} \]  

(5)

where the parameter \( \alpha \) controls the positions of the filter poles and zeros. The poles lie on the imaginary axis while the zeros lie on the unit circle.

Magnitude frequency responses of \( H_0 \) for different values of \( \alpha \) are demonstrated in Fig. 2 (for a clock frequency of 16 kHz).

Using conditions (1)-(3), the transfer function \( H_1(z) \) can be derived from \( H_0(z) \) as follows

\[ H_1(z) = -\frac{1}{2} G_1(z) = -\frac{1 - \alpha z^3 + z^2 - z + \alpha}{2 z(\alpha^2 + 1)}. \]  

(6)

A transfer function \( TF(z) \) of the whole filter bank can be expressed as

\[ TF(z) = \frac{H_0(z) G_0(z) + H_1(z) G_1(z)}{2} = \frac{z^2 + 1}{z(\alpha^2 + 1)}. \]  

(7)

A frequency response of the resulting filter bank corresponds to an all-pass filter with a nonlinear phase response caused by the implemented IIR filters. Whereas a magnitude response is constant for all values of \( \alpha \in (0, 1) \), the phase responses are nonlinear and are dependent on the parameter \( \alpha \) (see Fig. 3). The group delay of the filter bank is given in Fig. 4. Thus it is evident that the IIR filters cannot fully meet the conditions for a perfect reconstruction due to their nonlinear phase characteristic. Nevertheless, perfect reconstruction conditions are fully satisfied for the magnitude response regardless the coefficient of an \( \alpha \) value, which is, anyway, sufficient for many applications.

![Fig. 3](frequency_responses.png)

**Fig. 3.** Frequency responses of the whole filter bank. Magnitude responses are constant for \( \alpha \in (0, 1) \). Phase responses are not linear as shown for \( \alpha = 0.3, 0.5, \) and 0.7.

![Fig. 4](group_delays.png)

**Fig. 4.** Group delays of the whole filter bank for various \( \alpha \).

As expected, the linearity of the phase characteristics is better for smaller values of \( \alpha \). The transition filter band is narrower for higher values of \( \alpha \) but the ripple in the stopband is greater (see Fig. 5), where the magnitude frequency responses in the stopband of the low-pass branch of the filter bank \( (H_0 G_0) \) is shown for various \( \alpha \). Therefore, \( \alpha \) should be taken as a compromise between the slope of the magnitude response in the transition band and the ripple in the stopband. The determination of \( \alpha \) is described in the following subsection.

1 Positive powers of \( z \) are used in all following relations according to [13].
2.1 Determination of α Parameter

Parameter α changes the positions of the poles and zeros of the transfer function \( H_0(z) \). In this way, the magnitude and phase frequency responses of the corresponding filters are changed as shown in the previous section. A perfect signal reconstruction requiring a simultaneous constant magnitude and linear phase responses is feasible only for \( \alpha = 0 \), which leads to the degradation of the filters. For nonzero \( \alpha \), the phase response is not linear, which causes a signal distortion (see Section 4).

An optimal value of the parameter \( \alpha \) can be determined by minimizing the energy of the signal passed through the stopband of the filter bank branch. The transfer function of the low-pass branch is expressed by

\[
TF_{LP}(z) = H_0(z)G_0(z) = \frac{1}{4} \frac{(\alpha z^3 + z^2 + \alpha z)^2}{z^2 (z^2 + \alpha)^2}. \tag{8}
\]

The energy of the signal passed through the stopband of this branch can be expressed as

\[
E_{stdB}(\Theta_s, \alpha) = \int_{\Theta_s}^{\pi} TF_{LP}(z = e^{i\theta}) TF_{LP}(z = e^{-i\theta}) d\theta \tag{9}
\]

where \( \Theta_0 \) is the normalized frequency and \( \Theta_s \) is the normalized stopband frequency of the filter. Unfortunately, the determination of the minimum of \( E_{stdB}(\Theta_s, \alpha) \) is a highly nonlinear problem because of a \( \Theta_s \) dependence on \( \alpha \). Thus there is no analytical solution for \( \alpha_{opt} \). The suboptimal three-step procedure can be used for determining \( \alpha \). First, the stopband frequency \( \Theta_s \) is estimated. Second, for given \( \Theta_s \), the \( \alpha \) is evaluated giving the optimal \( \alpha_{id} \). Third, the numerical evaluation of the \( \alpha_{id} \) on various \( \Theta_s \) values is performed to determine a sensitivity of the \( \alpha_{id} \) on the \( \Theta_s \) value. The whole procedure is illustrated in Figs. 5-7. The estimate \( \Theta_s = \frac{\pi}{64} \) comes from the reasonable compromise between the transition bandwidth and the stopband ripple (see Fig. 5). The energy of the signal passed through the low-pass branch is then calculated analytically according to (9) for \( \Theta_s = \frac{\pi}{6} \) (or \( f_s = 4.8 \text{kHz} \) for the clock frequency \( f_c = 16 \text{kHz} \)). The resulting expression is too complicated to be written down here. To determine the optimal \( \alpha_{id} \) ensuring the minimum of the energy \( E_{stdB} \) (see Fig. 6), the dependence of the energy \( E_{stdB} \) on \( \alpha \) is evaluated together with its differentiation.

An Optimal value is \( \alpha_{id} = 0.51 \). It should be noted that the estimate of this \( \alpha_{id} \) is biased due to the fixed value of the stopband frequency \( \Theta_s \). Therefore the \( \alpha_{id} \) is verified also numerically for various values of the stopband frequency \( \Theta_s \) (see Fig. 7).

\[
\Theta_s = \frac{\pi}{64}, 0.125, 0.25, 0.375, 0.5, 0.625, 0.75, 0.875, 1.0 \pi.
\]

The sensitivity of \( \alpha \) on \( \Theta_s \) is not critical (see Fig. 7). Moreover, the minimum of the energy \( E_{stdB} \) is rather flat for a wide range of \( \alpha \) values (see Fig. 6). Thus, for the implementation of the filters in the filter bank, the coefficient \( \alpha = 0.5 \) has been chosen. This estimate of \( \alpha \) also ensures good ratios of the capacitors in the implementation of the SC circuits, which will be seen in the following section.

3. SC Filter Bank Implementation

The approach used in this paper extends the methods suggested in [9], [10]. First, due to the cascade synthesis for the filter implementation, it is necessary to factorize the transfer functions \( H_0 \) and \( H_1 \)

\[
H_0(z) = H_{01}(z)\cdot H_{02}(z) = \frac{z + 1}{2z} \cdot \frac{z^2 + \alpha^2 - z\alpha + \alpha}{z^2 + \alpha}, \tag{10}
\]

\[
H_1(z) = H_{11}(z)\cdot H_{12}(z) = \frac{z - 1}{2z} \cdot \frac{z^2 - z\alpha + z\alpha + \alpha}{z^2 + \alpha}. \tag{11}
\]

Similarly, \( G_0 \) and \( G_1 \) functions should be factorized:

\[
G_0(z) = G_{01}(z)\cdot H_{02}(z) \quad \text{where} \quad G_{01}(z) = \frac{z + 1}{z} \quad \text{and} \quad G_1(z) = G_{11}(z)\cdot H_{12}(z) \quad \text{where} \quad G_{11}(z) = \frac{z - 1}{z}.
\]
Each of the functions is composed of one first order section and one biquadratic section. For an effective implementation, the cascading is made, so that the biquadratic section were followed by the first order section. It is necessary to note that the input signal of the biquadratic section should be sampled in the first phase and held during the second phase for a proper function (see Fig. 9). In order to maximize a dynamic range, the gain of both transfer functions should be divided in the rate $K \pm 1.23$ for $\alpha = 0.5$. Thus, the first order transfer functions ($H_{01}$, $H_{11}$) should be multiplied by the factor $K$, while the second order functions ($H_{02}$, $H_{12}$) should be divided by this factor [1].

The $-H_{01}$ and $-G_{01}$ functions can be realized by the network in Fig. 8 which has been newly synthesized. The $-H_{11}$ and $-G_{11}$ functions are the transfer functions of a differentiator which can be implemented according to [14] by the circuit presented in Fig. 8. Biquadratic functions are realized by a simplified Fleischer-Laker biquad [14] shown in Fig. 8.

The transfer functions and normalized values of the capacitors were derived in [1]. The block diagram of the filter bank implementation is shown in Fig. 9. The control signals of all the switches are derived from the main clock signal $f_c$: $f_s = f_c \cdot f_{2c}$, where $f_{2c} = f_c/2$, $f'_s = f_c + f_{2c}$, consequently the frequencies of the signals $f_c$ and $f'_s$ are one half of the $f_c$ signal frequency [1].

![Block diagram of an implemented SC filter bank.](image)

The control signals are derived from the main clock signal $f_c$. The synthesis filter bank can be realized similarly to the biquadratic sections and all derivations were made in Maple package [15]. A symbolic analysis and all derivations were made with the PracCan program with a PraCAn package [15].

4. Implementation Results

The designed filter bank was realized by the above mentioned circuit diagrams. The part values for the implementation are used in the following tables.

![Circuit diagrams.](image)

![Noninverting (a) and inverting (b) S&H circuits.](image)

![Input S&H (a) and output summator (b) realization circuits.](image)

![Capacitance values for the implementation of the transfer functions.](image)

![Capacitance values for the implementation of the transfer functions.](image)

![Capacitance values for the implementation of the biquads.](image)

2 Operators "·" and "+" are used as binary operations.
The component values of the S&H and output summa-
tor circuits (Figs. 10 and 11) are: \( C = 100 \, \text{pF} \) for the capacitor and \( R = 10 \, \text{k}\Omega \) for the resistances.

The resulting structure of the filter bank was verified by
the analysis performed by the WinSpice program [17], [16]
and the ELDO simulator of Mentor Graphics development
environment [18].

The simulation of the filter bank was provided by the
transient analysis followed by the Discrete Fourier Trans-
form (DFT), as stated in [16]. The simulations were pro-
vided with the following simulator settings: rettol = 1e-1,
trtol = 4, chgtol = 1e-16 and method = gear. The capac-
tances were modeled by the ideal capacitors with leakage
resistors. The switches were modeled by their resistances
both in on-state and off-state. The charge injections of the
switches were modeled by the overlapping capacitors.

The simulated impulse response obtained by the ELDO
simulator with LT1055 OpAmp models is shown in Fig. 12.

The impulse response corresponds to the ideal impulse
response given by the inverse \( Z \) transform of the whole filter
bank transfer function \( T_F(z) \) according to relation (7)

\[
h(n) = 2\delta(n-1)(n) - \frac{3}{\sqrt{2}} \left( \frac{1}{2} \right)^n 2^n \sin \left( \frac{\pi n}{2} \right)
\]

(12)

where \( n \) is a natural number and \( \delta(n-1) \) is the unit impulse
delayed by one sample.

The differences from the ideal response are evident es-
pecially during the switching. The glimmers in the time re-
sponse are caused by the dynamic properties of the OpAmp
used in this case. These errors show the influence on the
computed frequency response. The frequency response of
the filter bank is calculated from the impulse response using
DFT. The setting of the transient analysis and DFT param-
eters are pivotal for the validity of the whole analysis [16].
The simulations were realized by means of various spice models
of OpAmp in order to show the impact of its properties on the
frequency response. However, many OpAmp models cause
a non-convergence of the simulation.

From our experience, big influence on the convergence
of the simulation is caused by the OpAmp model. The simu-
lations with the help of OpAmp models based on the
Boyle model [19] usually converge. The models based
on [22] must be usually modified. Most problems
with the simulation convergence are caused by the noise
sources usually located in series in input pins. For
low-noise OpAmps, the noise sources can be neglected.

The frequency response of the filter bank with
LT1055 [21] OpAmp model [21] is shown in Figs. 4
and 14. The results obtained from the ELDO simu-
lator and the Winspice program are nearly the same.
The differences between the ideal and the simulated magnitude frequency responses are less than 0.5 dB.

The magnitude frequency response of the filter bank calculated by the WinSpice program with the help of AD8033 OpAmp model [24], [23] is shown in Fig. 15. The shape of the frequency response is dependent on the used OpAmp, as show in Figs. 4 and 15. Significant differences are evident at the frequency near 4 kHz, where the transfer functions of both branches are the most sensitive.

Complete analyses were realized by real models affecting all the essential nonlinearities (including nonlinearities of the OpAmp and dynamic characteristics, a charge injection of the switches etc.). The analyses confirm a filter bank design and the possibility of the SC implementation with a special type of an integrated circuit.

5. Conclusion

This paper presents a design of a two-channel maximally decimated IIR filter bank and its implementation by SC circuits. The implementation confirms that the main characteristics of the digital filter bank are preserved. The SC filter bank uses the decimation of a discrete-time analog signal similarly to the original digital filter bank. Appropriate transfer functions of the third-order elliptic IIR filters and their implementation using an SC technique is described. Used SC circuits were simulated with real characteristics of the used components.

The simulations and all derivations were performed by the Maple program, the simulations of the idealized circuits with a PraCan package. The analysis of real circuit structures was performed by the WinSpice program and the ELDO simulator of Mentor Graphics development environment. The comments on the simulation convergence and here used OpAmp model structures are presented. Obtained results are in agreement with the theoretical derivations. The suggested approach enables a low-cost and robust implementation of the filter bank by means of the SC circuits.

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