A 0.18µm CMOS DDCCII for Portable LV-LP Filters

Vincenzo STORNELLI, Giuseppe FERRI

Dept. of Industrial and Information Engineering and Economics, University of L'Aquila,
via Gronchi 18, 67100 L'Aquila, Italy

vincenzo.stornelli@univaq.it, giuseppe.ferri@univaq.it

Abstract. *In this paper a current mode very low voltage (LV) (1 V) and low power (LP) (21 µW) differential difference second generation current conveyor (CCII) is presented. The circuit is developed by applying the current sensing technique to a fully balanced version of a differential difference amplifier (DDA) so to design a suitable LV LP integrated version of the so-called differential difference CCII (DDCCII). Post-layout results, using a 0.18µm SMIC CMOS technology, have shown good general circuit performances making the proposed circuit suitable for fully integration in battery portable systems as, for examples, fully differential Sallen-Key bandpass filter.*

Keywords

Current mode filters, low voltage, low power, CCII.

1. Introduction

Recently, the low voltage low power analog circuit design has gained much more attention [1], [2]. In this perspective, the current mode (CM) approach offers the inherent advantages of wide bandwidth, high slew-rate, low power consumption and, most important, simple circuitry and consequently low chip area occupation [3], [4]. Stepwise, the current-mode technique has emerged as an attractive method for the design of active filters as, for example, video frequency continuous time filters, used for disk drivers, video signal processing and both intermediate frequency (IF) and base band (BB) receiver sections [5], [12]. Concerning the current mode approach, the most versatile building block is the second generation current conveyor (CCII) that, since its introduction, has been used in a wide range of applications; moreover, several circuit architectures have been proposed for its implementation [4]. The CCII is basically a single ended device; however, modern high performance analog integrated circuits incorporate also fully differential signal paths, as in direct conversion wireless transceiver, in order to achieve immunity to digital noise and power supply noises, larger output dynamic range, higher design flexibility and reduced harmonic distortion. For all these reasons, a number of fully differential versions of the CCII have been presented in the literature [13-20] but, due to the continuous technological scaling and increasing request of LV and LP portable systems, there is always a great request for improved CCII based differential circuit topologies. In this paper, a LV (1 V) LP (21 µW) 0.18µm CMOS fully differential second generation current conveyor based on a differential difference amplifier (DDCCII*)* is proposed and its application for a Sallen-Key band pass filter is given showing its feasibility for LV and LP battery supplied portable applications.

2. The Differential Difference Second Generation Current Conveyor

The CCII is a three terminal single ended device, whose node relations are expressed in (1), represented symbolically in Fig. 1. It can be implemented, as shown in Fig. 2, by applying the current sensing technique to op-amp based analog buffers.

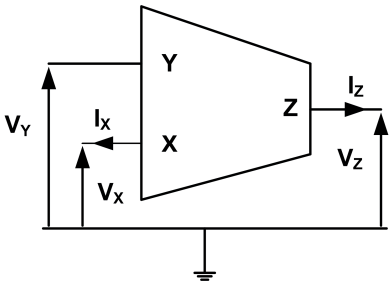

Fig. 1. CCII block scheme.

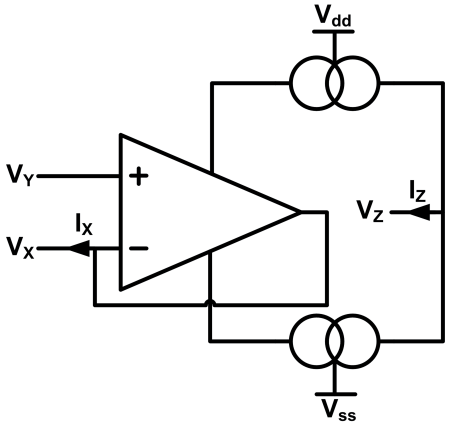

Fig. 2. Current sensing based CCII implementation block scheme derived from op-amp based configurations.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}. \quad (1)$$

The DDCCII is an evolution of the basic CCII and presents the advantages both of the CCII and of the differential difference amplifier (DDA) [7] such as larger signal bandwidth, greater linearity, wider dynamic range, simple circuitry, low power consumption, high input impedance and arithmetic operation capability. The DDA, whose block scheme is shown in Fig. 3, is a five-terminal device. It has two differential input ports, ($V_{pp} - V_{pn}$) and ($V_{np} - V_{nn}$) and a single-ended or differential output. The output of the DDA can be expressed as:

$$V_0 = V_{0p} - V_{0n} = A_0\left[\left(V_{pp} - V_{pn}\right) - \left(V_{np} - V_{nn}\right)\right]. \quad (2)$$

As the finite open-loop gain A_0 is low, the difference between the two differential voltages increases. Therefore, the open-loop gain is required to be as large as possible to improve circuit performance.

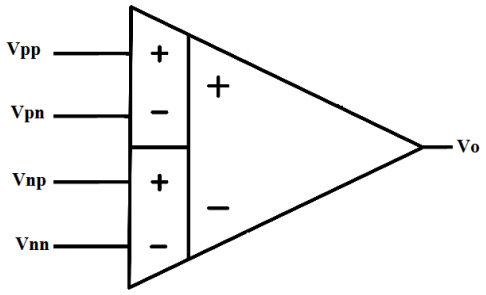

Fig. 3. DDA block scheme.

At circuit level, as well as the op-amp, the *DDA* consists mainly of two stages: a differential-input stage (differential pair with active load) and a second stage that typically is a gain stage for achieving high open loop gain. In order to reduce the circuit branches, so the static power consumption, it can be considered the theory developed in [5], where it has been demonstrated that, for not-high open-loop gains, it is better to use a current mode approach instead of classical op-amp based circuits in the implementation of high accuracy amplifiers. In order to simplify the circuit topology and lower the power consumption, in this work the second gain stage of the DDA has been substituted directly by a buffer. In this manner a fully differential DDA based CCII (DDCCII), with common mode control, whose block scheme and basic internal implementation are shown in Fig. 4, has been developed.

Fig. 5a shows the circuit schematic of the proposed DDCCII at transistor level, designed in a standard 0.18µm SMIC CMOS technology, while in Fig. 5b its layout implementation is reported; the occupied area (circled in the picture, without die pads) is about 0.04 mm^2. The gate terminals of the double cross coupled input transistors (M_1-M_4), together with their active load (M_5-M_6), are DDCCII Y_1 and Y_2 high impedance terminals, while X_1 and X_2 terminals, obtained at M_{21} and M_{22} sources, are low

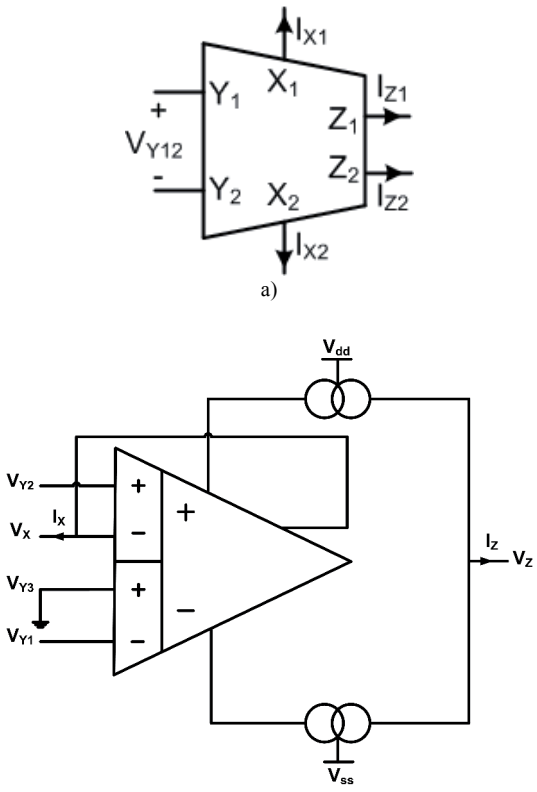

Fig. 4. a) DDCCII basic block scheme; b) DDA based DDCCII basic internal implementation.

impedance nodes (thanks to the negative feedback). More in detail, the differential input voltage V_{Y12} applied across Y_1 and Y_2 terminals is mirrored to a differential voltage V_{X12} ($V_{X12} = V_{Y12}$) while the currents flowing in the X_1 and X_2 terminals are conveyed to Z_1 and Z_2 terminals (i.e. $I_{Z1} = I_{X1}$ and $I_{Z2} = I_{X2}$) thanks to (M_{19}-M_{20}) and (M_{23}-M_{24}) current mirrors operations. Finally, Z_1 and Z_2 terminals are high impedance nodes suitable for current outputs. A traditional CMFB circuit consisting of transistors (M_{15}-M_{18}) and resistors (R_2-R_3) has been employed to fix the common-mode output voltage at middle supply level, so to avoid the common-mode voltage output drift. In Tab. 1 the designed DDCCII transistor dimensions are reported. With respect to previously published works [13-20] in this paper a very LV and LP portable DDCCII is presented with good general performances and a relatively simple implementation so reducing also the occupied silicon area: the circuit operates at a supply voltage equal to 1 V while its standby current is only 21 µA. Generally, the terminal characteristics of the DDCCII are specified by the voltage and current transfer functions: the voltage following characteristic between ports Y-X and the current following characteristic between ports X-Z. Fig. 6a shows the simulated differential DC voltage transfer characteristics $V_{Y12} \rightarrow V_{X12}$ while Fig. 6b shows the simulated DC current characteristics at X and Z nodes. The two curves are almost overlapped being the voltage and current gain greater than 0.98. Finally, Tab. 2 summarizes the DDCCII performances showing the voltage and current gain transfer constants.

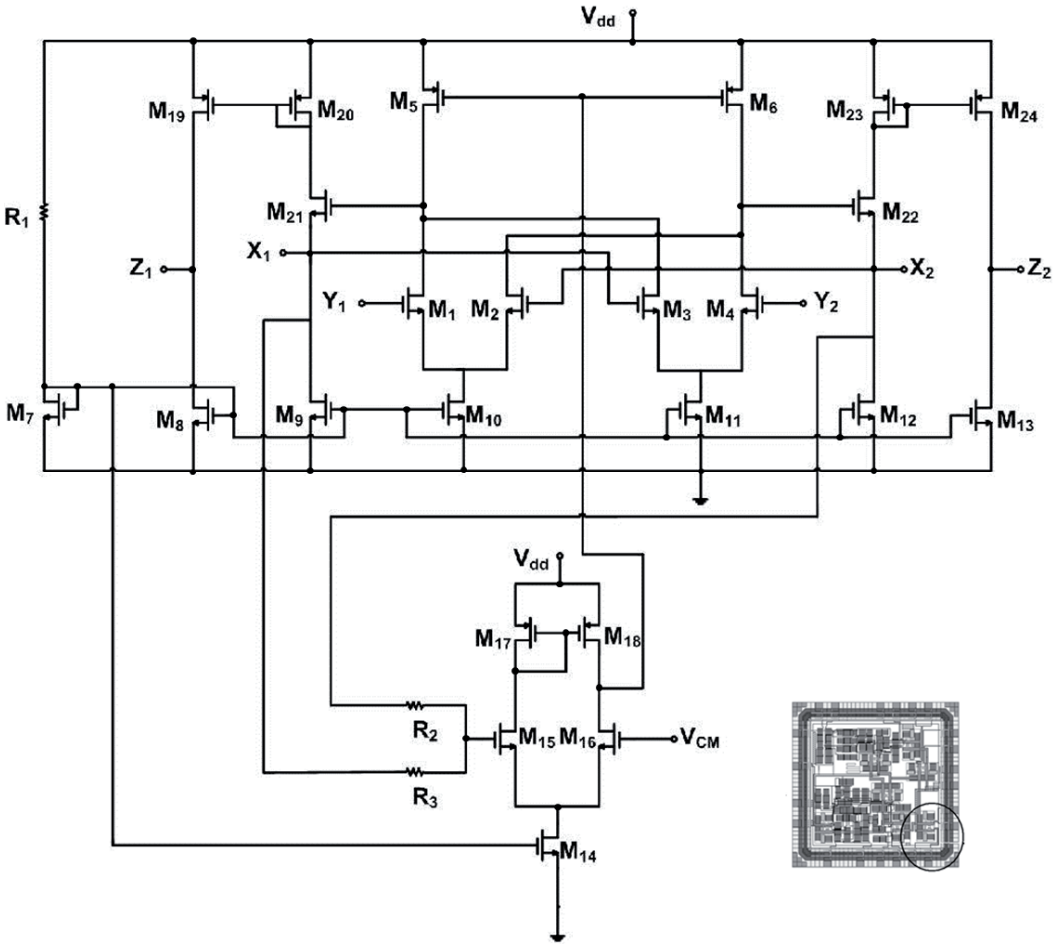

Fig. 5. Designed DDCCII at schematic level a) and micrograph of the layout implementation (circled area, b).

	Transistor	W [μm]	L [μm]
DDCCII transistor dimensions	M_1-M_4,	100	0.18
	M_5, M_6, M_{17}, M_{18}, M_{21}, M_{22}	60	0.18
	M_{10}, M_{11}, M_{14}	20	0.18
	M_7, M_8,M_9, M_{12}, M_{13}	10	0.18
	M_{19}, M_{20}, M_{23}, M_{24}	20	0.18
	M_{15}-M_{16}	200	0.18

Tab. 1. DDCCII transistor dimensions.

Circuit	DDCCII
Voltage supply	1V
Power Consumption	21 μW
3dB Bandwidth	11 MHz
Voltage Gain (α)	0.98
Current Gain (β)	0.98
Output Systematic offset	200 μV
Input dynamic range	700 mV_{pp}
X Parasitic Resistance	0.4 Ω
Z Parasitic Resistance	0.4 MΩ
Layout area	0.04 mm^2

Tab. 2. DDCCII main characteristics.

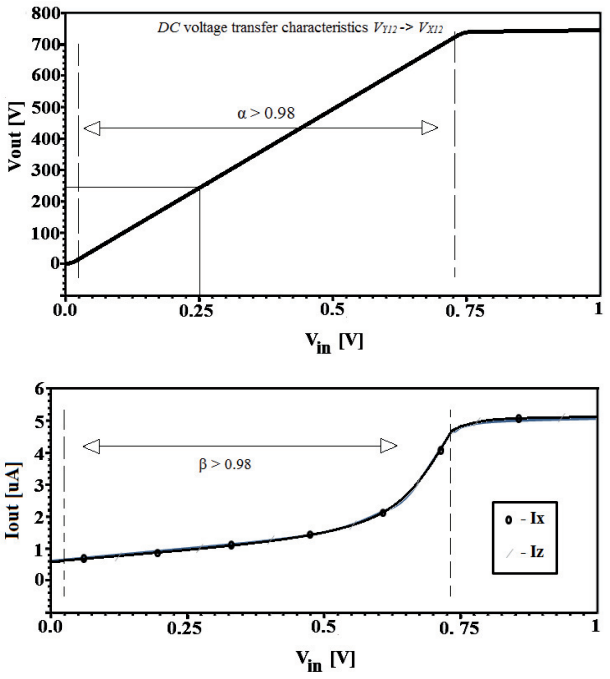

Fig. 6. a) Simulated DC voltage transfer characteristics $V_{Y12} \rightarrow V_{X12}$. b) Simulated DC current characteristics at X and Z nodes.

3. Filter Application

As a feasibility demonstration application example, the DDCCII has been used for designing a fully differential version of a second order Sallen-Key bandpass filter, implemented using only one active element. Continuous time CMOS bandpass filters, especially with tunable center frequency, quality factor and gain, are fundamental blocks in portable wireless heterodyne receivers and in many signal processing applications. The implemented second order filter architecture is shown in Fig. 7. A straightforward circuit analysis gives the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-\frac{R_3}{R_2 R_1 C_1} s}{s^2 + \frac{s}{R_2}\left(\frac{C_1 + C_2}{C_1 C_2}\right) + \frac{1}{R_2 R_1 C_1 C_2}} . \quad (3)$$

From (3), if $C = C_1 = C_2$, the filter center frequency ω_0, the quality factor Q and the gain A are given respectively by:

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2} C} , \quad (4)$$

$$Q = \frac{1}{2}\sqrt{\frac{R_2}{R_1}} , \quad (5)$$

$$|A| = \frac{1}{2}\frac{R_3}{R_1} . \quad (6)$$

Therefore, through a suitable choice of R_1 and R_2 values, it is possible to achieve high Q factors, while, regulating C values, it is possible to allow the center frequency tuning without varying the Q factor. This can be done in a discrete step mode adding switched elements or in a continuous mode by using, for example, varicap diodes and MOS resistive based resistors (MRC). Thanks to the current mode approach, also the filter gain can be controlled orthogonally from quality factor and center frequency, by changing R_3. Fig. 8 shows the simulated frequency response at three different filter gains (the following values have been used for passive components: $C_1 = C_2 = C =$ = 50 pF; $R_1 = 1$ kΩ; $R_2 = 100$ kΩ; $R_3 = 200$ Ω; $R_{3s} = 1$ kΩ; $R_{3s1} = 10$ kΩ); in this case the center frequency is about 280 kHz, the quality factor is fixed about to 5, the gain has been tuned from -17 to 12 dB in three steps by adding shunt switched resistors (using simple transistor as switches) to R_3 (R_{3S}) and R_2 (R_{3S1}). Finally, Tab. 3 summarized the main filter performance.

Filter linearity has been also evaluated, for the proposed example, in terms of its total harmonic distortion (THD) at 280 kHz and 0 dB gain as shown in Fig. 9. Post-layout results have also shown good general circuit performance in terms of temperature and process variations, making the design circuit suitable for fully integration in any kind of battery supplied portable system.

Circuit	Sallen-Key second order bandpass filter
Allowed filter tuning range	10 kHz ÷ 2 MHz
Simulated tuned voltage gain range	-30 dB ÷ +30 dB
Simulated tuned quality factor range	2 ÷ 30
Tuning voltage for filter gain control (Sw1 and Sw2)	Digital 0-1V

Tab. 3. DDCCII based filter main characteristics.

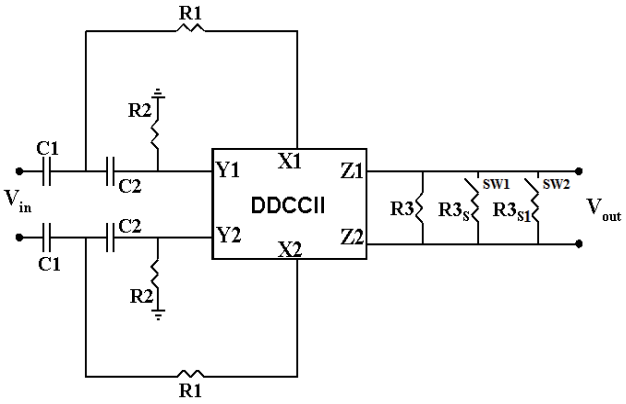

Fig. 7. Second order Sallen-Key tunable current mode bandpass filter.

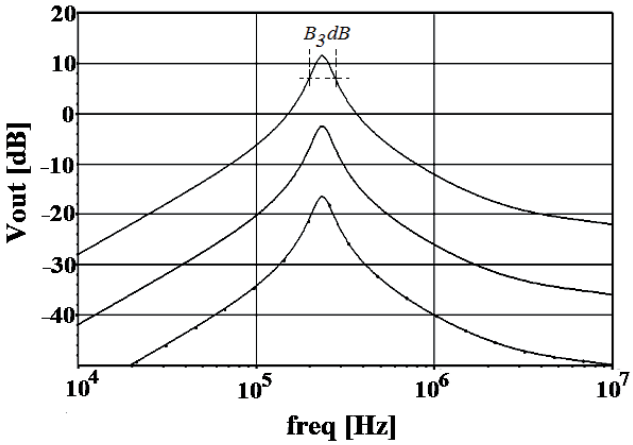

Fig. 8. Simulated filter frequency response, with a fixed designed center frequency, for three different filter gains.

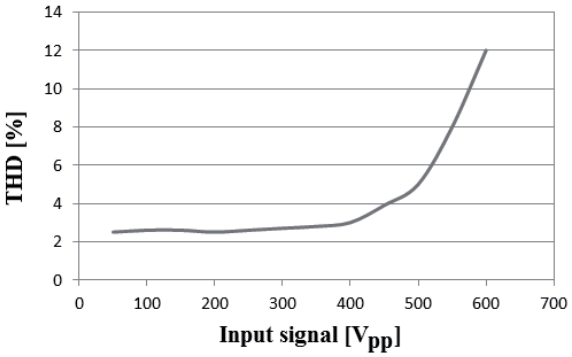

Fig. 9. Designed filter THD simulated at 280 kHz and 0 dB filter gain.

4. Conclusion

In this work a SMIC 0.18μm CMOS technology LV and LP DDCCII topology has been presented and discussed. The DDCCII operation has been obtained by applying the current sensing technique to a fully balanced version of a differential difference amplifier (DDA). As a feasibility demonstration, the DDCCII has been used for designing a fully differential version of a second order Sallen-Key bandpass filter showing very good general performance in agreement with theoretical expectations.

References

[1] VITTOZ, E. A. Low power circuit design: fundamentals and limits. In *IEEE International Symposium on Circuits and Systems*. May 1993, vol. 2, p. 1439 – 1442.

[2] STORNELLI, V. Low voltage low power fully differential buffer. *Journal of Circuits, Systems, and Computers (JCSC)*, 2009, vol. 18, no.3, p. 497-502.

[3] FERRI, G., STORNELLI, V., DI SIMONE, A. A CCII-based high impedance input stage for biomedical applications. *Journal of Circuits, Systems, and Computers (JCSC)*, Dec. 2011, vol. 20, no. 8, p. 1441-1447.

[4] FERRI, G., STORNELLI, V., FRAGNOLI, M. An integrated improved CCII topology for resistive sensor application. *Analog Integr. Circuits Signal Process.*, 2006, vol. 48, p. 247-250.

[5] FALCONI, C., FERRI, G., STORNELLI, V., DE MARCELLIS, A., D'AMICO, A., MAZZIERI, D. Current mode, high accuracy, high precision CMOS amplifiers. *IEEE Transactions on Circuits and Systems II*, May 2008, vol. 55 no. 5.

[6] MINAEI, S., CICEKOGLU, O. A resistorless realization of the first-order all-pass filter. *International Journal of Electronics*, 2006, vol. 93, no. 3, p. 177-183.

[7] KESKIN, D., BIOLEK, D., HANCIOGLU, E., BIOLKOVA, V. Current-mode KHN filter employing current differencing transconductance amplifiers. *International Journal of Electronics and Communications (AEU)*, 2006, vol. 60, no. 6, p. 443-446.

[8] HERENCSAR, N., KOTON, J., JERABEK, J., VRBA, K., CICEKOGLU, O. Voltage-mode all-pass filters using universal voltage conveyor and MOSFET-based electronic resistors. *Radioengineering*, 2011, vol. 20, no. 1, p. 10-18.

[9] KOTON, J., HERENCSAR, N., VRBA, K. KHN-equivalent voltage-mode filters using universal voltage conveyors. *AEU International Journal of Electronics and Communications*, 2011, vol. 65, no. 2, p. 154-160.

[10] MINAEI, S. Electronically tunable current-mode universal biquad filter using dual-X current conveyors. *Journal of Circuits, Systems, and Computers*, 2009, vol. 18, no. 4, p. 665-680.

[11] YÜCE, E., MINAEI, S. On the realization of high-order current-mode filter employing current controlled conveyors. *Computers & Electrical Engineering,* 2008, vol. 34, no. 3, p. 165-172.

[12] HORNG, J. W., HOU, C. L., CHANG, C.M., CHUNG, W.Y., LIN, C.T., SHIU, I.C., CHIU, W. Y. First-order all pass filter and sinusoidal oscillators using DDCCs., *International Journal of Electronics*, 2006, vol. 93, no. 7, p. 457-466.

[13] ALZAHER, H., ELWAN, H., ISMAIL, M. A CMOS fully balanced second-generation current conveyor. *IEEE Trans. Circuits Syst. II*, 2003, vol. 50, p. 278–287.

[14] MAHMOUD, S. A., HASHIESH, M. A., SOLIMAN, A. M. Digitally controlled fully differential current conveyor. *IEEE Trans. Circuits Syst*. I, 2005, vol. 52, no. 10, p. 2055–2064.

[15] ALZAHER, H., ELWAN, H., ISMAIL, M. CMOS fully differential second-generation current conveyor. *Electronics Letters*, June 2000, vol. 36, no. 13, p. 1095-1096.

[16] CHANG, C.M., AL-HASHIMI, B.M., WANG, C.L., HUNG, C.W. Single fully differential current conveyor biquad filters. *IEE Proceedings of Circuits Devices and Systems*, 2003, vol. 50, no. 5.

[17] MAHMOUD, S. A., HASHIESH, M. A., SOLIMAN, A. M. Low-voltage digitally controlled fully differential current conveyor. *IEEE Transactions on Circuits and Systems I*, 2005, vol. 52, p. 2055–2064.

[18] SOLIMAN, E. A., MAHMOUD, S. A. New CMOS fully differential current conveyor and its application in realizing sixth order complex filter. In *IEEE International Symposium on Circuits and Systems*, 2009, vol. 1, p. 57–60.

[19] MAHMOUD, S. A. New fully-differential CMOS second-generation current conveyor. *ETRI Journal*, Aug. 2006, vol. 28, no. 4, p. 495- 501.

[20] CHEN, H. P. Voltage-mode DDCC-based multifunction filters. *Journal of Circuits, Systems, and Computers (JCSC)*, 2007, vol. 16, no. 1, p. 93-104.

About Authors …

Vincenzo STORNELLI was born in Avezzano, Italy. He received the ''Laurea'' degree (cum laude) in Electronic Engineering in 2004. In October 2004, he joined the Department of Electronic Engineering, University of L'Aquila, L'Aquila, Italy. In February 2008 he received the Ph.D. in Microelectronics in the same university, where he is actually involved, as Aggregate Professor, with problems concerning low voltage and low power current mode applications; physics-based simulation; computer-aided design modeling characterization and design analysis of active microwave components, circuits, and subsystems; and the design of integrated circuits for RF and sensor applications. He is also a Consultant for the Radio Frequency Technology Laboratory, Thales Italia, Chieti, Italy, and serves as a reviewer for several international journals. His research interests include several topics in computational electromagnetics, including microwave antenna analysis for outdoor ultrawideband applications.

Giuseppe FERRI was born in L'Aquila, Italy, in 1965. He received the ''Laurea'' degree in Electronic Engineering from the University of L'Aquila in 1988. He is currently with the Department of Electrical Engineering and Information Engineering, University of L'Aquila, where he was a Researcher from 1991 to 2001 and has been an Associate Professor of Electronics since 2001. In 1993, he was a Visiting Researcher with SGS-Thomson Milano, Milan, Italy, where he worked on bipolar low-voltage op-amp design. From 1994 to 1995, he was a Visiting Researcher with Katholieke Universiteit Leuven, Leuven, Belgium, where he worked on low voltage CMOS design with Prof. W. Sansen's group. He is responsible for the group dedicated to integrated circuit analog design and for the Euro-

practice contract for the University of L'Aquila. He is a coauthor of the book entitled Low Voltage, Low Power CMOS Current Conveyors (Kluwer, 2003) and four textbooks in Italian on analog microelectronics (in 2005 and 2006). He is also the author or coauthor of more than 300 scientific works in international journals and a speaker at national and international conferences. He is an Associate Editor for the Journal of Circuits, Systems, and Computers. His research interests are the design of voltage- and current-mode analog integrated circuits for portable applications (e.g., sensors and biomedicals) and circuit theory. Prof. Ferri serves as a reviewer for numerous journals (such as the IEEE Transactions on Circuits and Systems I and II, Analog Integrated Circuits and Signal Processing, and the ETRI Journal) and international conference proceedings. He has been a coorganizer of international (Eurosensors 1991, International Meeting on Chemical Sensors 1994, and International Symposium on Industrial Electronics (ISIE) 2002) and Italian conferences (Associazione Italiana Sensori e Microsistemi 1995, 1996, and 1997). He was also the Publication Chairman for the ISIE 2002 Conference.