DTMOS-Based 0.4V Ultra Low-Voltage Low-Power VDTA Design and Its Application to EEG Data Processing

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Abstract. *In this paper, an ultra low-voltage, ultra low-power voltage differencing transconductance amplifier (VDTA) is proposed. DTMOS (Dynamic Threshold Voltage MOS) transistors are employed in the design to effectively use the ultra low supply voltage. The proposed VDTA is composed of two operational transconductance amplifiers operating in the subthreshold region. Using TSMC 0.18μm process technology parameters with symmetric ±0.2V supply voltage, the total power consumption of the VDTA block is found as just 5.96 nW when the transconductances have 3.3 kHz, 3 dB bandwidth. The proposed VDTA circuit is then used in a fourth-order double-tuned band-pass filter for processing real EEG data measurements. The filter achieves close to 64 dB dynamic range at 2% THD with a total power consumption of 12.7nW.*

Keywords

Ultra low-power, ultra low-voltage, DTMOS, VDTA, analog building blocks, EEG data processing.

1. Introduction

The demand for portable applications has continuously increased during the last decade. Smart phones, tablet computers, netbooks and several wireless devices are everywhere. However, this trend of ever-decreasing supply voltage levels of circuits for low power consumption have arisen the necessity to design analog circuits that are capable of operating under very low supply voltage levels. That severely limits the performance of analog circuits which share supply voltages with digital circuits. There is a strong need for new ideas and perspectives to analog circuit design to meet the requirements of modern electronic devices. Until now, especially in digital circuits, decreasing supply voltage levels for transistors having thinner gate oxides has been utilized as a solution to lower the power consumption and increasing chip density by laying out more transistors on a smaller chip area. However, further decreasing the channel lengths has created leakage current problems. Moreover, threshold voltages cannot be kept below certain limits to minimize the leakages in the chip. Conventional analog circuits suffer from very low supply voltages of digital circuits and relatively high threshold voltage levels to prevent large leakage currents in standard CMOS process technology.

As a solution to the problems of conventional circuits, DTMOS, dynamic threshold voltage metal oxide transistor was presented by Assederaghi et al. in [1] which operates as a low-leakage as well as low-voltage, low-power device. In this paper, we have used DTMOS transistors in our VDTA design to enable ultra low power, ultra low voltage operation under ±0.2 V symmetric supply voltages. Then, this design was applied to a fourth order double-tuned band-pass filter for EEG data processing [2], [3].

There are other low power filter designs in the literature [4-6]. For example, the filter circuit in [4] uses switched opamp, switched capacitor technique. Although it has 0.9 V supply voltage, the power consumption is 262 μW which can be considered quite large for ultra low power designs. The circuit in [5] uses g_m-C technique and consumes 230 nW but its supply voltage is 2.8 V and THD values are as high as 5%. More promising alternative was proposed in [6] however, in this circuit, 1V supply voltage was used. Our VDTA-based circuit, including DTMOS transistors, uses significantly lower supply voltage of ±0.2 V with a power consumption of only 12.7 nW.

2. DTMOS Transistor

DTMOS transistor shows high threshold characteristic when it is off to minimize the leakage and at the same, it behaves as a low threshold device for high current drivability under low voltage supplies. This feature makes it as a promising candidate for modern ultra low-voltage analog circuits. As shown in Fig. 1(a), a PMOS transistor's gate and body terminals are connected without requiring any additional processing steps and it can be produced in standard CMOS technology. DTMOS transistor and its commonly used circuit symbol are shown in Fig. 1.

This configuration although goes back to earlier dates [7-8] Assederaghi et al. extensively describe the device and

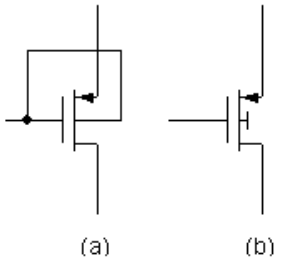

Fig. 1. DTMOS transistor and its circuit symbol.

express underlying reasons of its operation. The idea is to connect the gate and body of the device to dynamically change the threshold voltage of the transistor by utilizing the relation in (1).

$$V_{TH} = V_{TO} + \gamma\left(\sqrt{\left|2\Phi_F\right| + V_{SB}} - \sqrt{\left|2\Phi_F\right|}\right). \qquad (1)$$

DTMOS transistor, under the same V_{GS} voltage behaves as a high-transconductance MOSFET. As it is seen in Fig. 2, it conducts more current than a regular MOSFET. In the figure, V_{DS} kept at -0.1 V constant voltage while V_{GS} is swept from -0.4 V to 0 V. The reason behind this mechanism is the threshold voltage reduction due to the positive source body voltage.

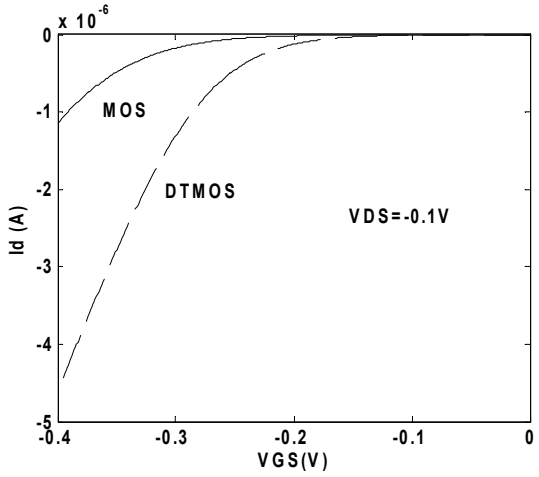

Fig. 2. DTMOS and standard MOS drain currents.

The main problem of such a connection is the possibility of very high forward biased junction currents of source body and drain body parasitic diodes. For this reason, DTMOS with its plain structure is not usable for supply voltages exceeding 0.7 V. Although it is possible to use it with an addition of an extra limiter transistor [1], this would almost double the chip area for digital circuits and additionally, it increases parasitic effects. Furthermore, the operation of all chip components strongly depends on those limiter transistors which decrease robust operation performance because any high on diode current totally disrupts transistor operation. For those reasons, supply voltages are chosen low enough to limit any forward biased diode currents in this study.

In the literature, transistors with source body junctions forward biased close to 0.4V~0.5V voltage levels are used without transistor operation being affected by the parasitic elements [9], [10]. The main reason is that the mobile carrier concentrations caused by parasitic elements for supply voltages less than 0.5 V do not reach high levels in modern highly doped bodies to affect the overall transistor operation.

Another question might arise that if the conventional MOSFET models are sufficient for proper modeling the operation the DTMOS transistor. Actually, mostly used MOSFET models such as BSIM, EKV are developed under the assumption that the channel is free of mobile carriers, which is the total depletion approximation. However, for a DTMOS transistor, this is not the case because there are mobile carriers and total depletion approximation is not valid now. Additionally, vertical drain body and source body junction currents add another dimension and this might require two dimensional device models. However, these are not necessary if the supply voltage is kept below 0.4V~0.5V voltage levels and the device channel length is not chosen very small to prevent short channel effects. Conventional models are still applicable to DTMOS transistor to model the device and the related circuits provided that the mentioned specifications exist [11], [12]. Therefore, we have used 0.4V supply voltage and transistors with minimum channel lengths 2 μm in our designs to be in agreement with results and compact models experimentally proven in [11-13].

3. VDTA Element

Voltage differencing transconductance amplifier (VDTA) has voltage inputs, an alternative of current differencing transconductance amplifier (CDTA) where the inputs are currents [14], [15]. These voltage inputs result in new propositions to conventional circuit solutions for analog signal processing [16]. The circuit symbol is given in Fig. 3 and its definition relations are shown in matrix form in (2).

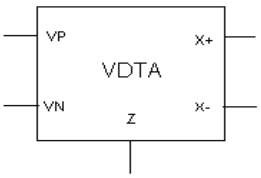

Fig. 3. VDTA element's circuit symbol.

The voltage difference of input terminals is multiplied by a transconductance of g_{m1} which becomes the I_Z current that is flowing over the impedance at the Z terminal forming the voltage at Z terminal. This voltage is then multiplied by positive and negative $\pm g_{m2}$ transconductances to form the output $\pm I_X$ currents. VDTA element can be generated by connecting two OTA circuits in a cascaded fashion.

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_{VP} \\ V_{VN} \\ V_Z \end{bmatrix}. \qquad (2)$$

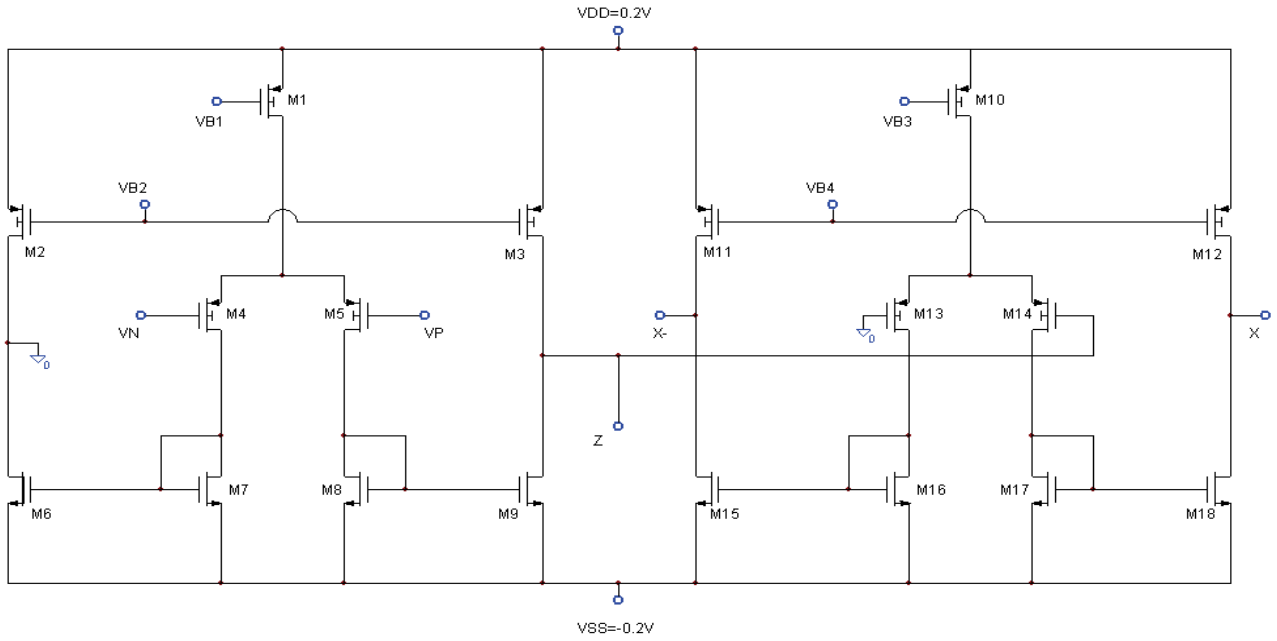

Fig. 4. The proposed DTMOS-based ultra low-voltage ultra low-power VDTA circuit.

DTMOS-based ultra low-voltage, ultra low-power proposed VDTA circuit is illustrated in Fig. 4. The transistors from M1 to M9 constitute the first OTA and the transistors from M10 to M18 constitute the second OTA where the transistors from M1 to M5 are DTMOS and similarly in the second part the transistors from M10 to M14 are DTMOS. These DTMOS transistors efficiently use available voltage headroom under the ultra low supply voltage of ±0.2 V.

In an n-well standard CMOS process, PMOS transistors can be connected as DTMOS transistors whereas NMOS transistors share a common well in an n-well process and their body terminals cannot be connected to their gates to generate NMOS DTMOS transistors. That requires expensive triple-well processes using deep n-wells to produce NMOS transistors with their own wells. This restriction limits the overall performance of the proposed circuit where most of the voltage headroom is consumed over the NMOS transistors. As a result, strong inversion operation and high frequency applications are not possible using this circuit. Therefore the transistors in this circuit are biased in weak inversion where a MOS transistor's drain current is given by

$$I_D = I_S\left(\frac{W}{L}\right)\exp\left(q\frac{V_{GS}-V_{TH}}{nkT}\right)\left[1-\exp\left(-q\frac{V_{DS}}{kT}\right)\right]. \quad (3)$$

If $V_{DS} \geq 3kT/q$, the transistor will saturate in weak inversion [17]. The transconductance g_m is described by

$$g_m = q\frac{I_D}{nkT} \quad (4)$$

where the parameters in (3) and (4) have their usual meanings.

Using TSMC 0.18µm BSIM3v3.2 process parameters, PSPICE gives $g_{m1} = g_{m2} = 54$ nA/V for the proposed VDTA circuit when the transistor dimensions in Tab. 1 are used. As it is seen in Fig. 4, there are four biasing voltages in the design of the VDTA circuit. For our application, we have found that using the ground reference voltage level for those biasing voltages are possible. Grounding the biasing voltages prevents the necessity of additional circuitry so we have used $VB1 = VB2 = VB3 = VB4 = 0$ V. Total power consumption of the proposed VDTA circuit is given by PSPICE as just 5.96 nW which is a suitable value for ultra low-power operation.

Transistors	Width	Length
M1, M2, M3, M10, M11, M12	5µm	2 µm
M4, M5, M13, M14	300 µm	2 µm
M7, M8, M16, M17	50 µm	5 µm
M6, M9, M15, M18	100 µm	5 µm

Tab. 1. The proposed VDTA circuit transistor dimensions.

Technology	TSMC 0.18µm
Supply Voltage	±0.2 V
Input Voltage Range	-170 mV - 60mV
Power Consumption	5.96 nW
Transconductances (g_{m1}= g_{m2})	54 nA/V
Transconductance 3dB Frequency	3.3 kHz
Input Resistance @300Hz	628 MΩ
Output Resistance@300Hz	1.85 GΩ

Tab. 2. Performance summary of the proposed VDTA.

In Fig. 5, input and output characteristic of the VDTA circuit are shown. VDTA was connected in a feedback configuration and the z terminal was loaded with a 1nF capacitor. It is found that the range that input voltage swing

is between -170 mV to 60 mV under ±200 mV supply voltages. VDTA transconductance $g_m = g_{m1} = g_{m2}$ is depicted in Fig. 6 where it is found approximately as 54 nA/V with a 3dB bandwidth of 3.3 kHz. Performance summary of the proposed VDTA is tabulated in Tab. 2.

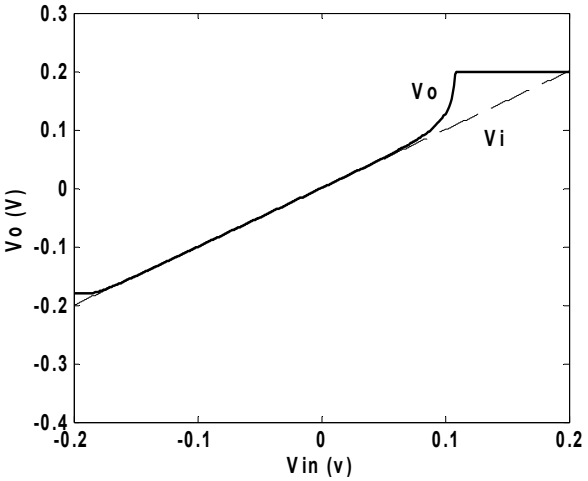

Fig. 5. The proposed VDTA's input and output characteristics.

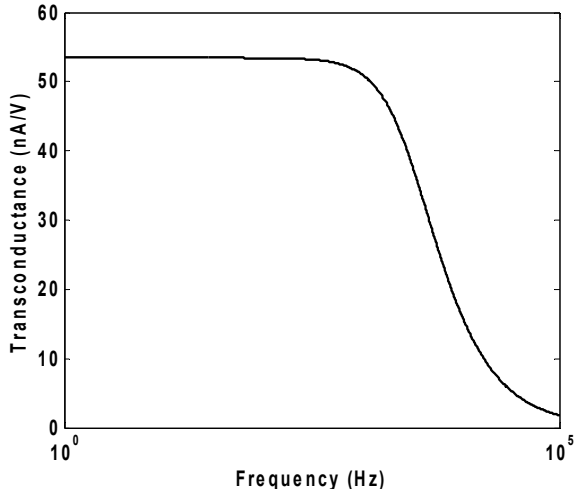

Fig. 6. The transconductance of the proposed VDTA.

4. VDTA-Based EEG Filter

EEG (Electroencephalography) is a commonly used way of recording brain electrical activity by connecting electrodes to scalp. It has a wide usage area in biomedical applications and plays an important role in diagnosing several brain disorders [18]. There is a need for low-voltage and low-power portable EEG processing circuits [19].

EEG data obtained by connecting electrodes to human scalp has very low-amplitude voltage signals in micro volts range which are amplified by an instrumentation amplifier and then unwanted frequency components are filtered out according to the application. In our study, we assume that the signals coming from scalp electrodes are applied to a low-noise instrumentation amplifier which sufficiently amplifies the signals with achieving required noise performance of EEG signals when the succeeding stages in the system have high noise characteristics.

The VDTA-based band-pass filters in [16] are used in this study. The fourth-order band-pass filter circuit is shown in Fig. 7.

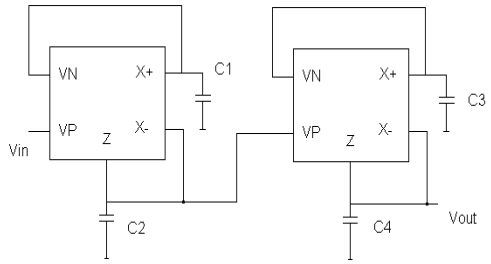

Fig. 7. VDTA-based double-tuned band-pass filter [16].

The double-tuned circuit is comprised of two band-pass filters which are tuned using two different pole frequencies. The transfer function of the filter in Fig. 7 is given in (5)

$$\frac{V_{out}}{V_{in}} = H_0 \frac{\frac{\omega_{p1}}{Q_{p1}} s}{s^2 + \frac{\omega_{p1}}{Q_{p1}} s + \omega_{p1}^2} \frac{\frac{\omega_{p2}}{Q_{p2}} s}{s^2 + \frac{\omega_{p2}}{Q_{p2}} s + \omega_{p2}^2} \tag{5}$$

where H_0 is the gain factor. Natural frequencies $\omega_{p1,2}$ and quality factors $Q_{p1,2}$ of the filter are determined according to the relations in the following equations.

$$\omega_{p1,2} = \sqrt{\frac{g_{m1,3} g_{m2,4}}{C_{1,3} C_{2,4}}}, \tag{6}$$

$$Q_{p1,2} = \sqrt{\frac{C_{2,4} g_{m1,3}}{C_{1,3} g_{m2,4}}}. \tag{7}$$

The non-ideal effects coming from the CMOS VDTA circuit such as parasitic capacitances and conductances modify the natural frequency and quality factor definitions as described in [16]. Parasitic capacitances appear at *VP*, *VN* inputs and *Z* terminal. Additionally, parasitic conductances occur at X+, X- and Z terminals.

The filter circuit was used in processing real EEG data measurements which will be explained in the next subsection. For our EEG application, the requirement was a fourth order band-pass filter with a pass-band between 4 Hz and 35 Hz. For the double tuned filter, we have used the pole frequency relations in [20] where B is the bandwidth and f_0 is the center frequency.

$$f_{p1} = \frac{\omega_{p1}}{2\pi} = f_0 + \frac{B}{2}\sin\left(45^0\right), \tag{8}$$

$$f_{p2} = \frac{\omega_{p2}}{2\pi} = f_0 - \frac{B}{2}\sin\left(45^0\right). \tag{9}$$

The EEG filter parameters, B = 31 Hz, f_0 = 19.5 Hz and $Q_{p1} = Q_{p2} = 1$ were chosen. The pole frequencies are f_{p1} = 30.45 Hz and f_{p2} = 8.54 Hz. To realize this pole frequencies, VDTA transconductances and capacitor values were determined according to the relations in (6) and (7) which give $C1 = C2 = 1.006$ nF, $C3 = C4 = 0.282$ nF when VDTA transconductances $g_{m1} = g_{m2} = g_{m3} = g_{m4} =$ =54 nA/V are chosen. Relatively large capacitors should be connected to the filtering circuit externally.

Double-tuned band-pass filter using the circuit in Fig. 4 was simulated using PSPICE program with above calculated passive element values. Ideal and simulated frequency responses of the filter are shown in Fig. 8. The deviation from the ideal one, after a few kHz frequencies, is caused by the proposed VDTA's bandwidth which is limited to a few kHz range because the transistors in the active circuit operate in weak inversion. Actually, there is a tradeoff between bandwidth and power consumption. High biasing currents bring higher bandwidth at the expense of high power consumption. Fortunately, for our EEG data filtering application our active block's bandwidth was quite sufficient and did not lead to any problems.

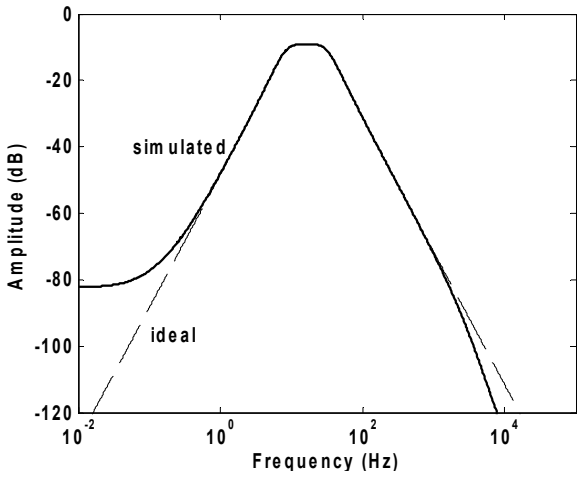

Fig. 8. Ideal and simulated frequency responses of the filter.

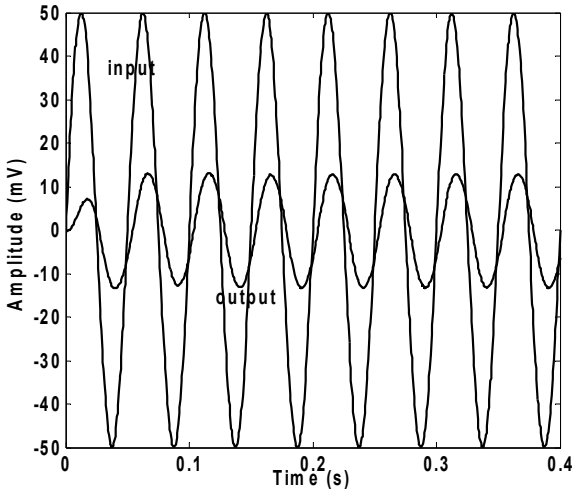

Fig. 9. Time response of the filter for a 20Hz, 100mV (p-p) input sine wave signal.

In order to investigate the time domain response of the double-tuned VDTA-based band-pass filter, an input sine wave with a frequency of 20 Hz and peak to peak amplitude of 100 mV is applied and the corresponding response in Fig. 9 is obtained. The decrease in the amplitude is actually the characteristic of the double-tuned filter design because two different intersections of the two band-pass filters to obtain double-tuned response cause an expected decrease in the amplitude which can be increased by an additional circuitry if necessary.

Temperature is an important factor for very low frequency filters with large time constants. Therefore, it is necessary to analyze the change of pole frequencies with respect to the change in temperature [21]. We have changed the temperature from its initial value of 27°C value to 40° and resulting amplitude and transient responses are shown in Fig. 10 and Fig. 11 respectively.

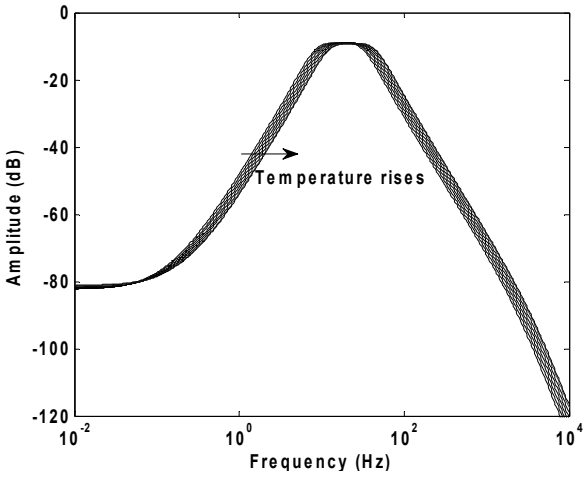

Fig. 10. Filter pole frequency change with temperature.

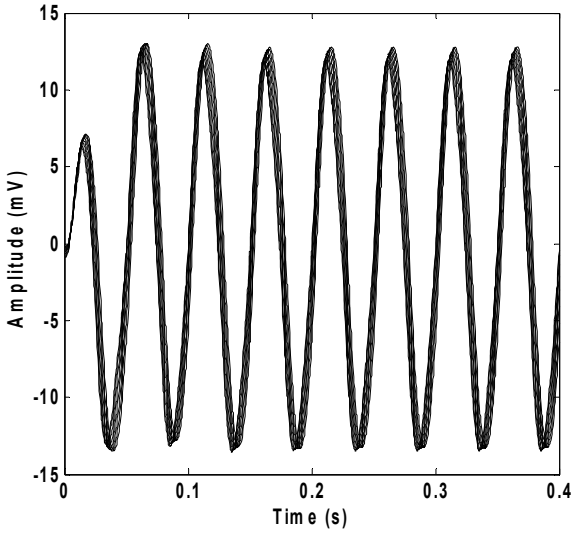

Fig. 11. Filter output transient response for the change in temperature.

Beyond this range, temperature drift of the center frequency slowly becomes significant and decreases transient amplitudes because of the drifted stop-band of the filter.

Nevertheless, the filter can be used under conditions or in environments requiring higher temperature change, if a compensation method is utilized to keep the center frequency in limits. One solution to resolve this problem was explained in [21]. Another solution might be off-chip tuning of pole frequencies of the filter.

THD of the proposed filter was calculated with PSPICE and the related results was depicted in Fig. 12 where the total harmonic distortion of the filter is less than 2% for inputs not exceeding 100 mV peak to peak voltage.

The noise is an important parameter in EEG signal processing where the signal voltage levels are so weak that the desired signal components might be lost in the measuring process if noisy equipment is used. To investigate the noise performance of the VDTA filter, PSPICE simulations are performed in the frequency range of interest. Over a 500Hz bandwidth rms noise voltage was found as 22.9 μV which is a significantly high value for EEG signal processing applications. This can be resolved by using, in the preceding stages, an instrumentation amplifier which has characteristically low noise level.

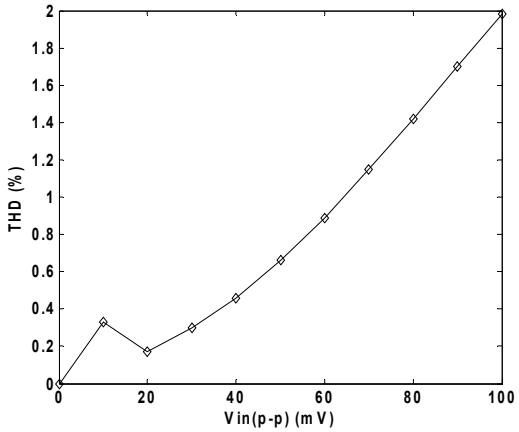

Fig. 12. Output THD of the filter with respect to input voltage.

Monte-Carlo simulations are performed with the help of PSPICE program to show the effects of process variation (W, L, t_{ox}, V_{TO}) on the filter amplitude characteristic.

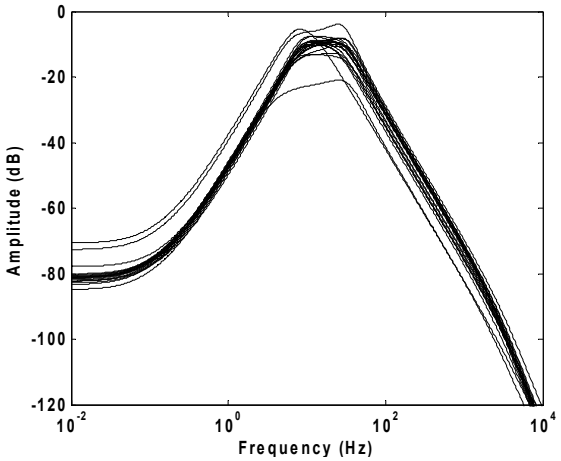

Fig. 13. Monte-Carlo simulation results for the amplitude characteristic of the filter.

From Fig. 13, it is seen that most of the cases the variations are in specific limits however there are some cases where deviations are significant. This is caused by the susceptibility of the circuit to process deviations which mainly affect the biasing under ultra low supply voltage with ultra low biasing currents. These biasing currents can be increased but this trades off power consumption performance of the filter.

4.1 Processing of the Measured EEG Data

In order to further investigate the characteristics of the proposed band-pass filter, real measurements from an SSVEP (Steady State Visual Evoked Potential)-based BCI (brain computer interface) EEG experiment were used with the help of MATLAB program. SSVEP dominantly appears in the visual cortex of the brain and it is the result of a person's attention on flickering lights [22]. It is measured by using EEG methods. Constant frequency signals visually stimulate a person and this affects the person's EEG signal at the same frequency which can be used as a mean to brain computer interaction which is currently an active research topic.

Fig. 14. EEG measurements setup [22].

EEG measurement setup and the data in [22] were used for applying input signal data to our filter. The experiment setup is shown in Fig. 14. EEG signal is sensed via electrodes connected to the scalp. These signals are then fed into an amplifier system specialized on EEG data recordings. Amplified signal data are then transferred to computer for further processing. The part of the experiment we used for filtering is comprised of computer recordings of the EEG signals of the subjects while they are looking at four red circles at the four corners of the computer monitor flickering at four different constant frequencies (4.60 Hz, 6.43 Hz, 8.03 Hz, and 10.70 Hz). Applied input data is taken from the OZ channel of the connected 16 electrodes. This channel is more sensitive to the visual stimulations.

The data was taken for 30s with a sampling frequency of 500Hz generating 15000 data points [22]. For simplic-

ity, in our filter application, we have just used the recordings for two seconds with 1001 data points from OZ channel recordings of the subject's visual attention on the left red circle that is flickering on the monitor with a constant frequency of 10.70 Hz.

Filter input and output signals are illustrated in Fig. 15. For figure clarity, only the data of first 0.4 s is shown in the figure and the output signal is multiplied by a factor of filter gain loss to compensate the decrease in amplitude. Input data signal amplitudes are also multiplied by a factor to manage to use them properly as inputs to the filter.

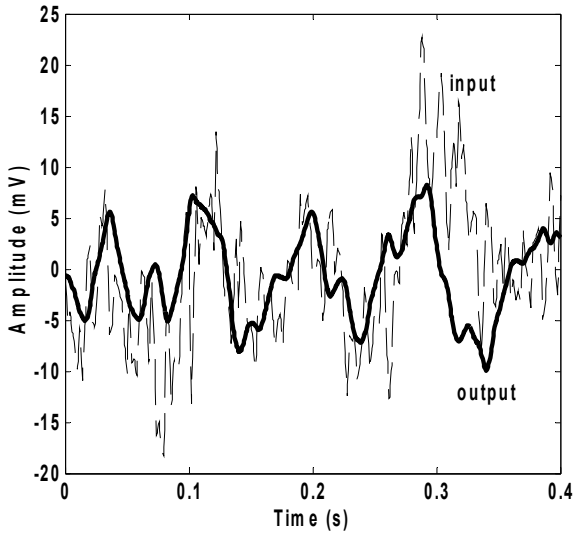

Fig. 15. Time response of the filter output for the measurement EEG data for 0.4 s.

In Fig. 16 and Fig. 17, pre-filter and post-filter frequency spectrums of our EEG signal are depicted respectively. As shown in the figures, unwanted frequency harmonics are successfully filtered out from the signal by the VDTA filter and the main frequency component of 10.74 Hz is become clearer after the filter. That is almost the same frequency of the applied visual stimulation signal to the subject which shows the validity of SSVEP study where the subject's brain reacts to the applied flickering light by producing EEG signal at the same frequency of the flickering. That phenomenon is used in brain computer interface applications.

Performance summary of the filter circuit in this work and comparison of other published low power filter circuits with a Figure of Merit (FoM) [6], which is described in (10), are given in Tab. 3. From the results, it is seen that, DTMOS-based VDTA filter in this work, with a FoM better than [4], [5] and worse than [6] achieves a moderate performance among the filters in Tab. 3. However, it is important to note that the proposed DTMOS-based filter circuit is capable of working under significantly lower supply voltage of ±0.2 V than its alternatives and consumes the least power.

$$FoM = \frac{P \times VDD}{n \times f_c \times DR}. \tag{10}$$

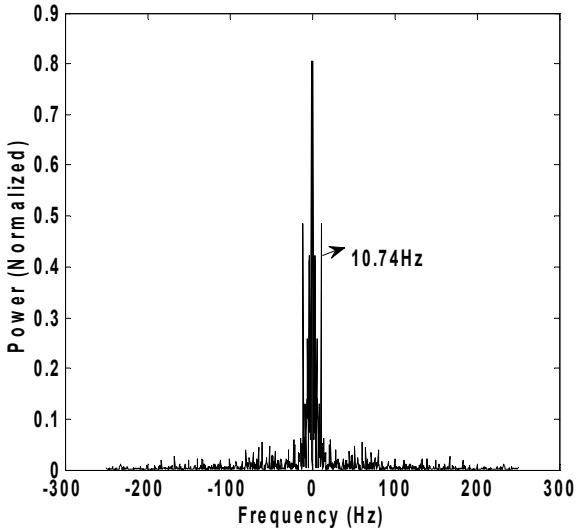

Fig. 16. Pre-filter frequency spectrum of the EEG data.

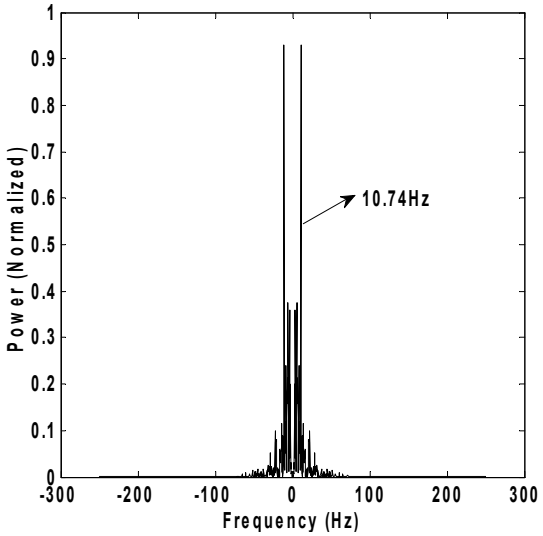

Fig. 17. Post-filter frequency spectrum of the EEG data.

Filter	[4]	[5]	[6]	This work
Supply (V)	0.9	2.8	1	±0.2
Power (nW)	262k	230	14.4	12.7
DR (dB)	52	67.5	55	63.7
f_c. (Hz)	1.12k	141	732	19.5
Order, (n)	6	4	4	4
THD (%)	1	5	1	2
FoM (10^{-13})	6632	169	0.89	10.2

Tab. 3. Performance summary and comparison of DTMOS-based VDTA filter.

5. Conclusion

In this study, DTMOS-based VDTA circuit was proposed. The circuit is capable of working under an ultra low supply voltage ±0.2 V and only consuming 5.96 nW. DTMOS transistors are used to efficiently exploit shrank voltage headroom. For very low power consumption, the transistors were used in weak inversion where DTMOS

transistors are very suitable to this mode of operation due to their well subthreshold slope characteristic.

Using the VDTA, a band-pass filter was designed for EEG data processing. The proposed circuit was used in a fourth order double-tuned pass-band filter. The filter consists of two VDTA cell and two externally connected capacitors. According to PSPICE simulations, both VDTA and the double-tuned filter have performed well. The filter was successfully used to filter out unwanted frequency components of an SSVEP based BCI system's amplifier outputs. Although, in measurements, there was amplifying and filtering integrated in the measurement hardware, there was still a need for additional filtering which is usually done by digital filtering via software. Instead of digital filtering approach, the proposed filter was utilized to investigate its performance in a practical application. It is found that both PSPICE and MATLAB results are in close agreement with theory. The proposed DTMOS-based VDTA circuit is suitable for ultra low-power, ultra low-voltage analog signal processing applications.

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