1.5V Fully Programmable CMOS Membership Function Generator Circuit with Proportional DC-Voltage Control

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Abstract. *A Membership Function Generator Circuit (MFGC) with bias supply of 1.5 Volts and independent DC-voltage programmable functionalities is presented. The realization is based on a programmable differential current mirror and three compact voltage-to-current converters, allowing continuous and quasi-linear adjustment of the center position, height, width and slopes of the triangular/trapezoidal output waveforms. HSPICE simulation results of the proposed circuit using the parameters of a double-poly, three metal layers, 0.5 μm CMOS technology validate the functionality of the proposed architecture, which exhibits a maximum deviation of the linearity in the programmability of 7 %.*

Keywords

CMOS, membership function generator, programmable current mirrors, non-linear circuits.

1. Introduction

The voltage shrinking in modern CMOS technologies and the growing need to develop efficient and low cost portable devices have obligated to produce circuits operating with narrow voltage headrooms and low power consumption requirements [1]. While supply voltages (V_{DD}) scale down, the threshold voltage of the transistors (V_T) does not follow proportionally this trend. In consequence, analog circuits must operate with small supply voltages in the range of $V_{DD} < 2V_{GS}$, being V_{GS} the voltage between the gate and source terminals of the MOS device. This condition entails analog designers to use low-voltage methodologies, such as floating-gate and bulk-driven transistors [1]–[3]. Unfortunately, most of those techniques exhibit large area requirements. This is a major disadvantage since area reduction is a crucial trend in modern VLSI circuits. This problem is particularly serious in extensive systems that realize several complex operations with dedicated hardware, like Neuro/Fuzzy systems [4]. An important building block of such systems is the Membership Function Generator. Membership Function Generator Circuits (MFGC) perform a non-linear transform from their input ports to their output ports. They are employed in applications including fuzzy logic systems [4]–[11], analog to digital conversion [12], non-linear control, piecewise-linear approximation [13], and neural networks [14], among others. Analog realizations of MFGC present a faster speed operation, a lower power consumption [15], [17], and a smaller area occupation than their digital counterparts. Unfortunately, most of the reported implementations exhibit important drawbacks [18]: (i) failure to adjust linearly and independently all the function parameters; (ii) linearity limited by Gaussian-like characteristics; (iii) complex programming functionalities; (iv) lack of adaptability, with the consequently establishment of a bottle-neck in the implementation of neuro-fuzzy systems.

The most common implementation of CMOS MFGC consists of source coupled differential pairs [4]-[6], [16]. Unfortunately, such approach produces bell-like shapes instead of triangular/trapezoidal output waveforms. Also, if slope adjustment is implemented, it affects the rest of the parameters. The realizations reported in [7], [8] and [18] overcome this disadvantage, where the slope adjustment is reached by switching resistive or transistor-based branches. However, those approaches can be susceptible to weak control unless a considerable number of switches is utilized. Moreover, n additional control signals are required to obtain 2^n different slopes. Other alternatives modify the slope with a bounded linearity by incorporating cross-coupled differential pairs with transistors operating in triode mode [19]. A fully programmable MFGC based on a programmable current mirror is reported in [20]. Unfortunately, that realization requires more than 132 transistors to be implemented and is not suitable for low voltage operation.

To overcome the issues mentioned above and improve the linearity of the slope control, a fully programmable MFGC with triangular/trapezoidal output characteristics is proposed in this paper. The architecture is based on a DC linearly controlled programmable current mirror and three compact voltage-to-current converters. The proposed MFGC possesses and independent control of the horizontal position. As well, height, width and the slopes of the membership function are controlled by DC voltage. The paper is organized as follows: in Section 2, the principle of operation of the proposed MFGC is described; later, in Section 3, the obtained simulation results of the circuit, designed in a double-poly, three metal layers, 0.5 μm CMOS technology are presented; finally, the conclusion is drawn in Section 4.

2. Proposed Voltage-Controlled MFGC

The proposed voltage-controlled MFGC is based on the current-controlled MFGC reported in [7] and [8]. That is a topology with DC voltage control of the height, the width and the center position of a triangular/trapezoidal output current, and with discrete slope adjustment reached by switching transistor-based branches that operate as digital to analog converters. Unfortunately, that approach have the following disadvantages: n additional ports are required to control 2^n different slopes; a weak control is obtained unless a considerable number of switches is utilized; voltage-mode instead of current-mode control signals can be preferred to simplify the interfacing with the adaptation mechanism. Thus, the main goal of this work is to develop a MFGC with trapezoidal output waveform and with independent DC control in voltage-mode of all the parameters.

Consider the input to output transfer relationship of Fig. 1(a). This transference characteristic is represented by the following relationship

$$\begin{aligned} I_{out} &= (\Psi \cdot V_{ref})\,\Theta m_b\,\{I_{in}\Theta(\Psi \cdot V_{aux}) + \\ &\quad [(\Psi \cdot V_{aux})\,\Theta I_{in}]\,\Theta(\Psi \cdot V_{sat})\} \end{aligned} \tag{1}$$

where I_{in} is the input current, V_{aux}, V_{sat} and V_{ref} are the voltages that are used to control the central point, the saturation and the maximum value, respectively, Ψ is a voltage-to-current conversion factor used to obtain $I_{aux} = \Psi V_{aux}$, $I_{sat} = \Psi V_{sat}$ and $I_{ref} = \Psi V_{ref}$ (I_{ref} defines the maximum degree of pertenence), and m_b is a current gain factor used to control the left and right slopes. Θ is the rectification or bounding difference operator, defined as

$$x\Theta y = \begin{cases} x-y & \text{if } x > y, \\ 0 & \text{in other case.} \end{cases} \tag{2}$$

The block diagram of the proposed implementation of (1) is depicted in Fig. 1(b). Blocks N_1, N_2, N_{3a}, N_{3b} and N_4 are unity-gain N-type current mirrors; P_3 is a P-type unity-gain current mirror; P_{V_1}, P_{V_2} and P_{V_3} are voltage-to-current converters with conversion factor Ψ; and P_b is a gain-programmable current mirror controlled by means of two balanced DC voltages V_{tune_1} and V_{tune_2}.

2.1 Principle of Operation

The double bounded operation between I_{in} and ΨV_{aux} in (1) is performed by the switching current mechanism realized by transistors M_{n_1} and M_{p_1} and by the CMOS inverter. The inverter reduces the required input voltage swing by the introduction of negative feedback. Consequently, a faster operation is obtained since the time delay to charge or discharge the parasitic capacitances is decreased. Transistor M_{p_1} drives current when $I_{in} > \Psi V_{aux}$. This charges the input node of the CMOS inverter, producing a low logic value in its output such that it turns-off transistor M_{n_1}, realizing the operation $I_{in}\Theta\Psi V_{aux}$. Alternatively, M_{n_1} drives current when $\Psi V_{aux} > I_{in}$. This discharges the input node of the CMOS inverter, producing a high logic value in its output which turns-off transistor M_{p_1}, performing the operation $\Psi V_{aux}\Theta I_{in}$. This mechanism avoids replication of I_{in} or ΨV_{aux} thus saving area and power consumption [8]. On the other hand, $-I_{sat}$ (which is equal to $-\Psi V_{sat}$) and the currents in M_{n_1} (mirrored with P_3) and M_{p_1} are added at node a to obtain the current $I_s = I_{in}\Theta(\Psi V_{aux}) + [(\Psi V_{aux})\Theta I_{in}]\Theta(\Psi V_{sat})$. Then, this current is amplified by a factor m_b equal to the gain of the programmable current mirror P_b. The use of a P-type programmable mirror along with the mirror N_{3b} instead of a programmable N-type current mirror N_{3a} allows a low-voltage realization, as will be described in section 2.4. Finally, the current $-I_s$, obtained with th mirror N_{3b}, is added at node b to $I_{ref} = \Psi V_{ref}$ and rectified with the mirror N_4 to complete expression (1).

2.2 N-Type and P-Type Mirrors

Blocks N_1, N_2, N_{3a}, N_{3b} and N_4 are implemented with the unity-gain N-type current mirrors shown in Fig. 1(c), while the block P_3 is the P-type unity-gain current mirror illustrated in Fig. 1(d). These mirrors are designed with a single transistor in the input to reduce the number of devices employed in the overall system and with cascoded outputs to improve the current copies.

2.3 Voltage-to-Current Converters

The compact circuit realization of the voltage-to-current converters P_{V_i} is depicted in Fig. 1(e). Herein, all the transistors operate in saturation mode. The input voltage is equal to $V_i = V_{bias} + v_{in}$, where v_{in} can be V_{aux}, V_{sat} or V_{ref}. By selecting

$$V_{eff_7} = V_{bias} - V_{T_n}, \tag{3}$$

$$I_{offset} = \beta_{M_7} V_{eff_7}^2, \tag{4}$$

$$V_{eff_7},\ v_{in} << V_{T_n}, \tag{5}$$

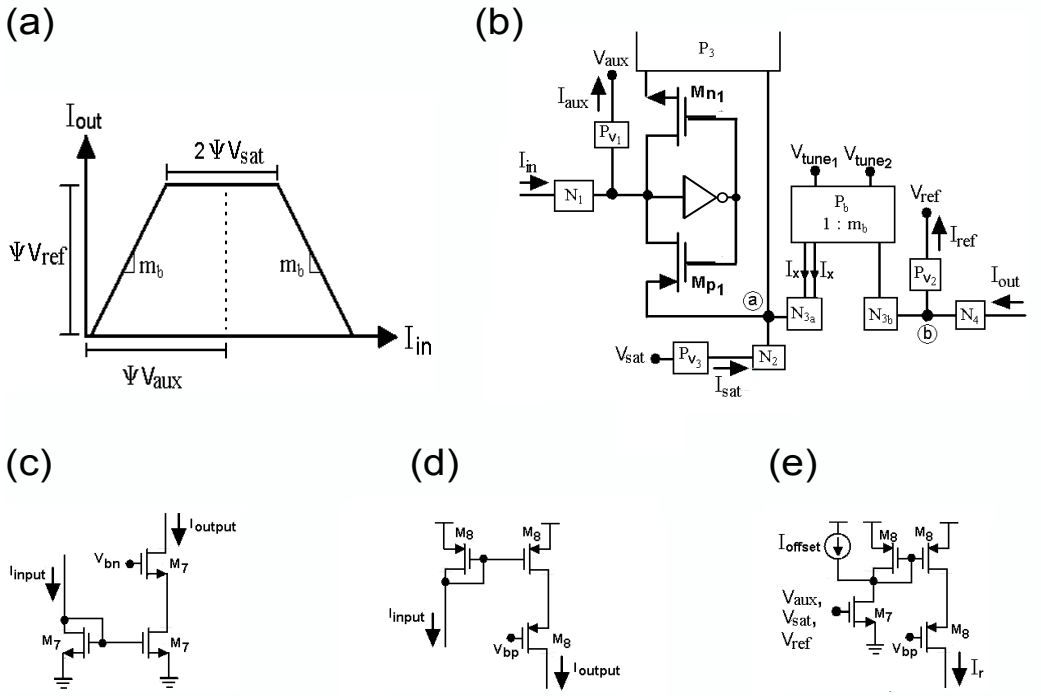

Fig. 1. MFGC: (a) parameters that define the triangular/trapezoidal response; (b) block diagram of the proposed voltage-controlled MFGC; (c) unity-gain N current mirror N_i; (d) unity-gain P current mirror P_3; (e) voltage-to-current converter P_{V_i}.

the voltage-to-current transference is obtained:

$$I_r \approx (\beta_{M_7} V_{eff_7})\, v_{in} = \Psi v_{in}. \tag{6}$$

The current I_{offset} is fulfilled with a current mirror similar to that illustrated in Fig. 1(d).

2.4 Programmable Current Mirror P_b

The proposed low-voltage programmable differential current mirror is shown in Fig. 2. The current mirrors N and P are implemented with current mirrors similar to the illustrated in Fig. 1(c) and Fig. 1(d). The two output currents of the block N_{3_a} of Fig. 1(b) and P generate the input balanced currents I_x and $I_y = -I_x$. Hence, by defining

$$V_{GS_{M3,4}} = V \pm \Delta V, \tag{7}$$

the current gain I_{ox}/I_x results in

$$\frac{I_{ox}}{I_x} = R\left(\frac{V_A + \Delta V}{V_A - \Delta V}\right)^2 \tag{8}$$

where

$$R = \frac{W_{M_2} L_{M_1}}{W_{M_1} L_{M_2}}, \tag{9}$$

$$V_A = V_{DD} - V_X - V - |V_{Tp}| \approx constant \tag{10}$$

and $|V_{Tp}|$ is the threshold voltage. The gain of the balanced configuration, $m_b = (I_{oy} - I_{ox}) / (I_y - I_x)$, is obtained approximating (8) by a Taylor series around $\Delta V = 0$ and canceling the even-order factors, resulting in

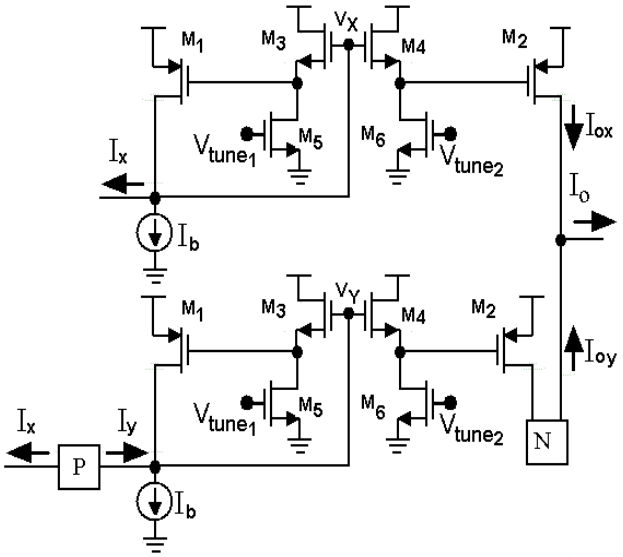

Fig. 2. Programmable current mirror P_b.

$$m_b = R\left\{1 + 4\frac{\Delta V}{V_A} + 12\left(\frac{\Delta V}{V_A}\right)^3 + \ldots\right\} \approx R\left\{1 + 4\frac{\Delta V}{V_A}\right\} \tag{11}$$

with $\Delta V << V_A$. This is an approximately linear depen-

dence with a small third- harmonic distortion component $H_{D3} = 0.75\,(A/V_A)^2$, where $\Delta V = A\sin(\omega t)$ has been used to calculate H_{D3}. In case that $A = 0.05\ V_A$ then $H_{D3} < -54$ dB.

The component ΔV of (7) is controlled by currents I_{M_5} and I_{M_6} which are adjusted respectively by

$$\begin{aligned} V_{tune_1} &= V_B - \Delta V, \\ V_{tune_2} &= V_B + \Delta V \end{aligned} \tag{12}$$

where V_B is a DC voltage. Transistors M_3 and M_4 remain in saturation mode as their drain terminal is connected to V_{DD}, while transistors M_5 and M_6 are forced to operate in triode mode using the restriction

$$V_{tune_1(tune_2)} > V_{DD} - V_{SG_{M_1(M_2)}} + V_{T_n}. \tag{13}$$

By defining $V_{DS_{M_6,M_5}} = V_X - (V \pm \Delta V)$ and $(W_3/L_3) = (W_4/L_4) = m\,(W_5/L_5) = m\,(W_6/L_6)$, the equalities $I_{D_{M_6}} = I_{D_{M_4}}$ and $I_{D_{M_5}} = I_{D_{M_3}}$ result in

$$2\,(V_C + \Delta V)^2 = m\,(V_D + \Delta V_{tune})\,(V_E - \Delta V), \tag{14}$$

$$2\,(V_C - \Delta V)^2 = m\,(V_D - \Delta V_{tune})\,(V_E + \Delta V) \tag{15}$$

where

$$V_C = V - V_{T_n}, \tag{16}$$

$$V_D = V_B - V_{T_n}, \tag{17}$$

$$V_E = V_X - V. \tag{18}$$

Now, if $m >> 2V_C/V_D$ is established in (14) and (15), after some algebraic manipulation, ΔV results in

$$\Delta V \approx (V_E/V_D)\,\Delta V_{tune} \tag{19}$$

and combining (11) and (19), m_b becomes

$$m_b = R\left(1 + 4\frac{V_E}{V_A V_D}\Delta V_{tune}\right). \tag{20}$$

The circuit of Fig. 2 is a low-voltage realization since the source-gate voltages of transistors M_1 and M_2 are in opposite polarity with respect to the gate-source voltages of transistors M_3 and M_4, respectively. As a consequence, the overall voltage at nodes V_X and V_Y is reduced. Therefore, the programmable current mirror requires $V_{X,Y_{min}} > V_{T_n} + 2V_{sat}$ with $V_X \approx V_{DD} - \left(|V_{T_p}| - V_{T_n}\right)$. Hence, for $|V_{T_p}| = 0.95$ V, $V_{T_n} = 0.65$ V and $V_{sat} = 0.1$ V, it is obtained that $V_{DD_{min}} \approx 1.2$ V.

There are two important differences between the proposed current scaler and the circuit reported by [17]:

- In the proposed circuit, the control is performed by voltage signals instead of current signals. It yields in a simplification of the interface between the signals from the sensor and the digital adaptation mechanism.
- In the proposed circuit, the control is performed by balanced signals. It allows getting a linear control in weak, moderate and strong inversion modes. The current scaler of [17] works linearly only in moderate inversion.

	Ratios and values
M_1, M_2, M_3	120/1.2, 360/1.2, 72/1.2
M_4, M_5, M_6	72/1.2, 9/30, 9/30
M_7, M_8	12/12, 30/1.2
V_{DD}, I_b, I_{offset}	1.5V, 5 μA, 4.5 μA

Tab. 1. Aspect ratios of transistors in Fig. 1 and bias details.

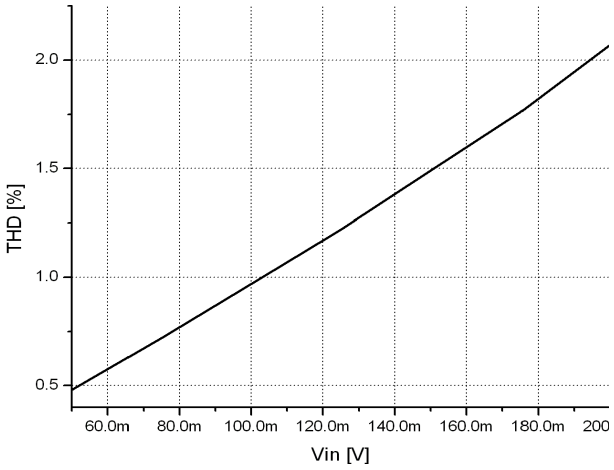

Fig. 3. Total harmonic distortion of the voltage-to-current converter .

3. Results

The MFGC of Fig. 1(b) was simulated in HSPICE using the parameters of a double-poly, three metal layers, 0.5 μm CMOS technology from ON-Semi foundry ($V_{T_n} = 0.65$ V, $|V_{T_p}| = 0.95$ V). The aspect ratio of the transistors and the bias of the circuit are detailed in Tab. 1. Dimensioning of the circuit was done considering the equations presented in Subsection 2.4, with $m = 200$ to facilitate the operation of the transistors M_5 and M_6 in triode mode. The bias supply for the circuit was 1.5 V with $I_b = 5$ μA and $I_{offset} = 4.5$ μA. The proposed MFGC can be considered a low-voltage realization because $V_{DD} < V_{T_n} + |V_{T_p}|$ (i.e., 1.5 V < 0.65 V $+ 0.95$ V). First, the behavior of the voltage-to-current converter is analyzed. The gain $\Psi = 36$ μV/A is presented with a Total Harmonic Distortion (THD) that ranged from 0.5 % to 2 % when the amplitude of the input signal changed from 60 mV to 200 mV (see Fig. 3).

The DC features of the MFGC are depicted in Fig. 4. The height adjustment was performed by means of V_{ref} in steps of 25 mV ranging from 1 V to 1.3 V (Fig. 4(a)). On the other hand, the horizontal position was tuned by means of modifying V_{aux} from 1.05 V to 1.20 V in 12.5 mV steps (Fig. 4(b)). The slopes were adjusted by means of $\Delta V_{tune} = V_{mb}$ in 50 mV steps from -0.5 V to 0.15 V (Fig. 4(c)). The saturation adjustment was realized by changing V_{sat} from 1 V to 1.1 V in 10 mV steps (Fig. 4(d)). According to the obtained simulation results, we conclude that the behavior of the MFGC follows the course anticipated in the synthesis of the circuit performed in Section 2.

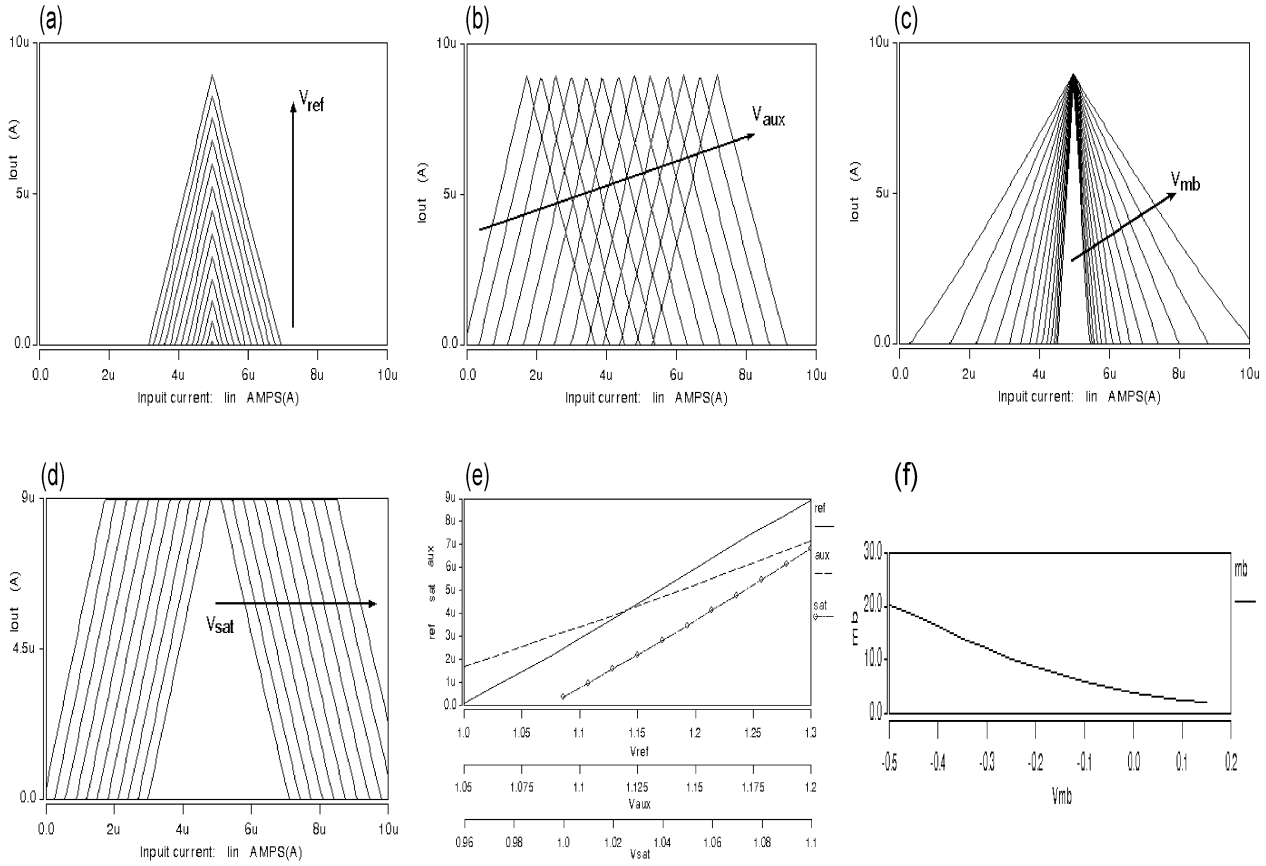

Fig. 4. Simulation results of the proposed MFGC: (a) height adjustment; (b) horizontal position adjustment; (c) slope adjustment; (d) saturation adjustment; (e) linearity of height, horizontal position, and saturation adjustments; (f) linearity of the slope adjustment.

Ref.	Tech.	Supply	Transistors count or area	Parameters controlled	Controled by	Power or I_{bias}	Control	In	Out
[4]	1.5 μm	–	variable	3	variable trasconductance	–	non independent	V	I
[5]	–	10 V	38+4I_{bias}	6	2 voltage sources 4 current sources	25 μA	slope: non linear	V	I
[6]	0.6 μm	5V	21+2I_{bias} 0.03 mm^2	4	2 voltage sources 2 current sources	200 μA	only position is independent slope: non linear	V	I
[8]	1.5 μm		variable	4	D/A converters	–	digital linear control	V	I
[11]	0.35 μm	1.5V	42+13I_{bias}	5	2 voltage sources 3 current sources	–	slope: non linear and non independent	V	I
[16]	0.8 μm	–	84 0.07 mm^2	5	2 voltage sources 3 current sources	80 μA	no linear slope control	V	I
[18]	0.5 μm	3V	28	5	switched brances 3 current sources	90 μA	all linear and non independent	V	I
[21]	0.7 μm	5 V	>50	3		1.7 mW	non independent	V	I
[20]	0.35 μm	3.3 V	>132	3	2 voltage sources 1 current source	100 μA	no linear slope control	I	I
This work	0.5 μm	1.5 V	61 (*)	4	4 voltage sources	200 μW 5 μA	all linear including slope	I	I

Tab. 2. Comparison of reported MFGC.
(*) 12 transistors are used to prepare the interfacing with the adaptation mechanism.

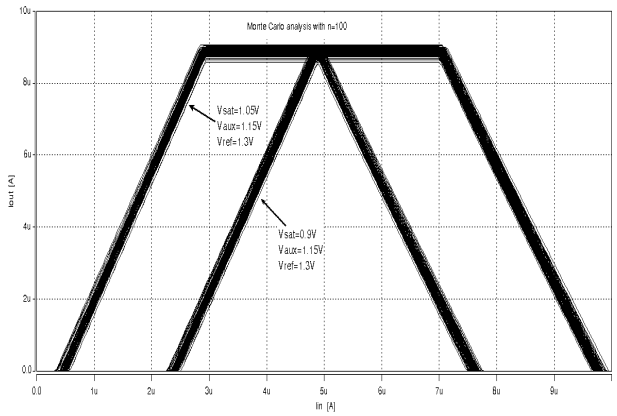

Fig. 5. Monte Carlo simulation of the MFGC.

The programmability resulted in a linear control in the height, horizontal position and saturation level, as can be appreciated in (Fig. 4(e)). However, the adjustment of the edge slops resulted approximately linear (see Fig. 4(f)) in the range from -0.5 V to 0.2 V, with a maximum deviation of the linearity of 7 %. When a positive step input current from 0 A to 10 μA is applied to a triangular MFGC, the fall time for the output voltage to settle to 10 % of the steady state is 2.2 μs, while the maximum delay time is 2 μs.

Figure 5 shows the effect of the tolerances of the transistor in both, threshold voltages and current factors. The triangular and trapezoidal waveforms were simulated with a 100 cases Monte Carlo simulation using the Pelgrom's model, resulting maximum height and width variations of 5.2 % and 6 %, respectively.

Table 2 presents a comparison of the proposed MFGC with other realization previously reported in the literature. As can be observed, the proposed circuit is one of the most suitable for low-voltage and low power operation because of it only requires $I_{bias} = 5$ μA and $V_{DD} = 1.5$ V. Besides, the proposed MFGC allows a linear and continuous control of all the parameters of the triangular-trapezoidal output waveforms. Finally, despite the number of transistors is considerable, the use of low-voltage techniques is avoided and some of these transistors are used to establish the interface with the adaptation mechanism.

4. Conclusion

A MFGC with voltage-mode programming functionalities has been presented. Compared to other implementations, the proposed circuit is a low-voltage realization that presents triangular/trapezoidal output characteristics with independently adjustable slopes (in a range of 650 mV), height (in a range of 3000 mV), center position (in a range of 150 mV) and saturation level (in a range of 100 mV). Also, it achieves quasi-linear control of the slopes from $m_b = 2.5$ to $m_b = 20$ with a maximum deviation of the linearity of 5 % and without the need of digital control, preventing a weak control. Because of its quasi-linear behavior, independent programmability of parameters and easy implementation, this circuit constitutes a potential building block for applications such as piecewise linear approximations, neuro-fuzzy systems, and type-1 – type-2 fuzzy controllers, to name a few.

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