An Ultra-Low-Power Oscillator with Temperature and Process Compensation for UHF RFID Transponder

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Abstract. *This paper presents a 1.28 MHz ultra-low-power oscillator with temperature and process compensation. It is very suitable for clock generation circuits used in ultra-high-frequency (UHF) radio-frequency identification (RFID) transponders. Detailed analysis of the oscillator design, including process and temperature compensation techniques are discussed. The circuit is designed using TSMC 0.18μm standard CMOS process and simulated with Spectre. Simulation results show that, without post-fabrication calibration or off-chip components, less than ±3% frequency variation is obtained from –40 to 85°C in three different process corners. Monte Carlo simulations have also been performed, and demonstrate a 3σ deviation of about 6%. The power for the proposed circuitry is only 1.18 μW at 27°C.*

Keywords

Ultra-low-power, oscillator, temperature, process, compensation, RFID.

1. Introduction

The passive ultra-high-frequency (UHF) radio frequency identification (RFID) technology has gained more and more attention due to its long operating range and low cost. In UHF RFID applications, minimizing power is given first priority since the entire transponder is powered from the incident radio frequency (RF) power. Complying with standard is another important issue that needs to be considered. A major UHF RFID standard is the electronic-product-code Class-1 Generation-2 (EPC C1G2) standard [1] which ensures reliable data rates and good performance of RFID applications. The EPC C1 G2 transponder needs a system clock of at least 1.28 MHz; the tolerance of the oscillator frequency is determined by the baseband processor variation-tolerant design [2] and the tolerance of the tag-to-interrogator link frequency defined in EPC C1 G2. This is challenging to achieve a low-power dissipation and frequency stability against variations in process, power supply, and temperature (PVT) at the same time.

Several ultra-low-power oscillators for UHF RFID have been reported in literature. In [3], a frequency stable relaxation oscillator is designed based on the mutual compensation of carrier mobility, capacitor and thermal voltage. However, the power to frequency ratio is still too large to be used in RFID transponder. Moreover, the NPN band-gap reference used in [3] requires a high value resistor to achieve low-current operation, and this result in a larger die area. In [4], two variants of low-power ring oscillator are designed and compared. The second variant shows acceptable process deviation for UHF RFID transponder. However the temperature feature is neglected and the generation of control current is unmentioned but assumed constant. Another oscillator for RFID transponder was reported in [5], a novel design was proposed to minimize the supply voltage and thus power consumption. However, the frequency variation over process and temperature is not mentioned. Overall, most of the reported ultra-low-power oscillators cannot achieve both temperature and process insensitive at the same time. The majority of existing PVT stable clock generator designs are based on either PVT compensation techniques [6-8] or digital calibration [9]. The former suffers from huge power consumption due to the complexity of topology. The latter relies on the comparison of the received RF signal's data rate and the on-chip clock frequency. However, the received signal's data rate is often not fixed. For instance, there are three possible values of the data rate according to the EPC C1 G2 standard. Therefore, an additional sampling-oscillator is required to determine the data rate, which increases power consumption. In this paper, we present an ultra-low-power CMOS oscillator with temperature and process compensation. By using a sub-threshold voltage reference and a simple compensation circuitry, the oscillator's frequency is insensitive to the variations of PVT, and the power for the proposed circuitry is only 1.18 μW under typical operating condition. Such oscillator can be used as a clock circuit in a passive UHF RFID transponder for EPC C1 G2 standard. The proposed design strategy is also suitable for on-chip clock generation in other low-power systems.

The rest of paper is organized as follows: Section 2 demonstrates the system architecture of the oscillator; Section 3 describes the detail circuit analysis and design con-

siderations of main blocks. Simulation results are presented in Section 4. Section 5 concludes this paper.

2. System Architecture

Fig. 1 shows the block diagram of the presented oscillator system, which is based on a ring oscillator structure. Since the passive RFID transponder employs a rectifier to convert incident RF wave to DC voltage for power supply, the output voltage of the rectifier will vary widely when changing the distance between tag and reader. Therefore, a voltage regulator, as shown in Fig. 1, is employed to generate constant DC voltages independent of the incident RF power. Two output voltages of the regulator, V_{dd} (about 1 V) and V_p (about 1.8 V), serve as a supply and a process variation monitor, respectively. V_p is supplied to the temperature and process compensation circuit. The output of the compensation circuit is a bias voltage, V_{ctrl}, which stabilizes the frequency of oscillation by varying the bias current of the ring oscillator adaptively. The output of the oscillator is converted to a full swing rail-to-rail clock signal by a two-stage buffer.

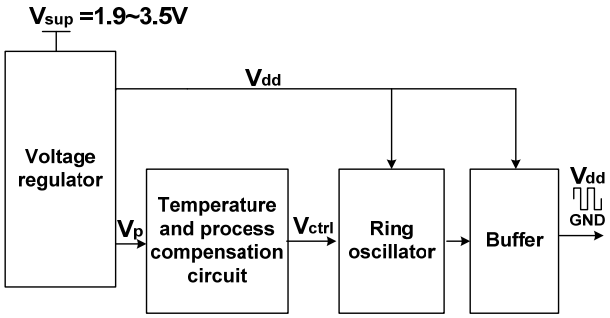

Fig. 1. Block diagram of the proposed oscillator.

3. Circuit Blocks

3.1 Oscillator

The reference frequency is created by a ring oscillator with three inverter delay stages as shown in Fig. 2. The oscillator has no capacitors and works with parasitic capacitances. The bias current, I_{bias}, controlled by the gate voltage of M11, V_{ctrl}, tunes the oscillation frequency. To decrease the sensitivity of the bias current to the supply, a degenerating resistor, R_d, is used to increase the output impedance of the current sink. The resistor R_d is implemented by two types of resistors, poly resistors and N-well resistors, which have opposite temperature dependency. Therefore, by changing the proportion of the poly resistors and N-well resistors, we can fine adjust the temperature coefficient of the bias current to obtain a better compensation. The time delay of each delay stage is given by [10]

$$t_d = \frac{C_p\left(V_{dd} - V_{dsp}\right)}{I_{bias}} \tag{1}$$

where C_p is parasitic capacitances, V_{dsp} is the drain-source voltage of M2~M4. Assuming a high W/L ratio of M1~M4, V_{dsp} can be neglected, then (1) can be simplified as

$$t_d = \frac{C_p V_{dd}}{I_{bias}} \ . \tag{2}$$

The relationship between the bias current and V_{ctrl} can be expressed as

$$I_{bias} = \frac{1}{2} K_{11}^{'} \frac{W_{11}}{L_{11}} \left[V_{ctrl} - I_{bias} R_d - V_{thn}\right]^2 . \tag{3}$$

By combining (2) and (3), the frequency of the oscillator can be expressed as a function of V_{ctrl}:

$$f = \frac{1}{3t_d} = \frac{1 + K_{11}^{'} \frac{W_{11}}{L_{11}} R_d (V_{ctrl} - V_{thn}) + \sqrt{1 + 2K_{11}^{'} \frac{W_{11}}{L_{11}} R_d (V_{ctrl} - V_{thn})}}{3C_p V_{dd} K_{11}^{'} \frac{W_{11}}{L_{11}} R_d^2} \tag{4}$$

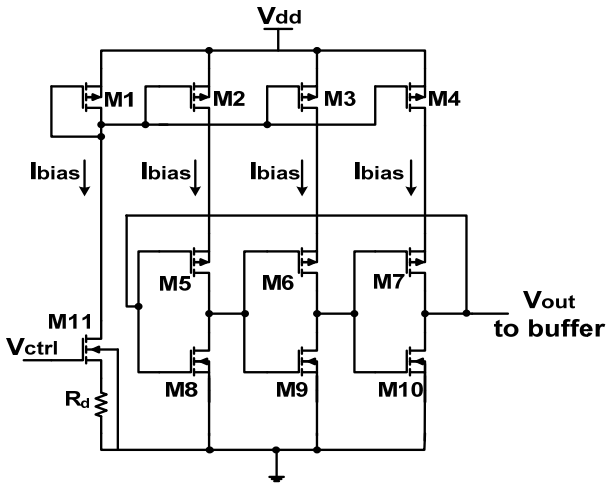

Fig. 2. Schematic of the ring oscillator.

Element	Size
M11	4μm/11μm
M1~M4	1μm/10μm
M5~M7	4.5μm/2.7μm
M8~M10	0.92μm/2.7μm
R_d	1.38MΩ poly resistor and 0.42MΩ N-well resistor

Tab. 1. Key element parameters of oscillator.

The circuit has been implemented in TSMC 0.18μm standard CMOS technology. The threshold voltage of the MOS transistors is about 450 mV. The oscillator is supplied with V_{dd}, which is 1 V under typical condition. The bias current I_{bias} is nominally set at 200 nA by the control voltage V_{ctrl}. The key element design parameters of the oscillator are summarized in Tab. 1.

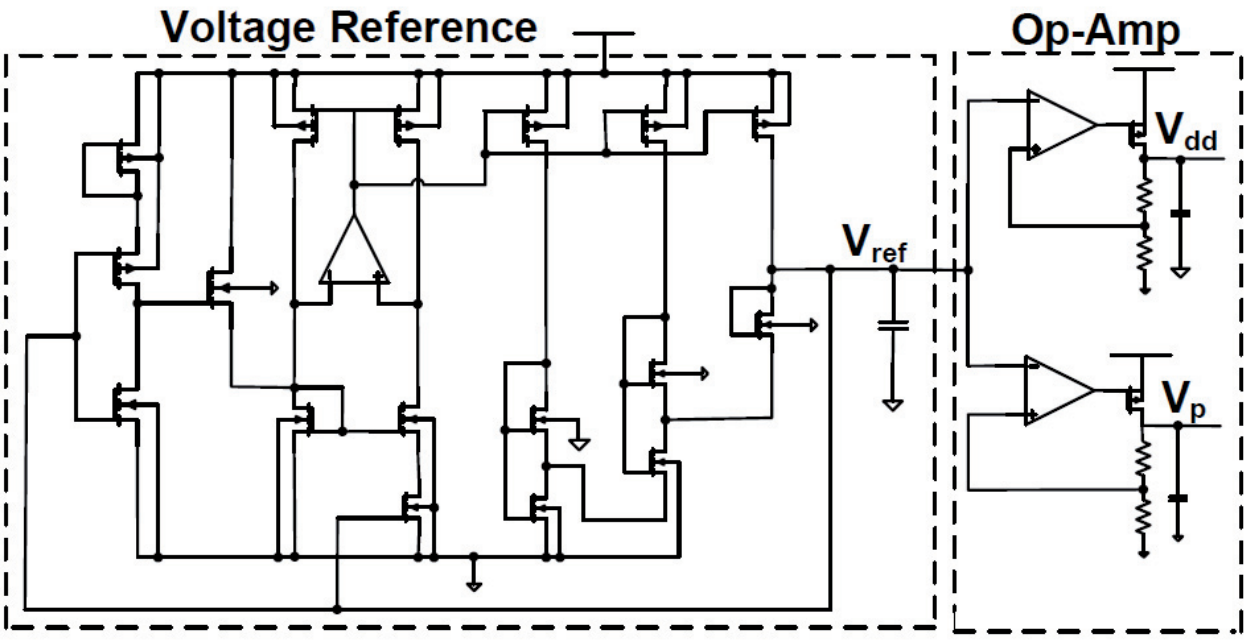

Fig. 3. Schematic of the voltage regulator.

3.2 Voltage Regulator

The voltage regulator, shown in Fig. 3, is based on a low-power sub-threshold MOSFETs reference [11]. The voltage reference consists of MOSFETs operated in the sub-threshold region and uses no resistors, therefore having a less power dissipation and smaller die occupation compared to the bandgap reference used in [6]. The reference voltage, V_{ref} is equal to V_{th0} the extrapolated threshold voltage of a MOSFET at absolute zero temperature. Hence, V_{ref} is independent of temperature, but contains the process corner information. The op-amp stages boost this reference level to V_{dd} (1 V under typical conditions) and V_p (1.8 V under typical conditions) serving as the power supply of the system and the process variation monitor, respectively.

3.3 Compensation Circuit

To maintain the oscillator frequency constant, V_{ctrl} must be changed with temperature and process variations adaptively. By rearranging (4), one can get the following relationship between V_{ctrl} and f:

$$V_{ctrl} = V_{thn} + 3fC_pV_{dd}R_d - \sqrt{\frac{6fC_pV_{dd}}{K_{11}^{'}\dfrac{W_{11}}{L_{11}}}}\ . \tag{5}$$

V_{dd} is determined by the voltage divider and reference voltage and hence can be expressed as

$$V_{dd} = A \cdot V_{ref} \approx A \cdot V_{th0} \tag{6}$$

where A is the factor of proportionality determined by the voltage divider. In addition, the temperature dependences of the threshold voltage, the mobility of the charge carriers, the junction capacitance and the oxide capacitance can be approximately given by [12]

$$\begin{aligned} V_{thn} &= V_{th0}(1+\kappa_{Vt}T) \\ \mu &= \mu_{p0}T^{-2.2} \\ C_p &= C_{p0}(1+\kappa_{Cp}T) \\ C_{ox} &= C_{ox0}(1+\kappa_{Cox}T) \end{aligned} \tag{7}$$

where κ_{Vt}, κ_{Cp}, and κ_{Cox} are the temperature coefficients and are all negative.

By combining (5) ~ (7), one can get the expression of V_{ctrl}:

$$V_{ctrl} = V_{th0} + V_{th0}\kappa_{Vt}T + 3fC_{p0}(1+\kappa_{Cp}T)AV_{th0}R_d - \sqrt{\frac{6fAV_{th0}C_{p0}(1+\kappa_{Cp}T)(1-\kappa_{Cox}T)}{\mu_{p0}T^{-2.2}C_{ox0}(1-\kappa_{Cox}{}^2T^2)\dfrac{W_{11}}{L_{11}}}} \tag{8}$$

Since the temperature coefficients (κ_{Vt}, κ_{Cp}, and κ_{Cox}) are quite small, the contribution of higher order terms are small, such terms can be neglected. With this approximation, (8) can be simplified as

$$V_{ctrl} = X + Y \cdot T \tag{9}$$

where X and Y are influenced by process parameters, and are given by

$$\begin{aligned} X &= V_{th0} + 3fC_{p0}AV_{th0}R_d \\ Y &= V_{th0}\kappa_{Vt} + 3fC_{p0}AV_{th0}R_d\kappa_{Cp} - \sqrt{\frac{6fC_{p0}AV_{th0}}{\mu_{p0}C_{ox0}\dfrac{W_{11}}{L_{11}}}} \end{aligned} \tag{10}$$

It can be seen that Y is negative. In other words, the temperature coefficient of V_{ctrl} is negative, and this can be supplied by V_{gs} of a diode-connected MOSFET working in sub-threshold regime. Furthermore, the process variation trend of the required V_{ctrl} is in agreement with that of the threshold voltage of MOSFET. As stated above, the reference voltage equals to the threshold voltage of MOSFETs at 0 K. Therefore, V_p can be used for process compensation. Fig. 4 shows the schematic of the compensation circuit. A diode-connected NMOSFET M12 is used to adjust the temperature coefficient of V_{ctrl}. Resistors R1 and R2 are used to divide V_p into certain proportion so that V_{ctrl} satisfies (9) across multiple process corners. The expression for V_{ctrl} generated by the compensation circuit is given by

$$V_{ctrl} = V_p - IR_1 = \frac{R_1 V_{thn} + R_2 V_p}{R_1 + R_2} - \frac{R_1}{K_1' \frac{W_1}{L_1}(R_1 + R_2)^2} - \frac{R_1}{K_1' \frac{W_1}{L_1}(R_1 + R_2)^2}\sqrt{1 + 2K_1' \frac{W_1}{L_1}(R_1 + R_2)(V_p - V_{th})} \quad (11)$$

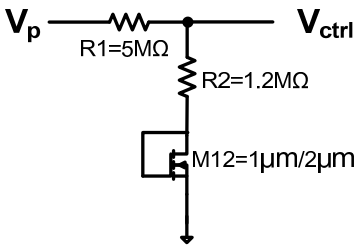

Fig. 4. Schematic of the compensation circuit.

Fig. 5 shows the required and simulated plots of V_{ctrl} versus temperature for various process conditions. It can be seen that the compensation circuit provides an excellent fit to V_{ctrl} for all process conditions and temperature variations. The temperature coefficient of V_{ctrl} shows a slight nonlinearity due to the curvature of the voltage reference's temperature coefficient.

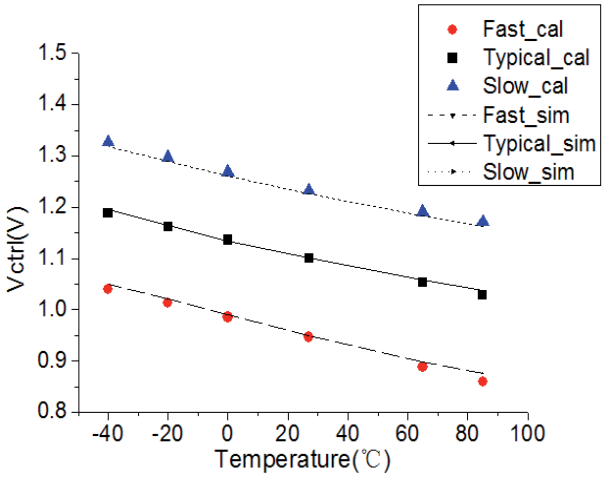

Fig. 5. Required and simulated V_{ctrl} versus temperature plots.

4. Simulation Results

The layout of the proposed circuit is shown in Fig. 6. The post-simulation of the proposed circuit has been done by using Spectre. Simulation results predict that the proposed oscillator generates a clock signal at about 1.28 MHz. Under the typical process corner, the power consumption of the proposed circuit is 1.18 μW at 27°C.

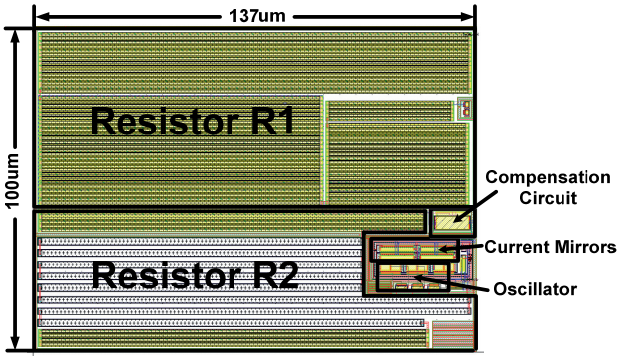

Fig. 6. Layout of the proposed oscillator.

Fig. 7(a) shows the oscillation frequency with respect to the temperature for various process conditions. Simulation results show a nominal frequency of 1.28 MHz, and a worst-case variation of ±3% in its output frequency over a temperature range of –40 to 85°C and for three different process conditions. As comparison, Fig. 7(b) demonstrates the simulation results of a variant for this oscillator which implements R_d with poly resistors only. Obviously, our proposed method of fine adjustment with hybrid resistors achieves less frequency dependence on temperature. Fig. 7(c) shows a plot of the temperature and process variation of frequency for the uncompensated systems (with a fixed V_{ctrl}). It may be observed that in the uncompensated scheme, the frequency variation with temperature and process is much larger even though the bias voltage is fixed.

In addition, Monte Carlo simulations have been performed at 27°C, and the results are shown in the histogram of Fig. 8. Simulation results show a mean value of the oscillation frequency of 1.284 MHz and a standard deviation of 27.6461 kHz, leading to a 3σ deviation of about 6%.

Tab. 2 compares the performance of the proposed circuit with that of previous designs. We can note that the proposed oscillator takes into account the variation of both process and temperature, and achieves outstanding balance between the clock accuracy and the power consumption. The variation of frequency is acceptable for several applications, such as RFID transponders or biomedical applications, but larger than that of the circuits in [6], [13]. However these circuits have the drawback of higher circuitry complexity and power consumption, compared to our proposed solution. The oscillators presented by [3-5] achieve low power. However, as is mentioned early, they don't fully consider the temperature and process variation. As a result, system may not work as frequency drifting in some temperature and process corners.

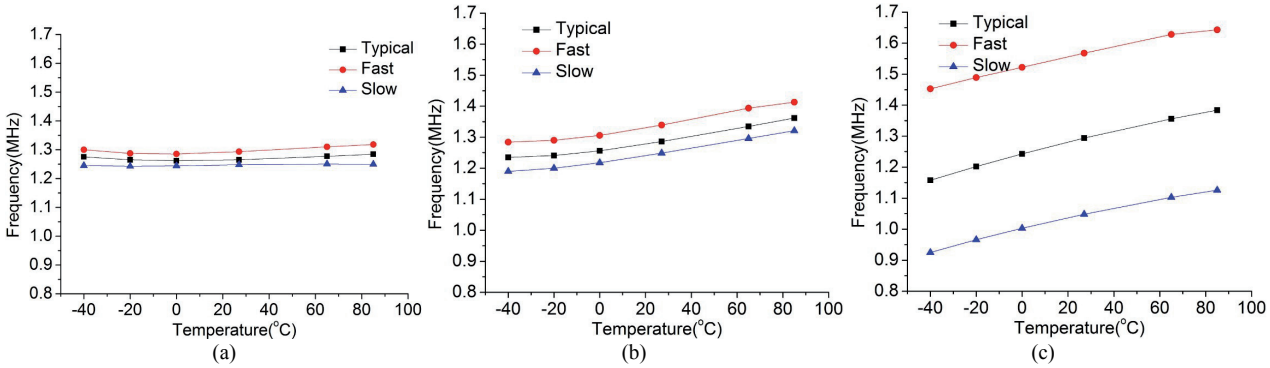

Fig. 7. Simulated frequencies versus temperature under different process corners. (a) Compensated oscillator. (b) The variant with poly resistors only. (c) Uncompensated oscillator with a fixed Vctrl.

Reference	[6]	[13]	[3]	[4]	[5]	This work
Process (µm)	0.25	0.18	0.35	0.14	0.13	0.18
Frequency (MHz)	7	30	0.08	1.28	1.52	1.28
Power (µW)	1500	220	1.14	0.44	0.32	1.18
Temp range (°C)	-40~125	-40~125	0~80	N/A	N/A	-40~85
Worst case variation (process & temperature, simulation results)	±1.7%	±2%	N/A	N/A	N/A	±3%
3σ deviation (From Monte Carlo simulation)	N/A	N/A	11.85%	8%	N/A	6%
Die area(mm^2)	1.6	0.0144	0.24	N/A	0.0134	0.0137

Tab. 2. Oscillator specification comparison with references.

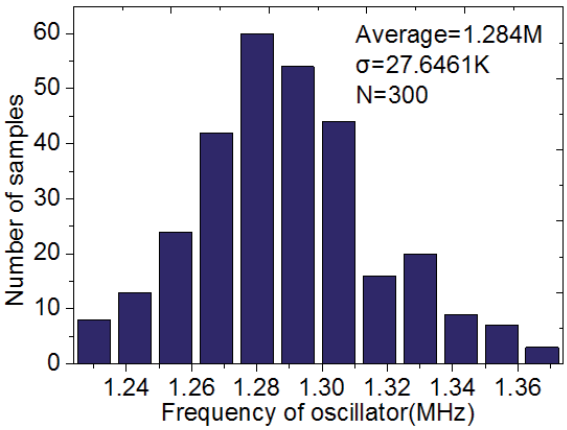

Fig. 8. Monte Carlo simulation with process variations and mismatches.

5. Conclusion

An ultra-low-power oscillator with temperature and process compensation has been presented. The proposed oscillator is for the clock generation of an EPC C1 G2 transponder. The whole circuit consumes only 1.18 µW for a clock centered at 1.28 MHz. According to the simulation, the overall frequency variation is within ±3% when consider three process corners and temperature ranging from –40 to 85°C. The proposed design strategy can also be used in the design of on-chip clock generation for other low-power systems, such as wireless sensors or implantable electronic devices.

Acknowledgments

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