Symbolic Nodal Analysis of Analog Circuits with Modern Multiport Functional Blocks

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Abstract. *This paper proposes admittance matrix models to approach the behavior of six modern multiport functional blocks called: differential difference amplifier, differential difference operational floating amplifier, differential difference operational mirror amplifier, differential difference current conveyor, current backward transconductance amplifier and current differencing transconductance amplifier. The novelty is that the behavior of any active device mentioned above can immediately be introduced in the nodal admittance matrix by using the proposed admittance matrix models and without requiring the use of extra variables. Therefore, a standard nodal analysis is applied to compute fully-symbolic small-signal performance parameters of analog circuits containing any active devices mentioned above. This means that not only the size of the admittance matrix is smaller than those generated by applying modified nodal analysis method, for instance, but also, the number of nonzero elements and the generations of cancellation-terms are both reduced. An analysis example for each amplifier is provided in order to show the useful of the proposed stamps.*

Keywords

Nodal admittance matrix, symbolic analysis, stamps controlled sources, operational amplifiers.

1. Introduction

During the last few years, various active devices have been proposed to be used in the analog signal processing [1], such as the Differential Difference Amplifier (DDA) [1], the Differential Difference Operational Floating Amplifier (DDOFA) [2], the Differential Difference Operational Mirror Amplifier (DDOMA) [3], the Differential Difference Current Conveyor (DDCC) [5], the Current Backward Transconductance Amplifier (CBTA) [6] and the Current Differencing Transconductance Amplifier (CDTA) [7], among others [1], [8], [9]. In most applications, the electronic circuit behavior can be predicted by means of numerical simulations or symbolic expressions [10]-[16]. In the former case, numerical simulations do not give any information about which component plays the most important role in the transfer function behavior, since numerical simulations are used to verify the circuit behavior on an isolated point of the design space. In the latter, symbolic analysis techniques are very useful to compute symbolic transfer functions, since a symbolic expression provides direct insight on the influence of each circuit component over the circuit behavior and at all the design space. Therefore, symbolic analysis is an essential complement to numerical simulations. In any case, formulation methods based on graphs or matrices are required to formulate the system of equations and later on, recursive determinant-expansion techniques are applied in order to compute either numeric or symbolic small-signal performance parameters of the circuit [10]-[16].

On the other hand, among all the formulation methods based on graphs or matrices, the modified nodal analysis method (MNA) was adopted for the development of numerical simulators like Hspice, and also on the development of symbolic analyzers like ISAAC and SNAP, where the element stamp is used to fill the admittance matrix [11], [12], [15]. In this context, controlled sources are used to model the behavior of voltage-, current- and hybrid-mode active devices and each of them is included in the admittance matrix by using stamps [10]-[15]. Unfortunately, only the behavior of voltage-controlled current sources (VCCS) and current-controlled current sources (CCCS) can immediately be introduced in the nodal admittance matrix (NAM) by applying a nodal analysis (NA) only. For the other two controlled sources, i.e., the current-controlled voltage source (CCVS) and the voltage-controlled voltage source (VCVS), a column and row along with six nonzero elements must be added to the admittance matrix by each controlled source used [13]-[15]. That means that the system of equations of analog circuits whose behavior is modeled with controlled sources becomes large and dense. But, even the computational complexity and memory consumption are both increased when recursive determinant-expansion techniques are applied in order to compute fully-symbolic transfer functions. Therefore, the introduction of reduction techniques on the size of the admittance matrix becomes mandatory.

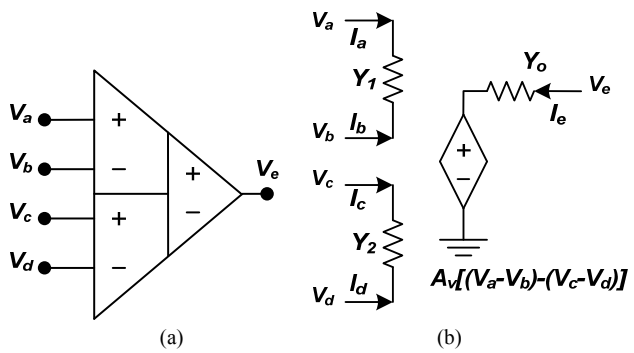


Fig. 1. (a) Symbol of the DDA, (b) equivalent model.

In order to reduce the complexity of the solution method, not only the admittance matrix must be as sparse as possible, but also the size of the system of equations must be kept as low as possible. In this scenario, new element stamps for the two non-NA compatible controlled sources have been reported, which are based on the concept of matrix port-equivalence and limit-variables [17]-[20]. However, although the behavior of the two controlled sources can immediately be introduced in the NAM, they present several drawbacks. The major drawback is that each proposed stamp introduces limit-variables and they must be taken as a limit to infinity once symbolic transfer functions are computed [8], [20], [21]. Therefore, valuable computer resources will be wasted in generating symbolic terms that will be pruned when the limits are applied on the symbolic expressions computed. On the other hand, following the same concept of limit-variables, the behavior of each controlled source in their fully-differential and single-ended versions can be modeled as VCCSs, as have already been reported in [21]-[24]. The difference of these stamps with those reported in [17]-[20], is that input-output impedances associated to each controlled source are taken into account. As a result, the behavior of any active device modeled with controlled sources can directly be introduced into NAM, including input-output impedances, and symbolic transfer functions are computed without loss of accuracy. The contribution of this paper is along the same line on the deduction of element stamps for those active devices mentioned above and as an extension of the works reported in [21]-[24]; thereby they can be used to directly fill the NAM, improving the CPU-time and memory consumption used during the compute of the symbolic transfer functions.

2. DDA Stamp

The DDA was proposed in [2] as a new active device. The symbolic representation is depicted in Fig. 1(a) and its equivalent model by using a VCVS is shown in Fig. 1(b). This amplifier handles voltage signals on its input terminals and a voltage difference on its output terminals. According to [23], [24], the stamp of the DDA is obtained as

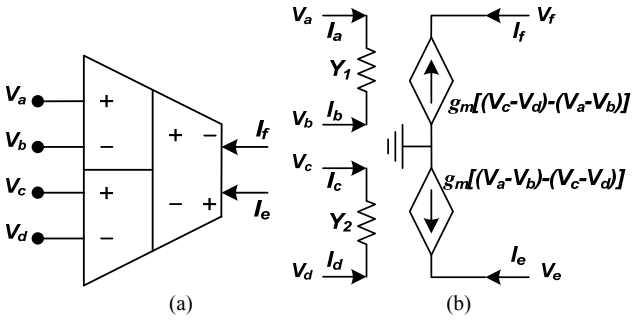


Fig. 2. (a) Symbol of the DDOFA, (b) equivalent model.

$$\begin{array}{c} \\ a \\ b \\ c \\ d \\ e \end{array}\begin{array}{c} \begin{array}{ccccc} a & b & c & d & e \end{array} \\ \begin{bmatrix} Y_1 & -Y_1 & 0 & 0 & 0 \\ -Y_1 & Y_1 & 0 & 0 & 0 \\ 0 & 0 & Y_2 & -Y_2 & 0 \\ 0 & 0 & -Y_2 & Y_2 & 0 \\ -A_vY_o & A_vY_o & A_vY_o & -A_vY_o & Y_o \end{bmatrix} \end{array}\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ V_e \end{bmatrix} = \begin{bmatrix} I_a \\ I_b \\ I_c \\ I_d \\ I_e \end{bmatrix} \quad (1)$$

where Y_1 and Y_2 are the input admittances, Y_o is the output admittance (ideally, $Y_o = \infty$) and A_v is the finite open-loop voltage gain. As one can see, (1) can be used to formulate the system of equations of analog circuits containing DDA by using standard NA. On the other hand, whether input admittances are considered as ideals (i.e., $Y_1 = Y_2 = 0$), (1) is simplified to

$$\begin{array}{c} \\ e \end{array}\begin{array}{c} \begin{array}{ccccc} a & b & c & d & e \end{array} \\ \begin{bmatrix} -A_vY_o & A_vY_o & A_vY_o & -A_vY_o & Y_o \end{bmatrix} \end{array}\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ V_e \end{bmatrix} = \begin{bmatrix} I_e \end{bmatrix}. \quad (2)$$

3. DDOFA Stamp

The DDOFA, whose symbol is shown in Fig. 2(a), has two differential input ports and provides two balanced output currents [3]. The equivalent model by using two VCCS is depicted in Fig. 2(b). This active device handles voltage signals on its input terminals and current signals on its output-terminals. According to [21], the stamp of the DDOFA can be deduced as

$$\begin{array}{c} \\ a \\ b \\ c \\ d \\ e \\ f \end{array}\begin{array}{c} \begin{array}{cccc} a & b & c & d \end{array} \\ \begin{bmatrix} Y_1 & -Y_1 & 0 & 0 \\ -Y_1 & Y_1 & 0 & 0 \\ 0 & 0 & Y_2 & -Y_2 \\ 0 & 0 & -Y_2 & Y_2 \\ -g_m & g_m & g_m & -g_m \\ g_m & -g_m & -g_m & g_m \end{bmatrix} \end{array}\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \end{bmatrix} = \begin{bmatrix} I_a \\ I_b \\ I_c \\ I_d \\ I_e \\ I_f \end{bmatrix} \quad (3)$$

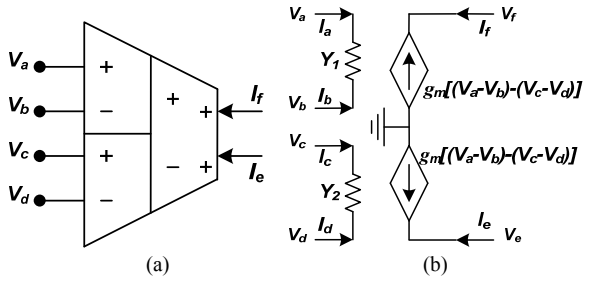


Fig. 3. (a) Symbol of the DDOMA, (b) equivalent model.

where Y_1 and Y_2 are the input admittances and g_m is the finite open-loop transconductance gain. As one see, (3) can immediately be used to formulate the NAM of analog circuits containing DDOFA. By considering ideal input admittances (i.e., $Y_1 = Y_2 = 0$), (3) is reduced to

$$\begin{array}{c} \\ e \\ f \end{array}\begin{array}{c} \begin{array}{cccc} a & b & c & d \end{array} \\ \begin{bmatrix} -g_m & g_m & g_m & -g_m \\ g_m & -g_m & -g_m & g_m \end{bmatrix} \end{array}\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \end{bmatrix} = \begin{bmatrix} I_e \\ I_f \end{bmatrix}. \quad (4)$$

4. DDOMA Stamp

The DDOMA has emerged as an alternate analog building block which inherits all the advantages of current mode techniques [4]. Basically, the behavior of the DDOMA is similar to the DDOFA, only that here, two current sources with the same direction are used on the output terminals. Note that the DDOFA and DDOMA are extended versions of the operational floating amplifier. The symbolic representation is depicted in Fig. 3(a) and its equivalent model by using two VCCS is shown in Fig. 3(b). Simple analysis of Fig. 3(b) allows obtaining a set of equations given by

$$\begin{array}{c} \\ a \\ b \\ c \\ d \\ e \\ f \end{array}\begin{array}{c} \begin{array}{cccc} a & b & c & d \end{array} \\ \begin{bmatrix} Y_1 & -Y_1 & 0 & 0 \\ -Y_1 & Y_1 & 0 & 0 \\ 0 & 0 & Y_2 & -Y_2 \\ 0 & 0 & -Y_2 & Y_2 \\ -g_m & g_m & g_m & -g_m \\ -g_m & g_m & g_m & -g_m \end{bmatrix} \end{array}\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \end{bmatrix} = \begin{bmatrix} I_a \\ I_b \\ I_c \\ I_d \\ I_e \\ I_f \end{bmatrix} \quad (5)$$

where Y_1 and Y_2 are the input admittances and g_m is the finite open-loop transconductance gain. Similarly as in previous section (i.e., $Y_1 = Y_2 = 0$), (5) can be reduced to

$$\begin{array}{c} \\ e \\ f \end{array}\begin{array}{c} \begin{array}{cccc} a & b & c & d \end{array} \\ \begin{bmatrix} -g_m & g_m & g_m & -g_m \\ -g_m & g_m & g_m & -g_m \end{bmatrix} \end{array}\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \end{bmatrix} = \begin{bmatrix} I_e \\ I_f \end{bmatrix}. \quad (6)$$

Therefore, (5) and (6) can be used to compute symbolic small-signal characteristics of analog circuits containing DDOMA by applying standard NA only.

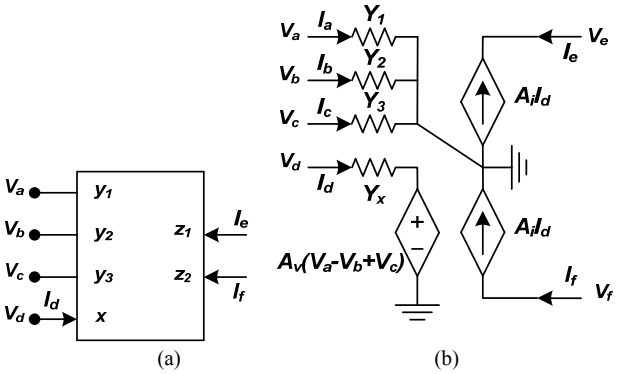


Fig. 4. (a) Symbol of the DDCC, (b) equivalent model.

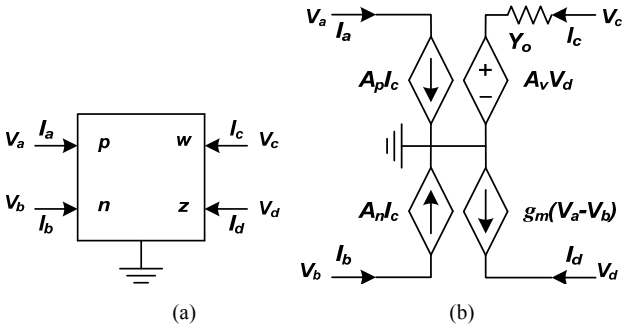


Fig. 5. (a) Symbol of the CBTA, (b) equivalent model.

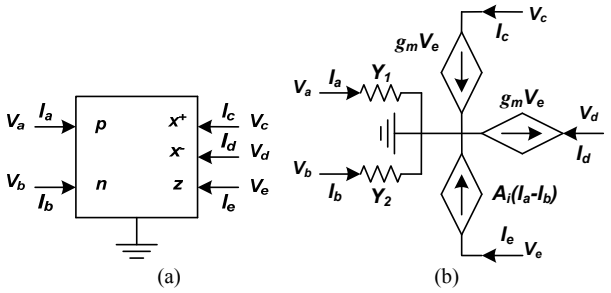


Fig. 6. (a) Symbol of the CDTA, (b) equivalent model.

5. DDCC stamp

The DDCC, whose symbol is depicted in Fig. 4(a), is a six-terminal network and its equivalent model by using controlled sources is shown in Fig. 4(b) [5]. This hybrid active device handles voltage and current signals on its input terminals and only current signals on its output-terminals. According to [21], [23]-[24] and analyzing each terminal of Fig. 4(b), the system of equations can be written as a general admittance matrix given by

$$\begin{array}{c} \\ a \\ b \\ c \\ d \\ e \\ f \end{array}\begin{array}{c} \begin{array}{cccc} a & b & c & d \end{array} \\ \begin{bmatrix} Y_1 & 0 & 0 & 0 \\ 0 & Y_2 & 0 & 0 \\ 0 & 0 & Y_3 & 0 \\ -A_vY_x & A_vY_x & -A_vY_x & Y_x \\ -A_iA_vY_x & A_iA_vY_x & -A_iA_vY_x & A_iY_x \\ A_iA_vY_x & -A_iA_vY_x & A_iA_vY_x & -A_iY_x \end{bmatrix} \end{array}\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \end{bmatrix}=\begin{bmatrix} I_a \\ I_b \\ I_c \\ I_d \\ I_e \\ I_f \end{bmatrix} \quad (7)$$

where Y_1, Y_2, Y_3 and Y_x (ideally, $Y_x = \infty$) are the input admittances, A_v and A_i are the finite open-loop voltage and current gains, respectively. By considering ideal input admittances (i.e., $Y_1 = Y_2 = Y_3 = 0$), (7) is reduced to

$$\begin{array}{c} \\ d \\ e \\ f \end{array}\begin{array}{c} \begin{array}{cccc} a & b & c & d \end{array} \\ \begin{bmatrix} -A_vY_x & A_vY_x & -A_vY_x & Y_x \\ -A_iA_vY_x & A_iA_vY_x & -A_iA_vY_x & A_iY_x \\ A_iA_vY_x & -A_iA_vY_x & A_iA_vY_x & -A_iY_x \end{bmatrix} \end{array}\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \end{bmatrix}=\begin{bmatrix} I_d \\ I_e \\ I_f \end{bmatrix}. \quad (8)$$

6. CBTA Stamp

The CBTA handles current signals at the input terminals and both voltage and current signals at its output terminals [6]. The circuit symbol of the CBTA is shown in Fig. 5(a) and its equivalent model by using controlled sources is depicted in Fig. 5(b). According to [21], [23], [24], the stamp of the CBTA can be deduced as

$$\begin{array}{c} \\ a \\ b \\ c \\ d \end{array}\begin{array}{c} \begin{array}{cccc} a & b & c & d \end{array} \\ \begin{bmatrix} 0 & 0 & A_pY_o & -A_pA_vY_o \\ 0 & 0 & A_nY_o & -A_nA_vY_o \\ 0 & 0 & Y_o & -A_vY_o \\ -g_m & g_m & 0 & 0 \end{bmatrix} \end{array}\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \end{bmatrix}=\begin{bmatrix} I_a \\ I_b \\ I_c \\ I_d \end{bmatrix} \quad (9)$$

where Y_o is the output admittance (ideally, $Y_o = \infty$), A_p, A_n and A_v are the finite open-loop positive-negative current and voltage gains, respectively; and g_m is the finite open-loop transconductance gain. As a consequence, (9) can directly be used to formulate the NAM of analog circuits containing CBTA.

7. CDTA Stamp

The CDTA handles currents in both input-output terminals [7]. Basically, it is a current operational amplifier with a complementary version on the *z*-terminal. The circuit symbol of the CDTA is shown in Fig. 6(a) and its equivalent model is depicted in Fig. 6(b). Again, according to [21], [23], [24], the stamp of the CDTA is given by

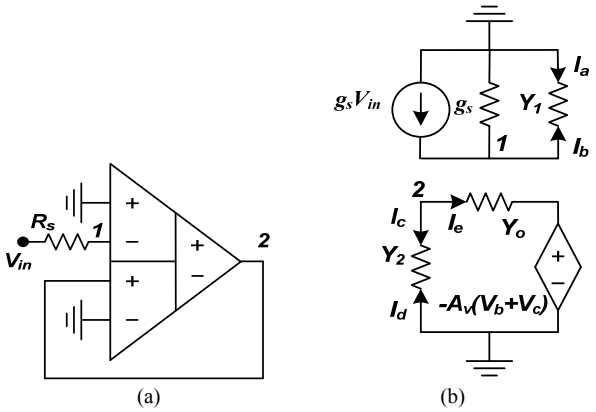


Fig. 7. (a) Voltage inverter, (b) equivalent circuit.

$$\begin{array}{c} \\ a \\ b \\ c \\ d \\ e \end{array}\begin{array}{c} \begin{array}{ccc} a & b & e \end{array} \\ \begin{bmatrix} Y_1 & 0 & 0 \\ 0 & Y_2 & 0 \\ 0 & 0 & g_m \\ 0 & 0 & -g_m \\ A_iY_1 & -A_iY_2 & 0 \end{bmatrix} \end{array}\begin{bmatrix} V_a \\ V_b \\ V_e \end{bmatrix}=\begin{bmatrix} I_a \\ I_b \\ I_c \\ I_d \\ I_e \end{bmatrix} \quad (10)$$

where Y_1, Y_2 are the input admittances (ideally, $Y_1 = Y_2 = \infty$), A_i is the finite open-loop current gain and g_m is the finite open-loop transconductance gain.

8. Illustrative Examples

In this section, examples are described to demonstrate the use of the proposed stamps in order to compute fully-symbolic small-signal characteristics of analog circuits containing DDA, DDOFA, DDOMA, DDCC, CBTA and CDTA. Let us begin with the simple topology show in Fig. 7(a) [2]. Its equivalent circuit by using Fig. 1(b) is depicted in Fig. 7(b). According to Fig. 7(b) and (2), a standard NA is applied and the system of equations is given by

$$\begin{bmatrix} g_s & 0 \\ A_vY_o & A_vY_o + Y_o \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}=\begin{bmatrix} g_sV_{in} \\ 0 \end{bmatrix} \quad (11)$$

where $Y_1 = Y_2 = 0$ are considered. From (11) the symbolic transfer function is computed as

$$\frac{V_2}{V_{in}} = -\frac{A_v}{1+A_v}. \quad (12)$$

As a second example, let us consider the DDOFA-based lossy differential integrator taken from [3] which is shown in Fig. 8(a). Its equivalent circuit is illustrated in Fig. 8(b). According to Fig. 8(b) and by applying (4), the NAM is given by

$$\begin{bmatrix} g_{s2} & 0 & 0 & 0 \\ 0 & g_{s1} & 0 & 0 \\ g_m & -g_m & g_1 - g_m & 0 \\ -g_m & g_m & g_m & g_2 + sC \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} g_{s2} V_2 \\ g_{s1} V_1 \\ 0 \\ 0 \end{bmatrix} \quad (13)$$

where $Y_1 = Y_2 = 0$ are considered. From (13) the output voltage is computed as

$$V_4 = \frac{V_1 - V_2}{C\left(R_1 - \frac{1}{g_m}\right)\left(s + \frac{1}{R_2 C}\right)}. \quad (14)$$

Let us now study the DDOMA-based differential voltage amplifier taken from [4] which is illustrated in Fig. 9(a) along with its equivalent model by using controlled sources shown in Fig. 9(b). According to Fig. 9(b), the NAM can be formulated using the stamp given by (6) as

$$\begin{bmatrix} g_{s1} & 0 & 0 & 0 \\ 0 & g_{s2} & 0 & 0 \\ 0 & 0 & g_1 + g_2 & -g_2 \\ -g_m & g_m & -(g_2 + g_m) & g_2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} g_{s1} V_p \\ g_{s2} V_n \\ 0 \\ 0 \end{bmatrix} \quad (15)$$

where $Y_1 = Y_2 = 0$ are again considered. Therefore, the output voltage is computed from (15) and given by

$$V_4 = \frac{R_1 + R_2}{\left(\frac{1}{g_m} - R_1\right)} (V_p - V_n). \quad (16)$$

A DDCC-based voltage-mode biquad filter taken from [5] is depicted in Fig. 10(a). Its equivalent circuit is illustrated in Fig. 10(b). By applying (8) in Fig. 10(b), the NAM is built as

$$\begin{bmatrix} g_s + Y_1 & 0 & 0 & 0 & 0 \\ 0 & sC_2 + Y_2 & 0 & -A_{i2}A_{v2}Y_{x2} & A_{i2}Y_{x2} \\ -A_{v1}Y_{x1} & A_{v1}Y_{x1} & g_1 + Y_{x1} & 0 & 0 \\ -A_{i1}A_{v1}Y_{x1} & A_{i1}A_{v1}Y_{x1} & -A_{i1}Y_{x1} & g_3 + sC_1 & 0 \\ 0 & 0 & 0 & -A_{v2}Y_{x2} & g_2 + Y_{x2} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix} = \begin{bmatrix} g_s V_{in} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (17)$$

Assuming $Y_1 = Y_2 = 0$, $Z_{x1} = 1/Y_{x1} = 0$ and $Z_{x2} = 1/Y_{x2} = 0$, the symbolic transfer functions for band- and low-pass responses are given by

$$\frac{V_4}{V_{in}} = \frac{s\frac{A_{i1}A_{v1}g_1}{C_1}}{s^2 + s\frac{g_3}{C_1} + \frac{A_{i1}A_{i2}A_{v1}A_{v2}g_1g_2}{C_1C_2}}, \quad (18)$$

$$\frac{V_2}{V_{in}} = \frac{\frac{A_{i1}A_{i2}A_{v1}A_{v2}g_1g_2}{C_1C_2}}{s^2 + s\frac{g_3}{C_1} + \frac{A_{i1}A_{i2}A_{v1}A_{v2}g_1g_2}{C_1C_2}}. \quad (19)$$

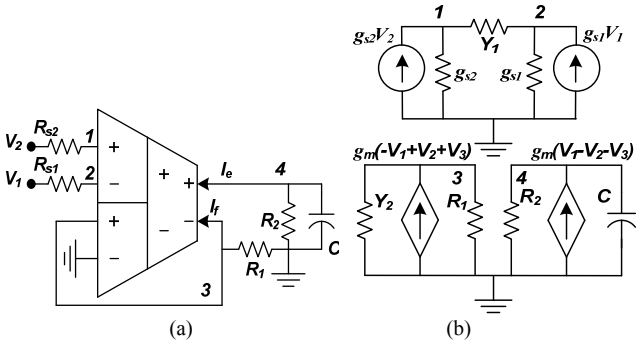


Fig. 8. (a) DDOFA-based differential integrator, (b) equivalent circuit.

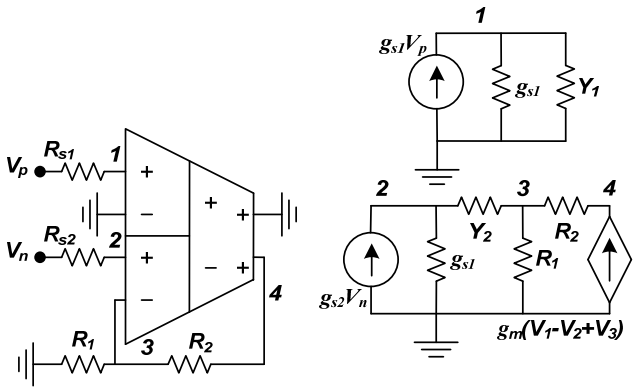


Fig. 9. (a) DDOMA-based differential voltage amplifier, (b) equivalent circuit.

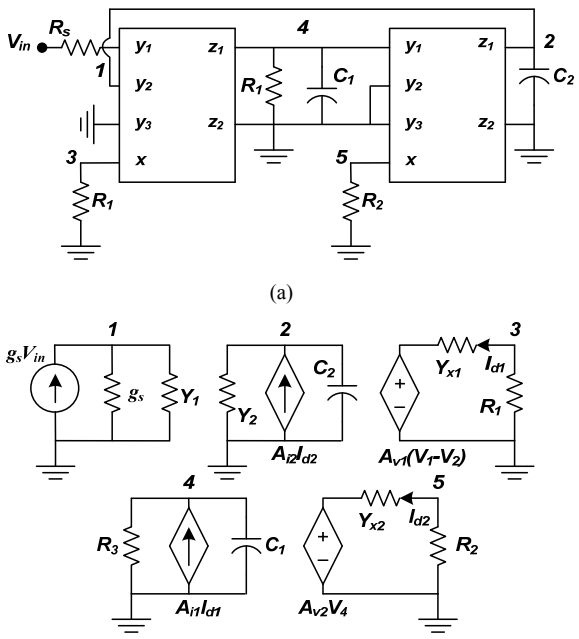


Fig. 10. (a) DDCC-based voltage-mode biquad filter, (b) equivalent circuit.

As a fifth example, we consider the CBTA-based oscillator taken from [25] which is shown in Fig. 11(a). Its equivalent circuit is illustrated in Fig. 11(b) with V_5 as output node. According to Fig. 11(b) and by applying (9), the NAM is given by

$$\begin{bmatrix} g_1 & 0 & A_pY_o & -A_pA_vY_o & 0 \\ 0 & g_1 & A_nY_o & -A_nA_vY_o & -g_1 \\ 0 & 0 & g_3+Y_o & -A_vY_o & 0 \\ -g_m & g_m & 0 & sC_2 & 0 \\ 0 & -g_1 & 0 & 0 & g_1+sC_1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix}. \quad (20)$$

Therefore, the characteristic equation for the oscillator circuit is given by

$$s^2 + s\frac{g_m A_v\left(A_nR_1 - A_pR_2\right)}{C_2(Z_o+R_3)} + \frac{A_nA_vg_m}{C_1C_2(Z_o+R_3)} = 0 \quad (21)$$

where $Z_o = 1/Y_o$ has been considered. From (21), the condition and frequency oscillation are computed as

$$A_nR_1 = A_pR_2, \quad f_o = \frac{1}{2\pi}\sqrt{\frac{A_nA_vg_m}{C_1C_2(Z_o+R_3)}}. \quad (22)$$

From (22), one can see that the condition oscillation can be controlled by R_1 or R_2, meanwhile the frequency oscillation is controlled by g_m or R_3. As a last example, let us consider the CDTA-based Kerwin-Huelsman-Newcomb (KHN) biquad taken from [26] and depicted in Fig. 12(a). Its equivalent circuit is illustrated in Fig. 12(b). By applying (10) in Fig. 12(b), the system of equations is given by

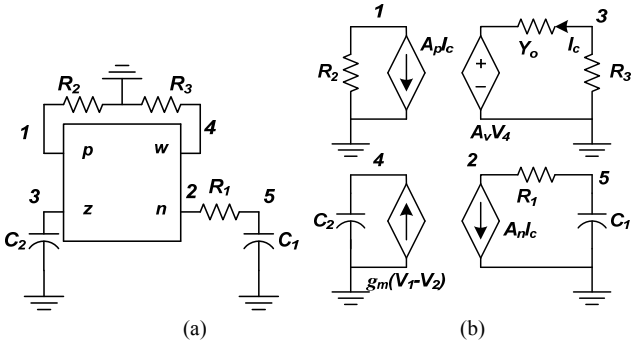
$$\begin{bmatrix} Y_2 & 0 & 0 & 0 & 0 & 0 \\ 0 & Y_1 & -g_{m1} & 0 & -g_{m2} & 0 \\ -A_{i1}Y_2 & A_{i1}Y_1 & sC_1 & 0 & 0 & 0 \\ 0 & 0 & g_{m1} & Y_3 & 0 & 0 \\ 0 & 0 & 0 & A_{i2}Y_3 & sC_2 & 0 \\ 0 & 0 & 0 & 0 & g_{m2} & Y_L \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} = \begin{bmatrix} I_{in} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (23)$$

Symbolic transfer functions for low-, band- and high-pass responses are given by

$$\frac{I_{Lp}}{I_{in}} = -\frac{\frac{A_{i1}A_{i2}g_{m1}g_{m2}}{C_1C_2}}{s^2 + s\frac{A_{i1}g_{m1}}{C_1} + \frac{A_{i1}A_{i2}g_{m1}g_{m2}}{C_1C_2}}, \quad (24)$$

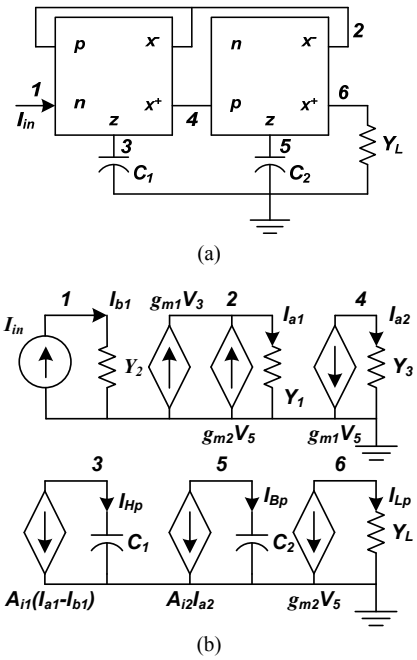
$$\frac{I_{Bp}}{I_{in}} = -\frac{s\frac{A_{i1}A_{i2}g_{m1}}{C_1}}{s^2 + s\frac{A_{i1}g_{m1}}{C_1} + \frac{A_{i1}A_{i2}g_{m1}g_{m2}}{C_1C_2}}, \quad (25)$$

$$\frac{I_{Hp}}{I_{in}} = -\frac{s^2A_{i1}}{s^2 + s\frac{A_{i1}g_{m1}}{C_1} + \frac{A_{i1}A_{i2}g_{m1}g_{m2}}{C_1C_2}}. \quad (26)$$



(a) (b)

Fig. 11. (a) Sinusoidal oscillator using CBTA, (b) equivalent circuit.



(a)

(b)

Fig. 12. (a) CDTA-based KHN filter, (b) equivalent circuit.

9. Summary and Conclusions

Symbolic analysis is a powerful tool which accelerates the electronic design process, since a symbolic expression that describes the behavior of a circuit gives information that is complementary to information supplied by numerical simulations [10]-[15]. In the past, several symbolic analyzers were proposed in order to compute symbolic performance parameters of electronic circuits [11], [12], [15]. In these analyzers, the MNA method was principally used to formulate the system of equations. However, the size of the admittance matrix and the number of nonzero elements increases by each controlled source used. For instance, whether the MNA formulation is applied in Fig. 10(b), the size of the matrix is 9×9 with 19 nonzero elements, which is larger and denser than (17). Therefore, the computational complexity and memory consumption is increased when recursive determinant-expansion techniques are applied in order to compute

performance parameters [14]. For the above reasons, other approaches to reduce the size of the system of equations have been reported in [13] and [15] and they are known as dead row and V/I methods. In the former method, the number of equations is equal to the number of independent nodes, similarly as NA. However, according to [15], the method is only useful for ideal active devices. In the latter, ideal active devices are again considered, and for the case of analog circuits containing ideal amplifiers, the number of equations is reduced by each amplifier. That is, the number of equations is equal or less than the number of independent nodes [13], [15]. In both methods, although the size of the system of equations is equal or less at comparison with the NAM by using the proposed method herein, only ideal active devices can be used. It is a serious drawback, since from the point of view of an analog designer, input-output impedances along with the gain must be included into the symbolic expressions to be computed, in order to obtain a behavioral model more realistic and accurate. Furthermore, one should be careful not only in the selection of the rows and columns to be omitted, but also in how to identify the signs of signed minors, when the determinant is computed [13], [15]. Moreover, new stamps for the CCCS and VCVS were recently proposed and they can be used to immediately include the behavior of any active device into the NAM [22]-[24]. As a consequence, not only smaller and less dense matrices can be obtained, as has already been demonstrated throughout the paper, but also the CPU-time and memory consumption used during the solution of the NAM are improved [8], [9]. It is worth mentioning that in the previous examples, a Norton equivalent was applied to transform the independent voltage sources to current sources. It is great advantage since this permits reducing the admittance matrix in one order. Furthermore, pathological equivalents of active devices have also been proposed at the literature [8], [9], [22], [27]-[31] with the target of reducing the size of the system of equations and improve the computation of symbolic expressions of a circuit. Even pathological elements have also been used in synthesis methods [20], [27], [28]. In addition, either the element stamp method or pathological elements can be used to reduce not only the size the NAM and the number of nonzero elements, but also the generation of cancelling-terms. Finally, the proposed stamps for modeling the behavior of active devices can easily be included in a CAD tool and, as result, symbolic performance parameters can be computed by applying a standard NA only. In this context, all the proposed stamps and those reported in [21], [23], [24], along with all the pathological equivalents of active devices reported in [8], [9], [22], are already implemented into a software called: Symbolic Analyzer and Design of Analog Integrated Circuits (SA^2IC), developed at the Autonomous University of Tlaxcala, Mexico.

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