

A Novel (DDCC-SFG)-Based Systematic Design Technique of Active Filters

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Abstract. *This paper proposes a novel idea for the synthesis of active filters that is based on the use of signal-flow graph (SFG) stamps of differential difference current conveyors (DDCCs). On the basis of an RLC passive network or a filter symbolic transfer function, an equivalent SFG is constructed. DDCCs' SFGs are identified inside the constructed 'active' graph, and thus the equivalent circuit can be easily synthesized. We show that the DDCC and its 'derivatives', i.e. differential voltage current conveyors and the conventional current conveyors, are the main basic building blocks in such design. The practicability of the proposed technique is showcased via three application examples. Spice simulations are given to show the viability of the proposed technique.*

Keywords

Signal-flow graphs, SFG-stamps, DDCC, DVCC, current conveyors, active filters.

1. Introduction

Realizing small size and low-cost ICs is an ever concern of analog designers. In ICs, integrated inductors are expensive in both terms: size and cost. Their elimination and replacement by equivalent active circuits was, and continues to be deeply investigated. The search for systematic, efficient and easy synthesis technique is of actuality [1]. The available literature offers a wide plethora of synthesis methods for the design of active networks (inductors, filters, oscillators, etc.), see for instance [1-5]. However, there still be a lack of systematic approaches for the design of such active circuits [1], [3].

Graphs are an interesting candidate for such approaches, since they may offer direct information about the circuit topology, as well as an easy and efficient way to synthesize new circuit topologies [6-10]. Graph-based synthesis techniques have been already investigated; see

for instance [8-16]. But the previously proposed approaches are quite complicated, delicate, hard to be adapted to handle ABBs (analog basic building blocks), and are not systematic.

In the following, we deal with signal-flow graphs and we propose their use for analog filter synthesis. We show that it is possible via the use of an equivalent SFG of a passive filter, or a direct manipulation of a filter's symbolic transfer function, to therein identify SFGs of current conveyors. We also show that the differential difference current conveyor (DDCC) can be considered as a versatile basic building block in the proposed technique. As a mean of fact, the active circuit can be constructed using DDCCs, DVCCs (differential voltage current conveyors), current conveyors (CCs), resistors and capacitors. (DVCCs and CCs can be considered as particular cases of DDCCs, as it is shown in the following).

It is worth mentioning that the literature offers a very large number of DDCC-based active filters, however for (almost) all the proposed papers there is no indication about the technique used to synthesize the proposed filters, see for instance [17-28]. Besides, the majority of these publications propose active networks encompassing floating components, i.e. [17-20], [23-28]. Ditto for the DVCC-based circuits, see for example [30-45].

Finally, it is to be highlighted that all the circuits we proposed exclusively use grounded passive components, thus, they are suitable for integration.

The rest of the paper is structured as follows. Section 2 explains the SFG-based approach and considers the cases of associating 'extended' SFGs to passive RLC basic circuits and handling symbolic transfer functions of active filters. Section 3 highlights the proposed idea of using basic SFG building blocks and the identification of DDCCs inside the constructed graphs. Three application examples are considered. Section 4 presents the synthesized active networks and shows the viability of the proposed technique via Spice simulations. Finally, Section 5 summarizes the work and gives some concluding remarks.

2. SFGs Associated to Active Filters

It was shown in [46], [47] that an inductor can be represented by a SFG in both the impedance and the admittance form. An equivalent SFG can be constructed where the classical inductor is replaced by one capacitor and two resistors, as it shown in Fig. 1. In the following, these equivalent SFGs will be used to construct SFGs of active filters.

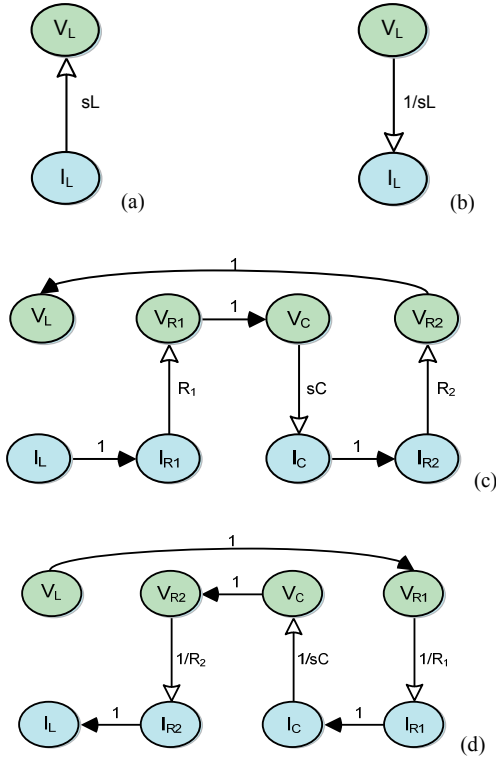


Fig. 1. (a): SFG of an ideal inductor (the impedance form).
 (b): SFG of an ideal inductor (the admittance form).
 (c): The equivalent SFG (the impedance form)
 $(V_L = \underbrace{s(R_1 R_2 C)}_{sL} I_L)$.
 (d): The equivalent SFG (the admittance form)
 $(I_L = \underbrace{(1/s(R_1 R_2 C))}_{1/sL} V_L)$.

Actually, the synthesis of an active filter can be performed on the basis of the use of a passive network, or directly by using the symbolic transfer function of a given filter. In the following we propose constructing SFGs and apply the proposed idea to both approaches.

2.1 SFGs of Equivalent Passive Networks

On the basis of a passive network, a signal-flow graph can be constructed (depending on the chosen tree and cotree elements). Then, the elementary SFG transmittances and vertices relative to the SFG of a classical inductor are replaced by the corresponding equivalent SFG, as intro-

duced above. The following two examples illustrate the technique.

- *Example #1: A serial RLC circuit.*

Let's consider the lossy serial LC-filter shown in Fig. 2. The circuit encompasses an independent voltage source. The inductor and the resistor are chosen to be in the tree branches, and the capacitor is, thus, placed in the cotree branch. Figures 3 and 4 give the corresponding SFG and the modified SFG associated with this circuit, respectively [47].

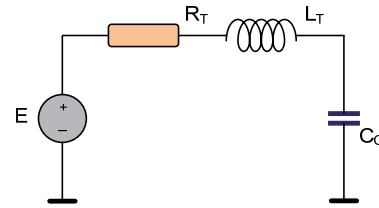


Fig. 2. A serial lossy LC-filter.

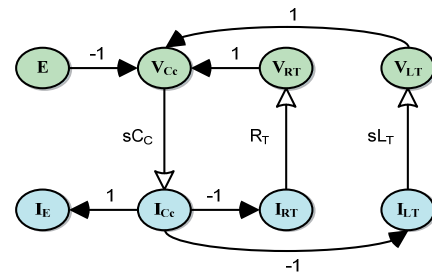


Fig. 3. The SFG associated with the circuit presented in Fig. 2.

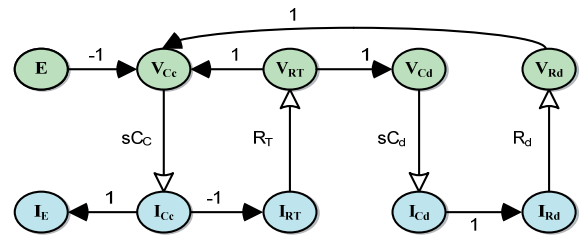


Fig. 4. The modified SFG of the one presented in Fig. 3.

- *Example #2: A fourth order band-pass RLC filter.*

Let's consider the lossy fourth order LC-filter shown in Fig. 5 [6]. Both inductors as well as the resistor R_2 are chosen to be in the tree branches. The direct representation of this circuit using SFGs is given in Fig. 6. Figure 7 depicts the corresponding modified SFG obtained by replacing the elementary SFG of each inductor by the equivalent SFG given in Fig. 1(c). A direct application of the *Mason* rule shows that both SFGs are equivalent, where $L_1 = R_{a1}R_{b1}C_{L1}$ and $L_2 = R_{a2}R_{b2}C_{L2}$.

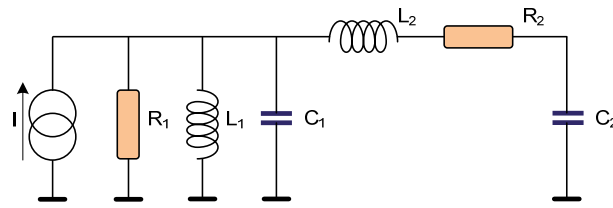


Fig. 5. A fourth order RLC filter.

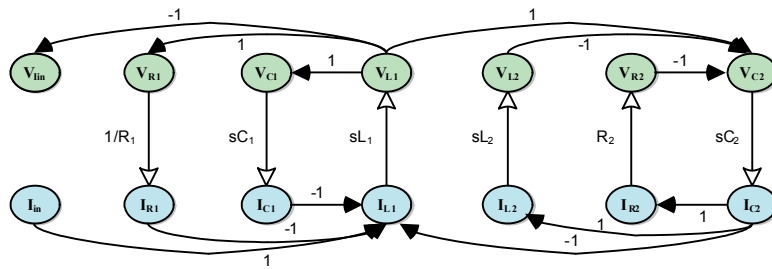


Fig. 6. The SFG associated with the circuit presented in Fig. 5.

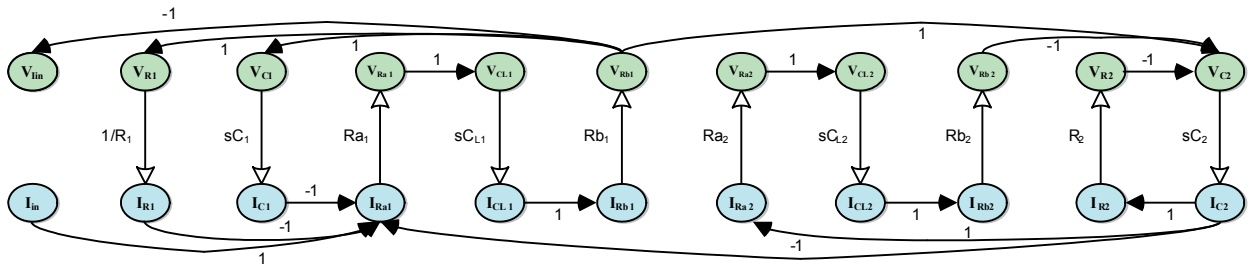


Fig. 7. The modified SFG of the one presented in Fig. 6.

2.2 SFGs Associated to the a Filter's Symbolic Transfer Function

It is also possible to construct a SFG of an active filter on the basis of its symbolic transfer function. Let us consider the following transfer function of a voltage mode multifunction filter (1). More than one SFG can be constructed and that reproduces the same transfer functions. Figure 8 presents one of them.

$$\begin{aligned}
 V_{HP} &= \frac{R_1 R_2 C_1 C_2 s^2}{D} V_{IN}, \\
 V_{LP} &= \frac{1}{D} V_{IN}, \\
 V_{BP} &= \frac{R_1 C_1 s}{D} V_{IN},
 \end{aligned}
 \tag{1}$$

with $D = R_1 R_2 C_1 C_2 s^2 + R_1 C_1 s + 1$.

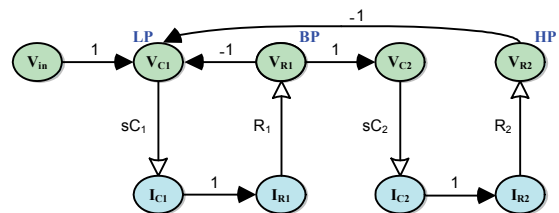


Fig. 8. The SFG associated to the transfer functions given in (1).

3. The Proposed Idea: BB-SFGs & DDCCs

An investigation of the SFGs shown in Fig. 7 and 8 (and others, such the ones in [46-48]), shows that these SFGs are mainly composed of two kinds of elementary SFGs. In a general representation, these elementary basic building SFGs (BB-SFGs) are shown in Fig. 9.

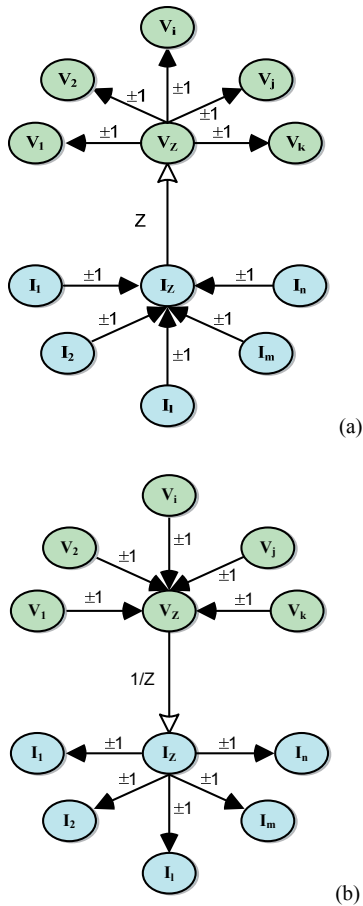


Fig. 9. The BB-SFGs.

Thus, two cases are possible: the BB-SFG of Fig. 9(a), and the BB-SFG of Fig. 9(b). For the former, it is relatively possible to be realized by simple parallel connections for the voltage vertex, and a direct node connection (KCL) for the case of the current vertex. However, things are different when realizing the BB-SFG given in Fig. 9(b); a signed sum has to be performed to get the value of the voltage vertex, and current mirrors/followers has to be used for the current vertex relations.

The differential difference current conveyor is a perfect candidate for the realization of the BB-SFG of Fig. 9(b). The DDCC is a variant of current conveyors (CCs), it was introduced in [49], where an N-type differential difference input stage was proposed. This stage allows performing the difference between two Y-input voltages, and applies it at the-X terminal of the CC. The corresponding circuit is shown in Fig. 10 (black lines). (in [36] $V_X = V_{Y1}^+ - V_{Y1}^-$, V_{Y2}^+ is grounded). Operating details of the differential difference input stage can be found in [23], [36]. Hence, it is possible to extend the number of voltage inputs by adding as many differential cells as necessary, as shown in grey color in Fig. 10. According to our experience, it is seldom necessary to have more than four input voltages, since it is rare to express the voltage of a cotree element with more than three or four tree element voltages. Regarding the current inputs, they can be easily realized by

adding current mirrors and/or current followers at the Z-terminal of the CC.

Expression (2) gives the general terminals relationships of the corresponding ‘extended’ DDCC. It is to be noted that if a unique positive and a unique negative input voltages are necessary, the corresponding circuit is known as a differential voltage CC; a DVCC. For the particular case of needing a unique positive input voltage, a classical CC can thus be used.

$$\begin{cases} I_{Zi}^+ = I_X \\ I_{Zi}^- = -I_X \\ V_X = \sum_i V_{Yi}^+ - \sum_j V_{Yj}^- \end{cases} \quad (2)$$

Figure 11 depicts the block representation of a multiple voltage input – multiple current output DDCC; a MIMO-DDCC.

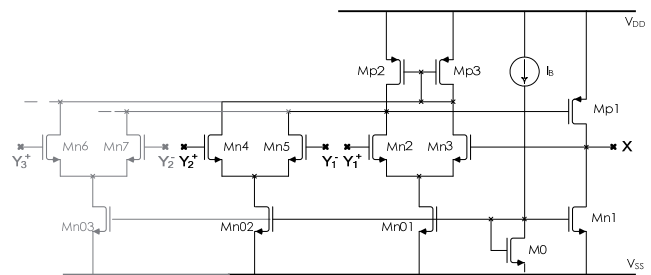


Fig. 10. The (extended) N-type differential difference voltage input stage.

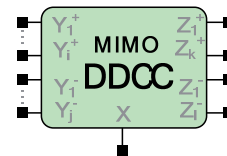


Fig. 11. The circuit symbol of a multiple voltage input – multiple current output DDCC.

Thus, the proposed idea consists of identifying the BB-SFGs of the DDCCs (eventually DVCCs / CCs) and then constructing the corresponding active circuit by simply connecting these ABBs and the passive components. This is detailed in the following section.

4. The Synthesized Circuits

- *Circuit #1:*

Figure 12 reproduces the SFG given in Fig. 4 and shows that it encompasses two BB-SFGs: one negative current output DDCC and one positive second generation CC (CCII+). The corresponding block circuit is given in Fig. 13. A routine analysis shows that the proposed circuit is correct. In order to further show the viability of the proposed circuit, Spice simulations were performed, they are shown in Fig. 14.

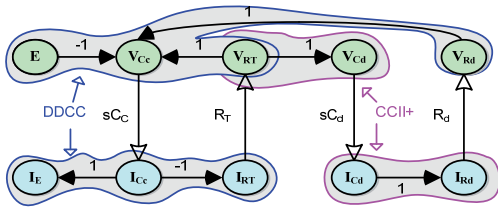


Fig. 12. The serial circuit equivalent SFG encompasses one DDCC and one CC.

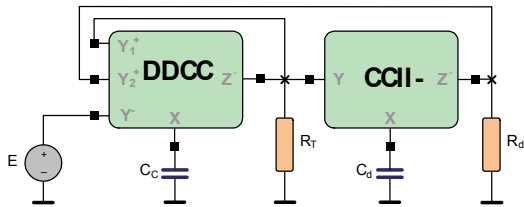


Fig. 13. The active equivalent lossy serial LC circuit (constructed on the basis of the SFG of Fig. 12).

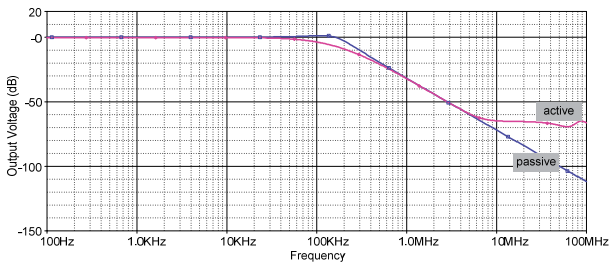


Fig. 14. Spice simulation results of the circuit shown in Fig. 13. $R_1 = R_d = 1 \text{ k}\Omega$, $C_d = C_c = 1 \text{ nF}$.

• *Circuit #2:*

Figure 15 reproduces the SFG given in Fig. 7 and shows that it encompasses four BB-SFGs: one MIMO-DDCC, one CCII+ and two CCII- (identified with different colors). The corresponding block circuit is given in Fig. 16. A routine analysis shows that the proposed circuit is correct. Corresponding Spice simulations are shown in Fig. 17.

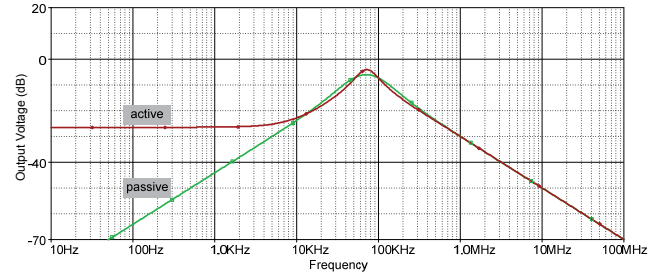


Fig. 17. Spice simulation results (low frequency difference between the curves is due to the non zero X-port resistance of the CCII-). $C_{L1} = C_{L2} = 1 \text{ nF}$, $C_1 = C_2 = 5 \text{ nF}$, $R_1 = R_{a1} = R_{b1} = R_2 = R_{a2} = R_{b2} = 1 \text{ k}\Omega$.

• *Circuit #3:*

A simple investigation of the SFG of Fig. 8 shows that the later encompasses one DVCC and one CCII. The corresponding constructed circuit is given in Fig. 18, and the Spice simulations of Fig. 19 show the viability of the proposed circuit.

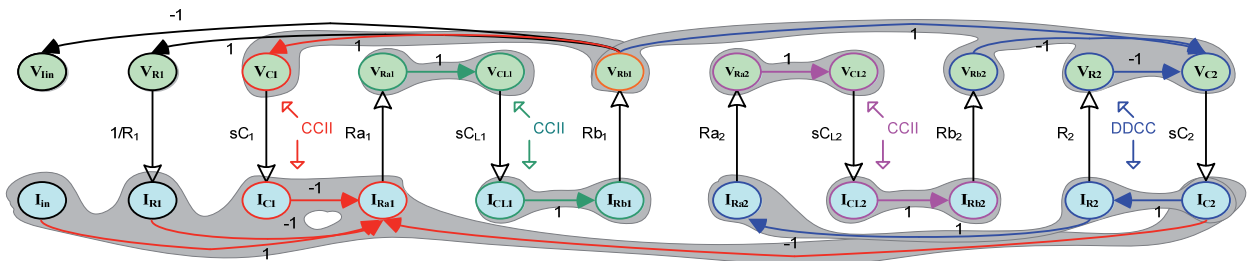


Fig. 15. The SFG of the expanded circuit (of Fig. 5) contains one MIMO-DDCC and three CCs.

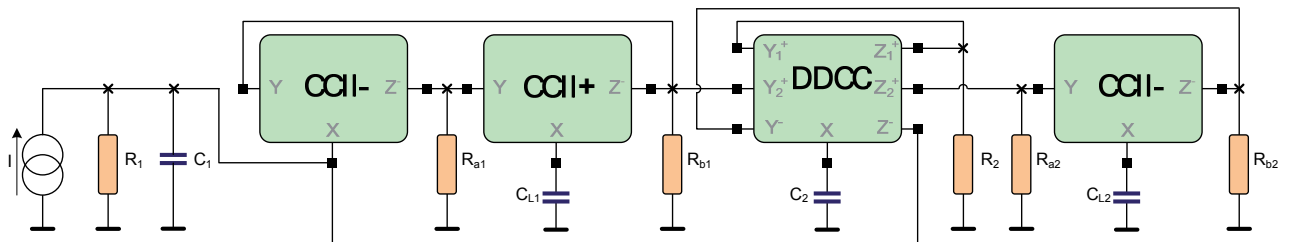


Fig. 16. The active filter constructed on the basis of the SFG of Fig. 15, according to the identified BB-SFGs.

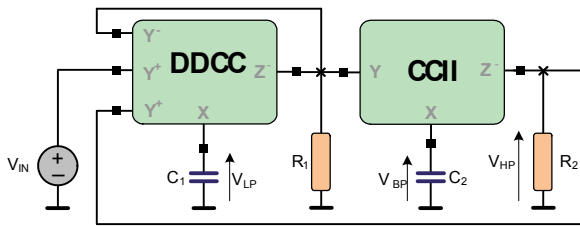


Fig. 18. The active circuit constructed on the basis of the SFG of Fig. 8.

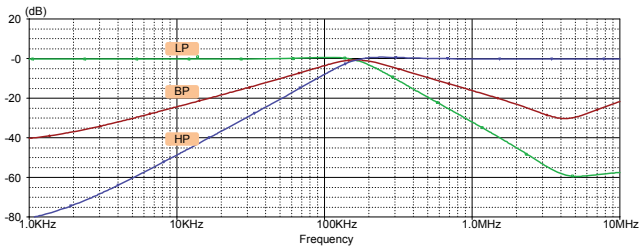


Fig. 19. Spice simulations of the active multi-function filter (of Fig. 17). $R_1 = R_2 = 1 \text{ k}\Omega$, $C_1 = C_2 = 1 \text{ nF}$.

5. Conclusion

The available literature offers a wide plethora of active filters. Current conveyors (CCs), differential voltage current conveyors (DVCCs) and differential difference current conveyors (DDCCs) were/are very widely used in such design. However, as it was highlighted in the paper, in most (or all) cases there is no indication on how these filters were synthesized! A lack of systematic, efficient and easy synthesis techniques exist. Besides, in most proposed networks floating passive components are used, making these circuits not adequate for integration. In this paper we proposed a novel, versatile, easy and efficient synthesis technique of active filters using signal-flow graphs (SFGs). We show that the DDCC (and consequently its derivatives, i.e. DVCCs and CCs) is a basic building block in such approach. We also show that the technique can be easily applied to both the RLC-passive basis and the symbolic transfer function basis, as well.

References

- [1] FAKHFAKH, M., TLELO-CUAUTLE, E., CASTRO-LOPEZ, R. (Eds.), *Analog/RF and Mixed-Signal Circuit Systematic Design*. Springer, 2013.
- [2] F. YUAN (Ed.) *CMOS Active Inductors and Transformers: Principle, Implementation, and Applications*. Springer, 2008.
- [3] TLELO-CUAUTLE, E. (Ed.) *Integrated Circuits for Analog Signal Processing*. Springer, 2013.
- [4] LO, T.-Y., HUNG, C.-C. *IV CMOS Gm-C Filters*. Springer, 2009.
- [5] COMER, D., COMER, D. (Eds.) *Advanced Electronic Circuit Design*. John Wiley & Sons, 2003.
- [6] FAKHFAKH, M., PIERZCHAŁA, M. Active filter design using a two-graph based transformation technique. Chapter 5, In: *Integrated Circuits for Analog Signal Processing*. Tlelo-Cuautle, E. (Ed.), Springer, 2013.
- [7] PIERZCHAŁA, M., FAKHFAKH, M. Transformation of LC-filters to active RC-circuits via the two-graph method. *Microelectronics Journal*, 2011, vol. 42, no. 8, p. 999–1005.
- [8] OZOGUZ, S., GÜNEŞ, E. O., ELWAN, H. O., TARIM, T. B. CCI-based balanced fully-integrated continuous-time current-mode filter synthesis: Signal-flow graph approach. In *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems*, 1998.
- [9] GÜNEŞ, E. O., ANDAY, F. Realisation of nth-order voltage transfer function using CCI+. *Electronics Letters*, 1995, vol. 31, p. 1022–1023.
- [10] BIOLEK, D., BAJER, J., BIOLKOVÁ, V., KOLKA, Z., KUBÍČEK, M. Z copy-controlled gain-current differencing buffered amplifier and its applications. *International Journal of Circuit Theory and Applications*, 2011, vol. 39, p. 257–274.
- [11] ZHANG, Q., WANG, C., SUN, J., DU, S. A new type of current conveyor and its application in fully balanced differential current-mode elliptic filter design. *Journal of Electrical Engineering*, 2011, vol. 62, no. 3, p. 126–133.
- [12] KOKSAL, M., SAGBAS, M. A versatile signal flow graph realization of a general transfer function by using CDBA. *International Journal of Electronics and Communication (AEÜ)*, 2007, vol. 61, p. 35–42.
- [13] GUINDI, R. S., ELMASRY, M. I. High-level analog synthesis using signal flow graph transformations. In *Proceedings of the IEEE International ASIC Conference and Exhibit*, 1995.
- [14] LIN, P. M. Signal flow graphs in filter analysis and synthesis. Chapter 21. In Lin, P. M. (Ed.) *Fundamentals of Circuits and Filters*. CRC Press, 2009.
- [15] ELES, P., KUCHCINSKI, K., PENG, Z., DOBOLI, A., POP, P. Scheduling of conditional process graphs for the synthesis of embedded systems. In R. Lauwereins, Madsen, J. (Eds.) *Design, Automation, and Test in Europe: The Most Influential Papers of 10 Years DATE*. Springer, 2008.
- [16] THULASIRAMAN, K. Graph theory. Chapter 7. In W.-K. Chen (Ed.) *Fundamentals of Circuits and Filters*. CRC Press, 2009.
- [17] IBRAHIM, M. A., KUNTMAN, H., CICEKOGLU, O. Single DDCC biquads with high input impedance and minimum number of passive elements. *Analog Integrated Circuits and Signal Processing*, 2005, vol. 43, p. 71–79.
- [18] IBRAHIM, M. A., KUNTMAN, H., CICEKOGLU, O. First-order all-pass filter canonical in the number of resistors and capacitors employing a single DDCC. *Circuits Systems Signal Processing*, Vol. 22, No. 5, 2003. pp. 525–536.
- [19] AGGARWAL, V. Novel canonic current mode DDCC based SRCO synthesized using a genetic algorithm. *Analog Integrated Circuits and Signal Processing*, 2004, vol. 40, p. 83–85.
- [20] YUCE, E. New low component count floating inductor simulators consisting of a single DDCC. *Analog Integrated Circuits and Signal Processing*, 2009, vol. 58, p. 61–66.
- [21] MAHESHWARI, S., GANGWAR, A. Versatile voltage-mode universal filter using differential difference current conveyor. *Circuits and Systems*, 2011, vol. 2, p. 210–216.
- [22] PANDEY, N., PAUL, S. K. Differential difference current conveyor transconductance amplifier: A new analog building block for signal processing. *Journal of Electrical and Computer Engineering*, 2011, vol. 2011, p. 1–10.

- [23] HORNG, J.-W., CHIU, T.-Y., JHAO, Z.-Y. Tunable versatile high input impedance voltage-mode universal biquadratic filter based on DDCCs. *Radioengineering*, 2012, vol. 21, no. 4, p. 1260–1268.
- [24] HORNG, J.-W., CHIU, W.-Y. High input impedance DDCC-based voltage-mode universal biquadratic filter with three inputs and five outputs. *Indian Journal of Engineering & Materials Sciences*, 2011, vol. 18, p. 183–190.
- [25] KRISHNA, P. V. S. M., KUMAR, N., SRINIVASULU, A., LAL, R. K. Differential difference current conveyor based cascaded voltage mode first order all pass filters. In *Proceedings of the International Conference on Circuits, Systems, Communications & Computers*, 2011.
- [26] KUMAR, M., KUMARI, R., SRIVASTAVA, M. C., KUMAR, U. Voltage mode notch filter using differential difference current conveyor (DDCC). In *Proceedings of SPIT-IEEE Colloquium and International Conference*, 2006.
- [27] IBRAHIM, M. A., MINAEI, S., YUCE, E., HERENC SAR, N., KOTON, J. Lossy/lossless floating/grounded inductance simulation using one DDCC. *Radioengineering*, 2012, vol. 21, no. 1, p. 3–10.
- [28] METIN, B., PAL, K., CICEKOGLU, O. All-pass filters using DDCC and MOSFET based electronic resistor. *International Journal of Circuit Theory and Applications*, 2011, vol. 39, no. 8, p. 881–891.
- [29] HORNG, J.-W., HOU, C.-L., CHANG, C.-M., CHOU, H.-P., LIN, C.-T. High input impedance voltage-mode universal biquadratic filter with one input and five outputs using current conveyors. *Circuits Systems Signal Processing*, 2006, vol. 25, no. 6, p. 767–777.
- [30] AGGARWAL, V., KILINC, S., CAM, U. Minimum component SRCO and VFO using a single DVCC. *Analog Integrated Circuits and Signal Processing*, 2006, vol. 49, p. 181–185.
- [31] HORNG, J.-W., HOU, C.-L., CHANG, C.-M., CHUNG, W.-Y. Voltage-mode universal biquadratic filters with one input and five outputs. *Analog Integrated Circuits and Signal Processing*, 2006, vol. 47, p. 73–83.
- [32] MINAEI, S., YUCE, E. All-grounded passive elements voltage-mode DVCC-based universal filters. *Circuits Systems and Signal Processing*, 2010, vol. 29, p. 295–309.
- [33] PANDEY, N., PAUL, S. K. VM and CM universal filters based on single DVCC. *Active and Passive Electronic Components*, 2011, p. 1–7.
- [34] HORNG, J.-W., HSU, C.-H., TSENG, C.-Y. High input impedance voltage-mode universal biquadratic filters with three inputs using three CCs and grounding capacitors. *Radioengineering*, 2012, vol. 21, no. 1, p. 290–296.
- [35] KHAN, M. Z., ANSARI, M. S. Digitally programmable voltage-mode universal biquadratic filter. *International Journal of Computer Applications*, 2012, vol. 54, no. 16, p. 26–31.
- [36] HU, J., XU, T., ZHANG, W. A CMOS rail-to-rail differential voltage current conveyor and its applications. In *Proceedings of the International Conference on Communications, Circuits and Systems*, 2005.
- [37] CHEN, H.-P., HUANG, K.-W., HUANG, P.-M. DVCC-based first-order filter with grounded capacitor. *International Journal of Information and Electronics Engineering*, 2012, vol. 2, no. 1, p. 50–54.
- [38] HASSAN, T., MAHMOUD, S. A. New CMOS DVCC realization and applications to instrumentation amplifier and active-RC filters. *International Journal of Electronics and Communication*, 2010, vol. 64, p. 47–55.
- [39] TEMIZYUREK, C., MYDERRIZI, I. A novel current-mode universal filter implemented with DVCCs. In *Proceedings of the International Conference on Microelectronics*, 2004.
- [40] CHANNUMSIN, O., PRASERTSOM, D., TANGSRIRAT, W. Single DVCC-based voltage-mode universal biquadratic filter. In *Proceedings of the International Conference on Information & Communication Technology, Electronic and Engineering*, 2010.
- [41] CHEN, H.-P., SHEN, S.-S. A versatile universal capacitor-grounded voltage-mode filter using DVCCs. *Journal of the Electronics and Telecommunications Research Institute*, 2007, vol. 29, no. 4, p. 470–476.
- [42] KAÇAR, F., UN, M. DVCC based current-mode first order all-pass filter and quadrature oscillator. *Trakya University Journal of Science*, 2007, vol. 8, no. 1, p. 01–05.
- [43] HORNG, J.-W. DVCCs based high input impedance voltage-mode first-order allpass, highpass and lowpass filters employing grounded capacitor and resistor. *Radioengineering*, 2010, vol. 19, no. 4, p. 653–656.
- [44] TANGSRIRAT, W., CHANNUMSIN, O. Voltage-mode multifunctional biquadratic filter using single DVCC and minimum number of passive elements. *Indian Journal of Pure & Applied Physics*, 2011, vol. 49, p. 703–707.
- [45] HORNG, J.-W. High input impedance first-order allpass, highpass and lowpass filters with grounded capacitor using single DVCC. *Indian Journal of Engineering & Material Sciences*, 2009, vol. 17, p. 1751–78.
- [46] FAKHFAKH, M., PIERZCHALA, M., RODANSKY, B. An improved design of VCCS-based active inductors. In *Proceedings of the International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design*, 2012.
- [47] PIERZCHALA, M., FAKHFAKH, M. Generation of active inductor circuits. In *Proceedings of the IEEE International Symposium on Circuits and Systems*, 2010.
- [48] PIERZCHALA, M., FAKHFAKH, M. Design of settable active lossy inductors. Chapter 14. In Fakhfakh, M., Tlelo-Cuautle, E., Castro-Lopez, R. (Eds.) *Analog/RF and Mixed-Signal Circuit Systematic Design*. Springer, 2013.
- [49] ELWAM, H., SOLIMAN, A. M. Novel CMOS differential voltage current conveyor and its applications. *IEE Proc. Circuits Devices and Systems*, 1997, vol. 144, no. 6, p. 195–200.

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