A Three-Dimensional DRAM Using Floating Body Capacitance Cells in an FD-SOI Process

Xuelian LIU, Aamir ZIA

Dept. of Electrical & Computer System Engineering, Rensselaer Polytechnic Institute, 110, 8th street, 12180 Troy, NY

liux11@rpi.edu, ziaa@rpi.edu

Abstract. *This paper describes a three-dimensional DRAM in which the floating body capacitance (FBC) of a fully depleted SOI (FD-SOI) device is used as a storage node. This 1T DRAM lends itself particularly well to a 3D wafer-to-wafer bonding process because of the absence of deep etched and filled trench capacitor structure, and the improved thickness control tolerance in wafer thinning. A novel three-tier, 3D, 1T embedded DRAM is presented that can be vertically integrated with a microprocessor, achieving low cost, high-density on-chip main memory. A 394 Kbits test chip has been designed and fabricated using the Lincoln Labs 3-Tier 3D 0.18 um fully depleted SOI CMOS process where an earlier (and previously reported) successful 3D SRAM was obtained. The measured retention time under holding conditions in this 180 nm process is greater than 10 ms. The test chip measures an access time of 50 ns and operates at 10 MHz.*

Keywords

Capacitor-less 1T DRAM, embedded DRAM, FD-SOI, floating body cell, memory stack, 3-D integration.

1. Introduction

The main memory presents a major performance bottleneck in modern computer systems because of the memory wall problem wherein the speed of the off-chip main memory lags behind the speed of the processor by several orders of magnitude. This problem is popularly referred to as the Memory Wall [1]. Conventional main memory usually consists of a large DRAM organized as multiple DIMMs (Dual Inline Memory Modules) that are external to the processor. The limitations of on-board inter-chip communication severely handicap the speed of data transport between the processor and the external memory. Power dissipated by pad drivers for this chip-to-chip transport at high speed is not insignificant. 3D chip stacking is a technology that can reduce or eliminate DRAM DIMMs needed external to the processor, thereby improving the speed (and width) of data transfer between the memory and the processor while reducing the physical board size and the length of board level interconnections that remain to be implemented using conventional packaging. Hence, three-dimensional (3D) integration can reduce main memory latency, reduce driver power, and possibly reduce packaging costs, especially if the 3D process can be made sufficiently simple and economical for batch processing. Deep trench capacitors, often used as a storage node in DRAM cells, are an impediment towards 3D integration of DRAM because of their varying trench depths and the associated wafer thinning challenges that they pose. This makes the prospect of avoiding the deep trench capacitor as a storage node particularly attractive from a 3D processing standpoint. As lithography pushes towards 22 nm, fabrication costs are expected to climb because of a steep increase in the cost of fabrication facilities, the cost of a mask set, and turn-around times [2]. Vertical memory densification is a promising approach in that it offers the potential to reduce both footprint and interconnect length without shrinking the transistor size [3].

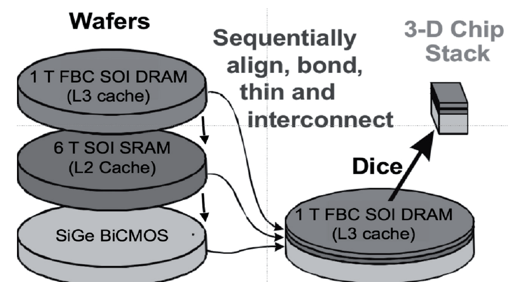


Fig. 1. Schematic drawing showing a vertical 3D stack of SRAM and DRAM memory wafers on a SiGe HBT BiCMOS processor wafer.

Fig. 2. 3D Visualization picture rendering of the three tiers in the MIT-Lincoln Labs 3D process.

The large numbers of vertical vias made possible by monolithic 3D processing (e.g. wafer to wafer bonding) can be utilized in several ways. At the very least, multiple blocks of data can be transferred from main memory to a lower level cache in one memory access cycle. This could approach several thousand gigabits of parallel transfer bandwidth; all done without pad drivers, package parasitic or ESD(electrostatic-discharge), with extremely low skew, and low total delay [4]. There are already publication in the DRAM design using TSV based stacking [5], [6], which are based on the SDRAM cell and planer DRAM cell.

Fig. 1 shows the 3D wafer bonded approach to integration of a SiGe BiCMOS processor, placed at the bottom tier, with a SOI SRAM and DRAM tiers stacked on top of it. One or more tiers of SRAM can be used as cache, due to superior access time. However, for large footprint code or data intensive applications, large amounts of DRAM are needed. Some of the authors predicted 3D memory chip stack performance in papers [7], [8], [9] and implemented a 3D SRAM with ultra-wide data bus used as L2 cache in paper [10] using a 180 nm 3 tier 3D FDSOI process developed by Lincoln Labs as shown in Fig. 2. The 3D DRAM design, which is another part of the 3D memory-processor stack, is presented in this paper.

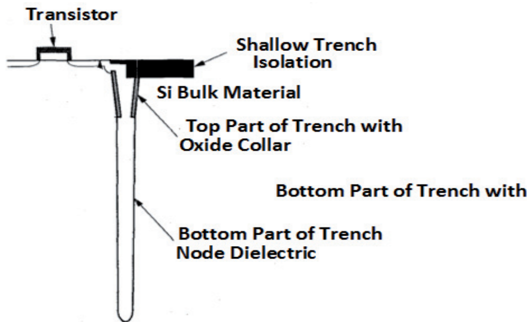


Fig. 3. Schematic representation of the deep trench capacitor showing how the trench protrudes deep into the substrate.

The standard DRAM cell comprises a small transistor and a large capacitor (1T + 1C). However, it is becoming difficult for standard DRAM to be scaled down because of its small cell size and high operation speed. DRAM industry is making prominent effort to address the scalability of the cell capacitor while maintaining the minimum capacitance needed for state discrimination immune to noise (C~25fF/cell) [11]; To achieve the capacitance requirement, the DRAM cells have evolved from the initial planar configuration [12] to three-dimensional structures SDRAM (stacked capacitors [13]) or deep trench capacitors [14]. This change leads to more process steps, and consequently, less process compatibility with logic devices. The increment in complexity and the size difference between the transistor and capacitor of each cell have motivated the search for a DRAM substitute able to outperform the 1T+1C cells in terms of simplicity and scalability. Also, in efforts to achieve very large memories, such a 1T-1C topology, present key challenges in integration of the storage capacitor while simultaneously achieving short access time and very high density. The deep trench as shown in Fig. 3 is also problematic for wafer thinning in 3D fabrication using the wafer-to-wafer bonding approach. This is due to the protrusion of the trench capacitor far into the substrate, where wafer over-thinning can damage the capacitor tips. Additionally, in stand-alone DRAM applications, the impact of eliminating the capacitor process should be around 20~ to 30% of the total process cost [15].

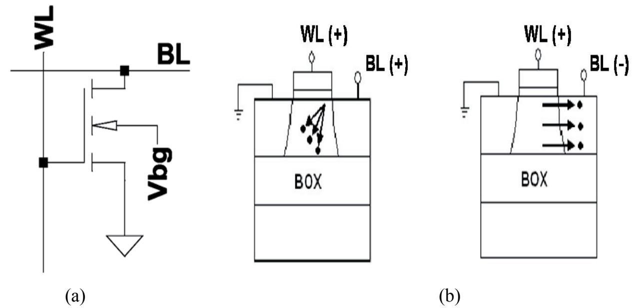


Fig. 4. DRAM operation: (a) Schematic drawing of a DRAM, (b) Write operation for “1” and “0” in an SOI FET Floating Body Cell.

A single transistor gain cell whose floating body serves as a data storage node is one of the candidates for small and scalable DRAM cells in the near future [16]-[18]. Fig. 4(a) shows the circuit diagram of such a DRAM cell. The concept of the cell which we named the floating body cell (FBC) can be realized by a MOSFET on bulk silicon [18], a PD-SOI (Partially Depletion SOI) MOSFET [16], [17] or FD-SOI MOSFET [19], [20], [21]. SOI devices are particularly suited in DRAM design for both low voltage and low leakage power [22], [23]. When the gate length scales down, the retention time decreases significantly because not only the partial depletion degrades the device performance, but also the number of storage charges in the floating body decreases with gate length. As a result, a double gate SOI MOSFET [24], [25] and a FinFET [26], [27], PiFET [28], Fully Depleted Polysilicon TFTs [29] can be a possible substitutes for this capacitorless DRAM design. A Novel Capacitorless DRAM Cell Using Superlattice Bandgap-Engineered (SBE) Structure with 30-nm Channel Length presented in [30] is also another possibility to implement the capacitorless DRAM.

In such a topology, sometimes also called ZRAM, the elimination of the trench capacitor offers a two-fold advantage of higher memory density and a vastly improved suitability for integration in 3D processing. Another benefit would be the ability to realize the memory in a digital logic process, as embedded DRAM, resulting in excellent compatibility with processor logic and reduction in costs of mask generation. However, there are some issues mainly needed to be solved in the ZRAM design, one major concern in the capacitorless DRAM is the reliabilities. There-

fore, there has been no verification of the performance of high-density mass commercial memories using the cell. The requirements of large enough, functional with a reasonable redundancy and completely free from any possible disturbance should be met when this capacitorless DRAM goes to product; also there are yield problems especially due to the realization of a compact-sized 3-D LSI as discussed in [6]. During 3-D intergradation, each functional wafer should be thinned. However, this may cause severe degradation in device reliability. Inter-tier redundancy and Intra-tier redundancy are employed in order to increase the yield of the chip [10].

In this paper, a three-dimensional DRAM in which the floating body capacitance (FBC) of a fully depleted SOI (FD-SOI) device is used as a storage node is explored. This paper not only presents the capacitor-less FD-SOI DRAM design but also integrates the design in 3D process, which is the novelty of this paper.

The paper is organized as follows. The principle of 1T DRAM cell is presented in Section 2. Section 3 explores the key features of a 0.18 um fully depleted SOI CMOS process that we use to design our 3D-DRAM chip. In Section 4, typical write, read and hold mode operation conditions are given based on simulations. Section 5 discusses the detailed circuit design and circuit architecture. In Section 6, both simulation result and measured result of the fabricated chip are shown. This paper ends with the conclusion in Section 7.

2. Principle of Operation

Depending on the condition of the thin film during operation, SOI CMOS devices are classified into two categories: (1) partially depleted (PD) and (2) fully depleted (FD) as shown in Fig. 5.

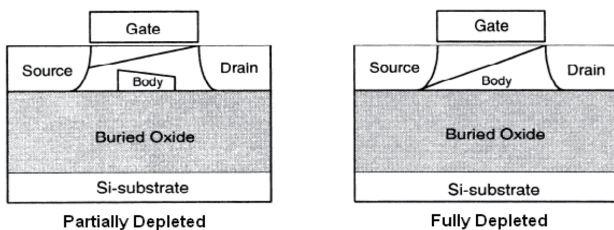
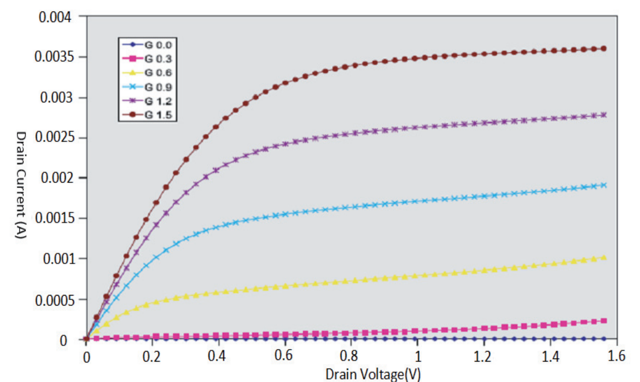


Fig. 5. Simplified cross-section of PD and FD SOI.

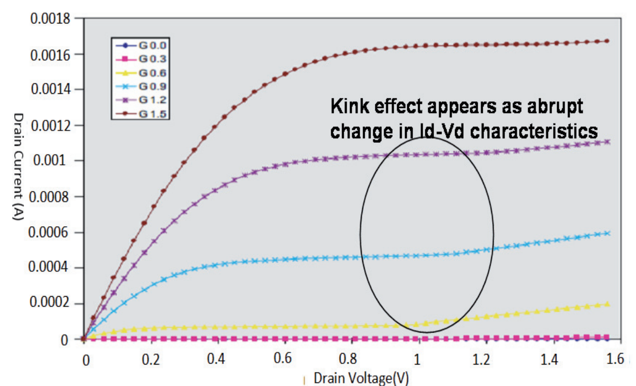
In a PD device, the depletion region extends into its thin film under the gate at source-body and drain-body junctions but it does not deplete all of the charge in the body. For an FD device, the thickness of the thin film is smaller than PD devices resulting in full depletion of body under all bias conditions. The write operation for the 1T DRAM cell with floating body capacitor is depicted in Fig. 4(b). The write '1' operation is achieved by creating a positive charge in the transistor body using the impact ionization mechanism. Both the word line (WL) gate voltage and the bit line source voltage are raised high, whereupon impact ionization creates positive charges within the body, where they stay trapped while the word line is low. A high gate voltage and low drain forward biases the body-drain junction, thereby removing the holes trapped in the body; this corresponds to a write '0'. The read operation is performed by operating the transistor in the linear region and comparing the drain current against that of a reference cell.

3. 3D Process

The process of 3D wafer scale integration using wafer-bonding process as done by MIT Lincoln Lab (MITLL) entails assembling of the 3D circuit from separate FD-SOI wafers, each of which is independently fabricated [31]. Fig. 2 shows 3D Visualization picture rendering of the three tiers in the MIT-Lincoln Labs 3D process. The bottom wafer acts as a handle wafer. Etching to remove the substrate of the second wafer is done after stacking and aligning. The buried oxide (BOX) of the upper tier FD-SOI wafer acts as etch stop. The same process is then repeated for the top wafer. Vertical interconnects, known as 3D vias, are etched to provide connections between stacked wafers.



(a) 0.2 µm



(b) 0.5 µm

Fig. 6. I-V characteristics of FD-SOI NMOS transistors.

In this process, these inter-wafer 3D vias are 1.75 µm square and 3 µm deep and they connect top-level metal of the first wafer to that of the second wafer and, first level

metal of the second wafer to top-level metal of the third wafer. These 3D vias are then filled with tungsten plugs to form electrical interconnections. The depth of 3 µm is much thinner than the deep trench capacitor's depth (4.5 µm) presented in paper [32].

As stated above, MITLL's 3D process involves wafer level stacking of fully depleted FD-SOI CMOS wafers. In this process, the NMOS transistors exhibit minor kink effect in their IV characteristics when the channel length is comparatively long (0.5 µm or more). The kink, which is a consequence of the stored charge in the floating body of the SOI transistor, an effect we utilize to design the DRAM cell, is not apparent in devices with small gate lengths. Fig. 6 illustrates the IV characteristics of the FD-SOI NMOS transistor with channel lengths 0.2 µm and 0.5 µm, with small kink effect appearing only in the latter.

4. Design Consideration

Since fully depleted SOI devices exhibit minimal floating body effect as compared to partially depleted SOI transistors, exploiting this effect for charge storage in FD-SOI devices is challenging. Several methods have been proposed to generate memory effect in these devices by creating a potential well in the thin body [19], [20] or creating a dip in device transconductance [33], [34]. All these methods require control of back gate voltage to obtain suitable bias conditions for proper operation. In a 3D integrated chip, back gate control is not available since the backside of all the wafers, except for the bottom one, are removed by thinning the substrate to the BOX layer prior to bonding with the other wafers that form the stack. Therefore, we need a different methodology to create memory effect in 3D FDSOI circuits. As discussed above, floating body effects in MITLL's process devices appear only when channel length is at least 0.5 µm, and they become more significant with increasing channel length. Moreover, device robustness improves with increasing channel width. This creates a tradeoff between robustness and cell density. We choose a channel length of 1 µm and width of 6 µm as a balance between the two. Simulations were performed to find the biasing conditions under which body charge storage can be maximized. Fig. 7 illustrates impact ionization current as a function of drain voltage. Although this current is higher with higher drain voltage, it must be kept somewhat below transistor's oxide breakdown voltage. Fig. 8 depicts change in body voltage with gate voltage. It can be seen that body voltage is maximum at 0.58 V. For writing a "0", the stored charge in the body has to be removed. This can be done by applying a zero or negative voltage to the drain. For a read, the transistors operated in the linear region with very low drain voltage so as not to minimize the amount of charge in the body. Fig. 9 shows the ID-VD characteristics of a 0.18-µm SOI NMOS in the bottom tier, which has back gate control in MITLL's FDSOI process, with negative backgate voltage. As shown in Fig. 9, based on the different body potential, the current sensed from the cell is different, and this current difference is maximized when drain voltage is biased around 0.2 V to 0.75 V. Based on these observations, memory operating voltages shown in Tab. 1 are derived. The device substrate is kept grounded at all time.

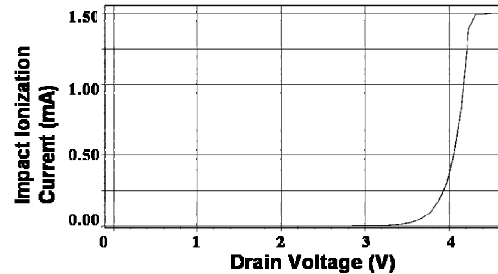


Fig. 7. Impact ionization current vs. drain voltage (L = 1 µm).

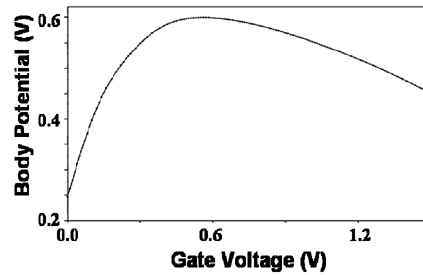


Fig. 8. Body voltage vs. gate voltage (L = 1 µm).

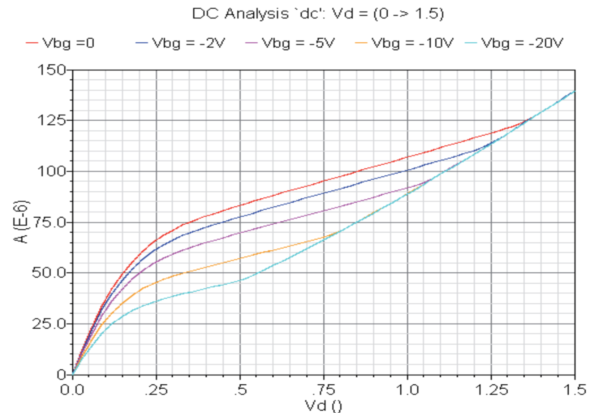


Fig. 9. I-V plot of the 3D FDSOI device.

Terminal	Writing "1"	Writing "0"	Hold	Reading
VG (V) (WL)	0.58	1.5	0	0.6
VD (V) (BL)	3.6	0	0	0.3

Tab. 1. Memory operation condition.

5. Circuit Design

Fig. 10 illustrates the array architecture of the 3D

FDSOI DRAM. Word lines are joined at the top tier with row decoder present only on that tier as shown in Fig. 12.

Fig. 11 depicts block level circuit diagram of a single DRAM cell with peripheral circuitry. Key challenge in the circuit design is to generate accurate and stable reference voltages at the drain and gate of the cell. For writing a "1", 3.6 volts need to be applied at the drain of the transistor. Dickinson type of charge pump is used to generate that voltage. Fig. 13 depicts its circuit schematic and transient response. In this process, diodes are realized in active region by blocking silicide formation using poly or NOSLC (silicide protection) layer.

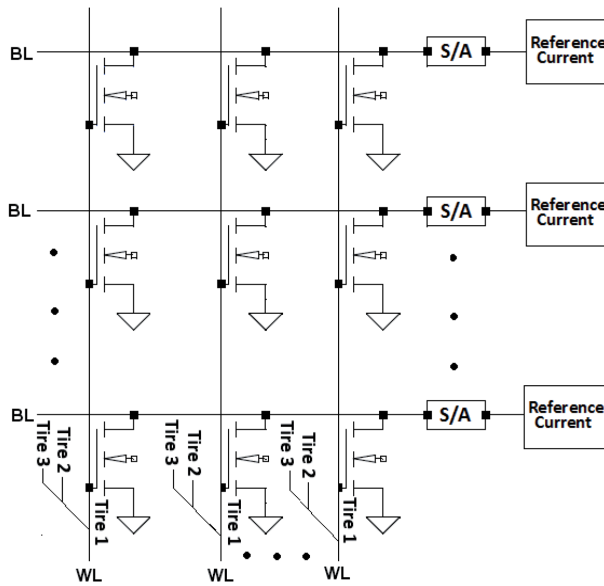


Fig. 10. Array architecture of the 3D 1T DRAM.

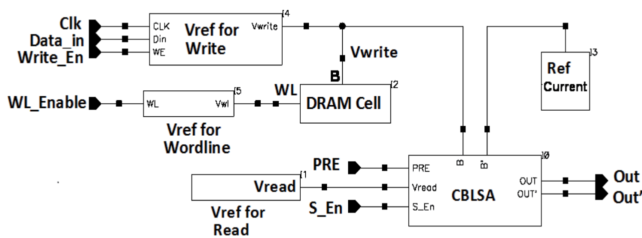


Fig. 11. Block level circuit diagram of a single cell.

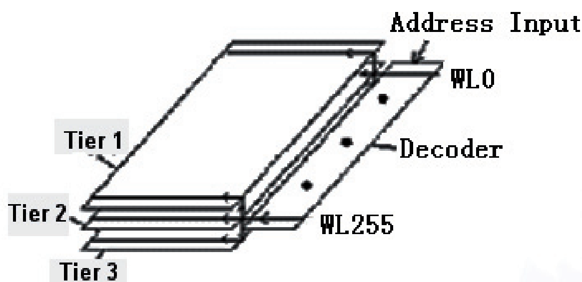
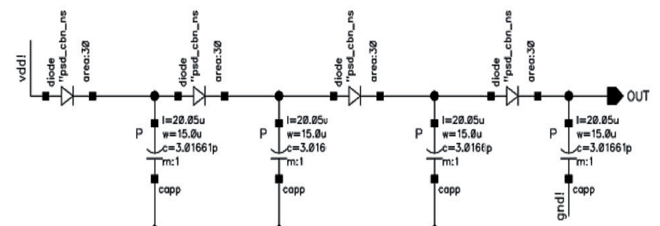
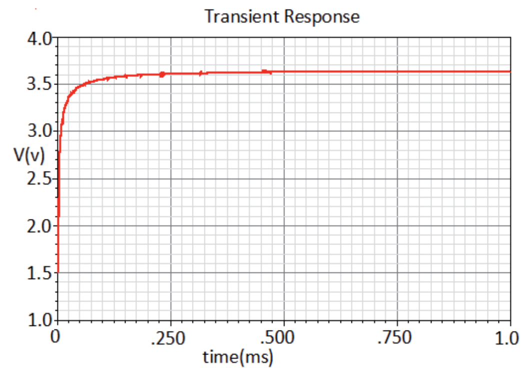


Fig. 12. Bank arrangement in the 3D memory.

With the operating voltages mentioned in Tab. 1 at room temperature, the cell current is estimated to be between 157uA and 114uA for logic "1". It is expected to vary from 90uA to 72uA for logic "0". Fig. 14 shows the simulated statistical distribution of the source currents for the two different memory states at room temperature for different memory cells. For the same memory state, different memory cells have read currents that differ significantly. Fig. 15 illustrates the clamped bit-line sense amplifier (CBLSA) [35] that is used to compare memory cell current with the reference current. Transistors M1-M4 form a latch with cross-coupled inverters. M5 and M6 are biased in the linear region and provide low impedance tie up to the bit lines. The circuit operation is completed in two phases. The first phase is precharging which begins by asserting PRE1 and PRE2 to high. This equalizes the input and output nodes. During this phase, Vread is set to 0.3 V and S_En is asserted high to facilitate drain bias (Vread) to the selected memory cell. At the start of second stage, the wordline of the selected memory cell is activated and at the same time PRE1 is released. After a short while, S_En, Vread and PRE2 are also asserted low. At this point, M1 and M2 act as low impedance common gate amplifiers and the latch use positive feedback to convert the current difference between M1 and M2 into sense amplifier output. Fig. 16 illustrates the transfer characteristics of the CBLSA. It displays a metastable range of 20µA. Beyond 110µA and below 90µA, the sense amplifier provides correct output.



(a) Dickinson type charge pump used to generate voltage.



(b) Transient behavior of the charge pump.

Fig. 13. Dickinson charge pump circuit design.

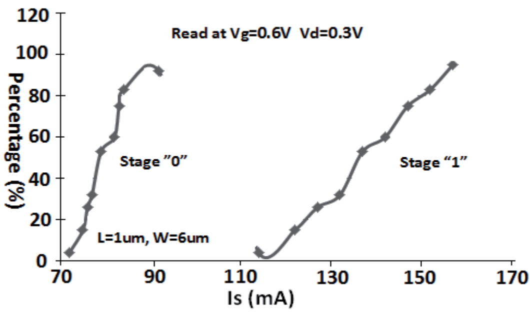


Fig. 14. Statistical distribution of the source current corresponding to the "0" and "1" states.

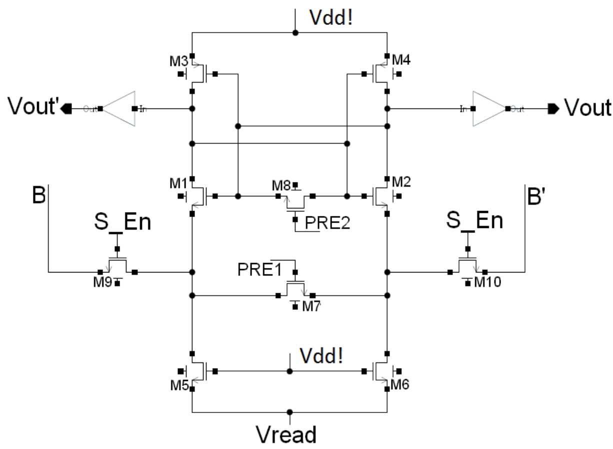


Fig. 15. Schematic of the sense amplifier.

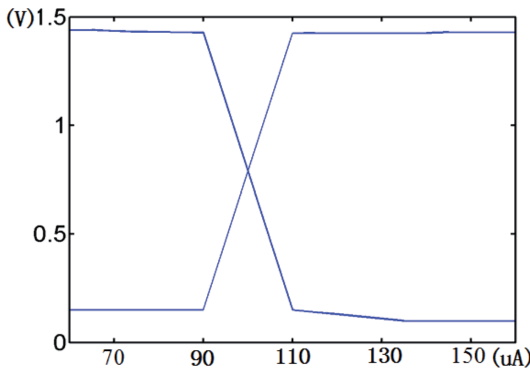
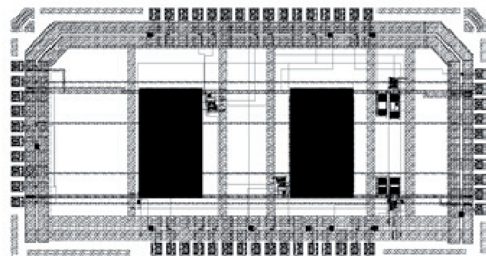


Fig. 16. Transfer characteristics of the CBLSA.

6. Result

The 3D embedded DRAM has been fabricated using a 0.18 μm, 3D FD-SOI process with three levels of metal. The memory consists of multiple arrays of 256 × 256 cells. The nominal supply voltage is 1.5 V for this process. Fig. 17 shows the layout and the micrograph of the fabricated chip. The chip has a dimension of 2.5 mm × 5 mm and with 1.5 V voltage supply. As we can see from the layout, there are 2 arrays in each tier. So there are totally 6 arrays in three tiers of fabricated chip. Fig. 18 shows the section of the layout of DRAM array. 3D vias are 1.75 μm square and 3 μm deep. These 3D vias are then filled with tungsten plugs to form electrical interconnections. Fig. 19 shows the simulation waveforms of Read and Write of "0" and "1" to a single DRAM cell. In this simulation, read and write cycles are both 50 ns. Although, read cycle can be completed in 5 ns(depending upon the current margin), write "0" is a major limiting factor in this design due to slow removal of holes from the body. On the other hand, write "1" can be completed successfully in 5 ns and has been verified by simulations. The 'Vout' waveform in Fig. 19 will AND with the 10 MHz system clock waveform to get the clear read result for each read section. Fig. 20 shows the measured waveform of successively READ output port from the continuously changed word line address of the DRAM verifying correct operation. The test waveforms show the highest working frequency of DRAM chip is 10 MHz, consistent with simulation. The chip has 95% function bit yield, and Fig. 21 shows the Fail count of 394 Kbit when different voltages are applied to test chip.



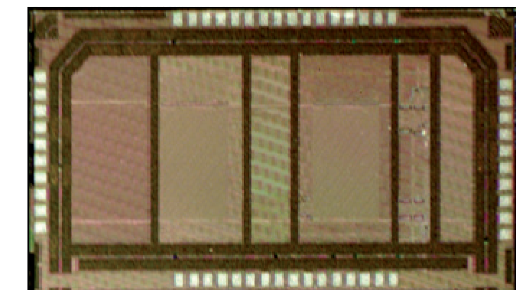


Fig. 17. Layout and micrograph of the 3D capacitorless DRAM chip.

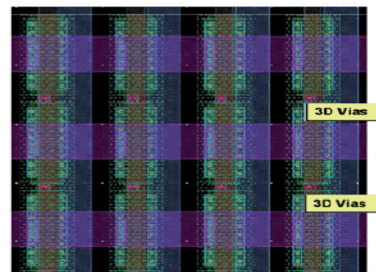


Fig. 18. Section of the layout of DRAM array.

In order to estimate the noise margin of the memory cell, simulations were performed with varying operating

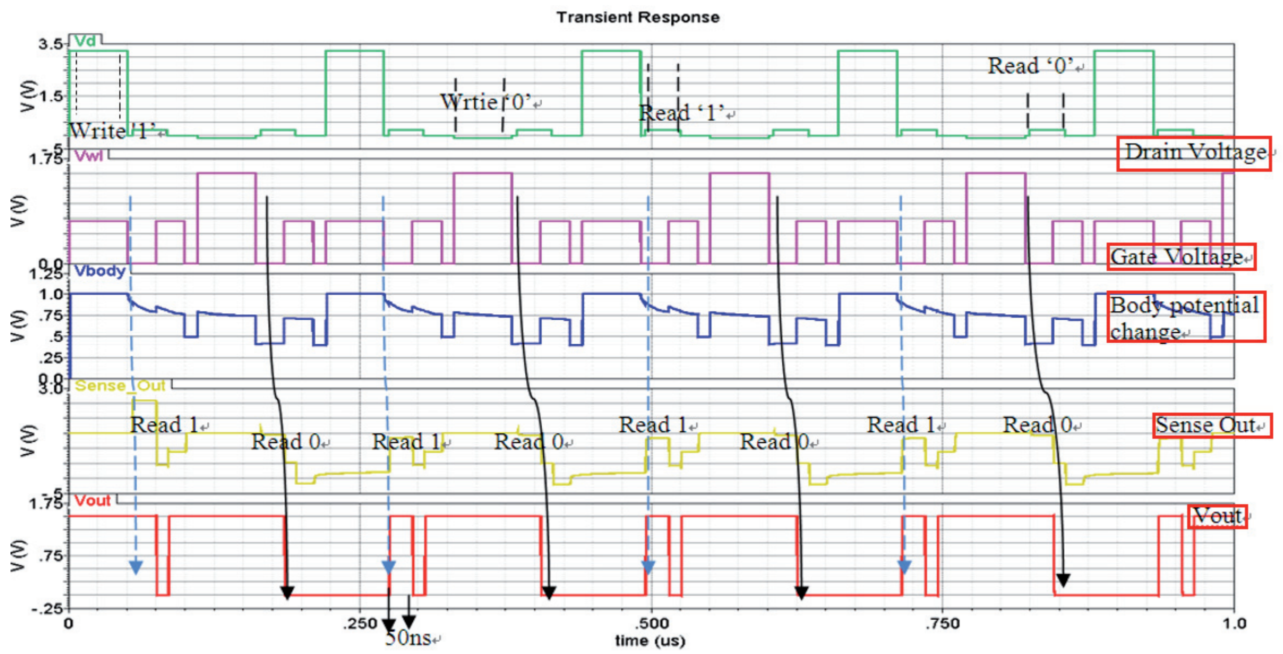


Fig. 19. Simulation waveforms of Write and Read from a single cell of the 1T DRAM.

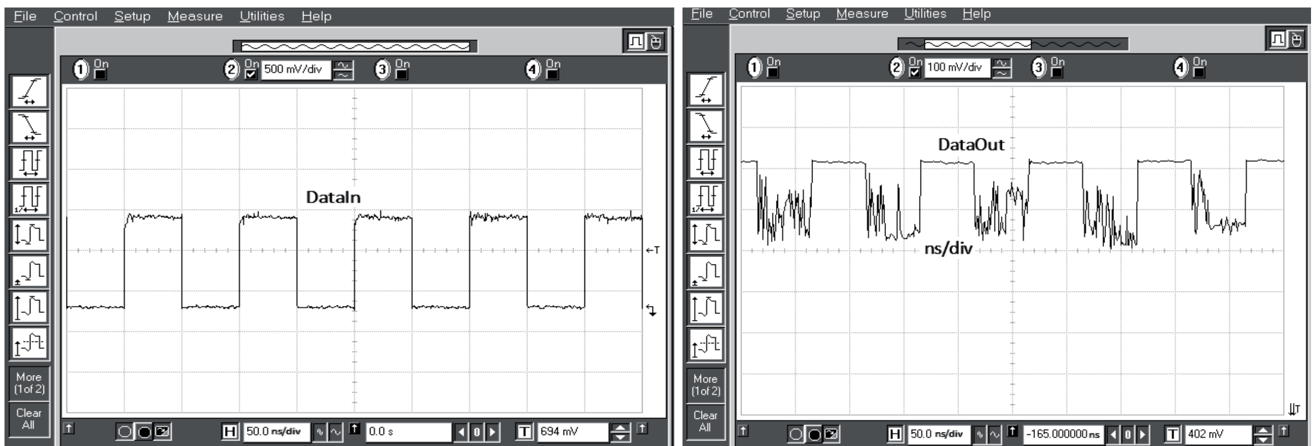


Fig. 20. Measured waveforms of read from Tier 1 of the 3D-DRAM chip for 1010 pattern.

conditions. Fig. 22 shows the change in cell current with varying temperature. It can be seen that cell current for both logic levels decreases significantly with increasing temperature. The noise margin (difference between min current with "1" stored and max current with "0") also decreases from about 60 µA to less than 40 µA. Fig. 23 illustrates the retention characteristics of the 1T DRAM in HOLD state. It was simulated by first writing the data value to the memory cell and then doing a READ after some time. Transistor current for logic "1" drops to 110 µA after 10 mS which is within 20 µA away from the current representing a "0", so the transistor is still working in the safety margin.

Fig. 24 represents the retention characteristics while READ operation. This was simulated by continuously reading a memory cell while noting its cell current. The cell current for logic "1" becomes equal to that for logic "0" after about more than 20 µs, which is more than enough to complete a READ operation. It is apparent that this DRAM is not non-destructive. To ensure stability of stored data, it is suggested that every READ should be followed by a refresh. Also, for optimal performance, it is suggested that each DRAM cell should be periodically refreshed after 3 msec.

The charge stored at the storage node of a FD-SOI based DRAM is small. It was therefore expected that the sense amplifier would be particularly sensitive to noise induced from nearby circuits. The layout of the DRAM included planned topographical variations in the position of the sense amplifier with respect to the DRAM cells and the

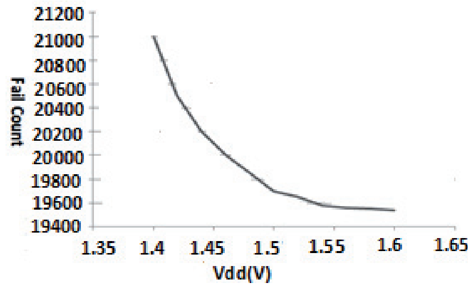


Fig. 21. Fail count of 394 Kbit DRAM with Vdd.

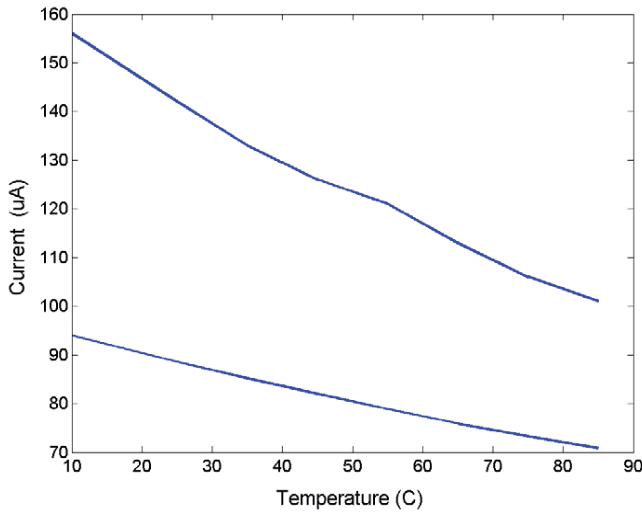


Fig. 22. Cell current variation with temperature.

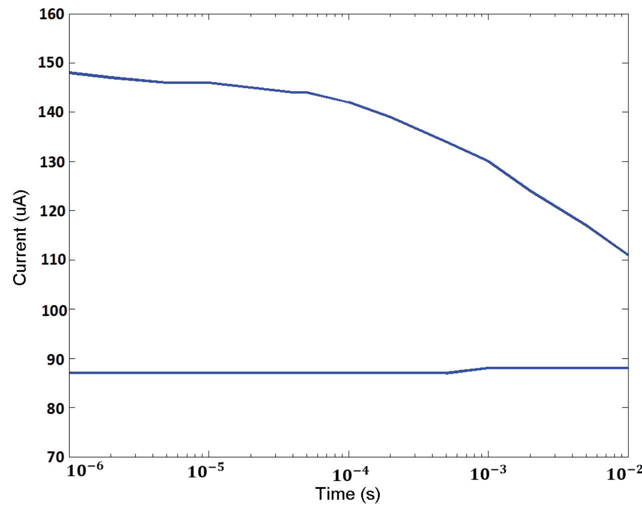


Fig. 23. Hold retention characteristics.

peripheral circuitry. It was found through various variations that the layout isolating the sense amplifier from peripheral circuitry such as read/write voltage generation circuits while keeping it close to the DRAM cells functioned correctly. For some other arrangements it did not, and the output was noisy. Consequently, sense amp. placement and layout is critical. The redundancy circuits also are included in the chip. It is incorporated at two levels. The first one, that might be called intra-tier redundancy, is the conventional use of redundant columns and/or rows to replace some defective part of the data array on the same tier. The second scheme, that might be called inter-tier redundancy, can be introduced by employing redundant arrays on a given tier, which might be made operational in case of massive defects in data sub-arrays on other tiers. All the above strategies increase the yield of the DRAM chip. Tab. 2 summarizes the measured characteristics of the 3-D DRAM chip described in this paper.

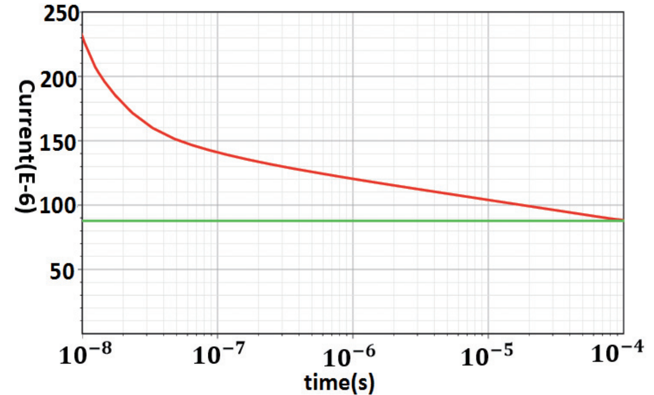


Fig. 24. Read retention characteristics of the floating body memory.

Technology	0.18-um 3D FD-SOI CMOS with 3 levels of metal
Supply Voltage	1.5 V
Area	2.5 mm × 5 mm
Operation Frequency	10 MHz
Access Time	50 ns
Chip organization	256 × 256 each bank, 3 tiers, 2 banks each tier, totally 394 kbits

Tab. 2. Chip summary of 3-D DRAM.

The 1-T DRAM cell scales well to 32 nm and beyond due to its litho-friendly nature and electrical characteristics that improve in an array implementation with scaling [36]. A 2 ns read latency reported from similar 1T DRAMs fabricated using 45 nm devices [37]. It is to be noted that PD-SOI devices offer an inherent advantage over FD-SOI devices in being used as a charge storage node because of the greater floating body effect in the PD-SOI devices [38]. This makes the possibility of developing a 3D integration process for PD-SOI devices very attractive; particularly from the standpoint of designing embedded 1T DRAM with short read-write latencies to improve the speed for the DRAM design, which is the limit of this paper.

7. Conclusion

Three-dimensional capacitor-less DRAM presents an approach that can be used to realize high-performance high-density DRAM not possible by any other way. FDSOI

transistors are used as memory cells and a novel scheme is proposed for writing to the cell. Simulations are performed to characterize the memory cell robustness under variations in operating conditions. Measured and simulation result with existing 180 nm 3D FDSOI are demonstrated in this paper.

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About Authors ...

Xuelian LIU received her Bachelors in Electrical Engineering from Xi'an Jiaotong University, China in 2003, and her MS degree in Electrical Engineering from Shanghai Jiaotong Univeristy, China in 2006. She is currently pursuing the Ph.D degree in the Department of Electrical, Computer and Systems Engineering at Rensselaer Polytechnic Institute. Her research interests include memory circuit design, high-speed digital circuit design, and RF circuit design.

Aamir ZIA received the B.Sc. degree in Electrical Engineering from the University of Engineering and Technology, Lahore, Pakistan, and the M.S. degree in Electrical Engineering from the University of Oklahoma, Norman. He gets the Ph.D. degree from the Department of Electrical, Computer, and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY. He currently is research associate in the Rensselaer Polytechnic Institute. His research interests include circuits and architectures for high-performance memories, 3-D IC technology, SOI and SiGe BiCMOS circuit.