A Low-Voltage Electronically Tunable MOSFET-C Voltage-Mode First-Order All-Pass Filter Design

Bilgin METIN[1], Norbert HERENCSAR[2], Oguzhan CICEKOGLU[3]

[1]Dept. of Management Information Systems, Bogazici University, Hisar Campus, 34342 Bebek-Istanbul, Turkey
[2]Dept. of Telecommunications, Brno University of Technology, Technicka 3082/12, 616 00 Brno, Czech Republic
[3]Dept. of Electrical and Electronics Engineering, Bogazici University, 34342-Bebek-Istanbul, Turkey

bilgin.metin@boun.edu.tr, herencsn@feec.vutbr.cz, cicekogl@boun.edu.tr

Abstract. *This paper presents a simple electronically tunable voltage-mode first-order all-pass filter realization with MOSFET-C technique. In comparison to the classical MOSFET-C filter circuits that employ active elements including large number of transistors the proposed circuit is only composed of a single two n-channel MOSFET-based inverting voltage buffer, three passive components, and one NMOS-based voltage-controlled resistor, which is with advantage used to electronically control the pole frequency of the filter in range 103 kHz to 18.3 MHz. The proposed filter is also very suitable for low-voltage operation, since between its supply rails it uses only two MOSFETs. In the paper the effect of load is investigated. In addition, in order to suppress the effect of non-zero output resistance of the inverting voltage buffer, two compensation techniques are also introduced. The theoretical results are verified by SPICE simulations using PTM 90 nm level-7 CMOS process BSIM3v3 parameters, where ±0.45 V supply voltages are used. Moreover, the behavior of the proposed filter was also experimentally measured using readily available array transistors CD4007UB by Texas Instruments.*

Keywords

Analog signal processing, all-pass filter, output resistance compensation techniques, first-order filter, inverting voltage buffer, loading effect, MOSFET-C filter, MOS resistive cell, tunable filter, voltage-mode.

1. Introduction

Electronically tunable circuits attracted significant attention in the design of analog integrated circuits, since tolerances of the electronic components in integrated circuit (IC) realization in practice are unacceptably high and thus after manufacturing fine-tuning is necessary. The most commonly used tunability approaches are the following: Firstly, the operational transconductance amplifier (OTA) can be mentioned, which is widely used in the design of electronically tunable circuits, since its transconductance gain (g_m) can be varied through an external bias current [1]–[3]. After the current-controlled conveyor (CCCII) was introduced by Fabre *et al*. [4], a new period has been opened with respect to electronic tunability in the analog filter design. Here the parasitic/intrinsic X-input terminal resistance of the CCCII is controlled via an external bias current allowing electronic tunability to some current conveyor-based filter topologies. Another technique is given in [5]–[8], where the current and/or voltage gains of active building blocks (ABBs) are used for tuning purposes. In [9]–[23], MOS resistive circuits or metal-oxide semiconductor field effect transistor-C (MOSFET-C) filters were proposed. In MOSFET-C technique, the resistors are replaced with MOSFETs such that distortions, due to MOSFET non-linearities, are canceled and voltage-controlled resistors (VCR) are obtained. In the classical MOSFET-C approach the filters are composed of operational amplifier (Op-Amp)-based integrator blocks, where each of them is individually linearized [9], [10]. Also, beside Op-Amps, other ABBs are used in the design of MOSFET-C filters [10], [12], [14], [17], [20]. It is worth noting that all the above mentioned tunability methods require an active element that includes large number of transistors.

In this study, a two n-channel MOSFET-based inverting voltage buffer (IVB) is used in the design of MOSFET-C filter in contrast to circuits that require an active elements that are composed of large number of transistors [9]–[23]. The two NMOS-based IVB is employed in the realization of the MOS resistive cell (MRC) in [23]. In this technique, a MOS transistor is used with balanced signals due to an IVB in order to cancel even-order non-linearities of the MOS transistor [23]. In order to show the advantage of this method, in this work a voltage-mode (VM) first-order all-pass filter (APF) example is presented. In the open literature several VM first-order APFs were reported [24]–[44] (and works cited therein), however, only circuits in [39]–[44] employ in total less than ten transistors. The use of low number of transistors in the circuit may results in lower silicon area in case of on-chip fabrication. This can be also seen from Tab. 1, which summarizes the advantages and disadvantages of previously reported VM low-transistor count APFs [39]–[44]

Ref.	Year	No. of ABBs	No. of transistors	No. of R/C	Technology	Supply voltages (V)	Tunability	Frequency tuning range (Hz)	Total area[c] (μm^2)
[39]	2002	–	6	1 / 1	0.35 μm CMOS	3.3	No	–	30
[40]	2010	–	3 MOS	2 / 1	TSMC 0.35 μm CMOS	±1.5	No	–	24.5
[41]	2003	1 IUGA	5 MOS[b]	0 / 1	0.35 μm BiCMOS	±1.5	Yes	500 k → 3 M	190
[42]	2010	1 IVB	2+2 MOS	2 / 1	TSMC 0.18 μm CMOS	±0.9	Yes	544.8 k → 2.9 M	39.53
[43]	2012	–	4+1 MOS	0 / 1	TSMC 0.18 μm CMOS	±0.9 and −0.37	Yes	840 k → 2.25 M	64.15
[44]	2013	1 VDIBA	6 MOS[b]	0 / 1	TSMC 0.18 μm CMOS	±0.9	Yes	1.07 M → 9.44 M	97.2
This work[a]	2013	1 IVB	2+1 MOS	2 / 1	PTM 90 nm CMOS	±0.45	Yes	103 k → 18.3 M	29.33

Tab. 1. Comparison with previously published low transistor count VM all-pass filters.
Notes:
– Not applicable
[a] Solution with m-ratio compensation shown in Fig. 4(b) is considered
[b] Ideal current source(s) assumed
[c] Sum of products of the lengths and widths of each transistors in used CMOS structure incl. VCR area

based on various relevant criteria. Recently, there is an increasing trend on the design of low-voltage circuits due to the requirement of efficient portable electronic systems with long battery lifetime [45]. In this paper and in [39], [41]–[43] proposed circuits are suitable for low-voltage operation, because only two MOSFETs are used between its supply rails. From Tab. 1 it can be also seen that only APFs in [41]–[44] are electronically tunable. From the tunability point of view, the circuit in [41] adapts the Fabre's controlling parasitic resistance technique [4] adjusting the output resistance, circuits in [42] and [43] belong to MOSFET-C filters, while the APF in [44] is based on OTA. In order to suppress the effect of non-zero output resistance of the IVB, which negatively effects the gain response of the APF, two compensation techniques are also proposed and their efficiency are compared. The functionality of the proposed APF is verified by SPICE simulations and with experimental measurements.

2. The Proposed First-Order All-Pass Filter

The MOS resistive cell in Fig. 1 can be used for cancellation of MOS transistor non-linearities and a voltage-controlled linear MOS resistor is obtained [23]. The drain current of an n-channel MOS transistor in triode operation:

$$I_D = K \left[a_1 (V_1 - V_2) + a_2 \left(V_1^2 - V_2^2 \right) \dots \right] \quad (1)$$

where V_1 and V_2 denote the drain and source voltages, respectively. Equation (1) shows how even-order terms are canceled for $V_1 = -V_2$. The $I_D \approx 2V_1/R_{mos}$, where the equivalent resistance can be calculated as:

$$R_{mos} = 1/Ka_1 = \frac{1}{\mu C_{ox} \frac{W}{L} (V_C - V_{Th})}. \quad (2)$$
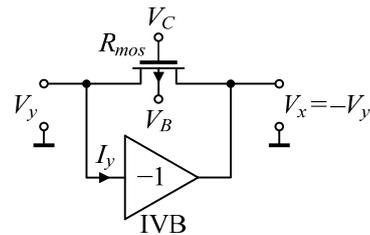
Fig. 1. The MOS resistive cell (MRC), which cancels even-order non-linearities of the MOS transistor [23].

Here μ is free electron mobility in the channel, C_{ox} is gate oxide capacitance per unit area, W and L are channel width and length of the NMOS, V_{Th} is threshold voltage of the transistor, and V_C is control voltage at the gate of the MOSFET used for tuning, respectively. In the MRC, even-order non-linearities of the MOS transistor can be canceled by the IVB that provides opposite signals at its drain and source.

The proposed VM APF circuit is given in Fig. 2. The NMOS transistors M_1 and M_2, both working in saturation region (satisfy conditions $V_{GS} > V_{Th}$ and $V_{DS} > V_{GS} - V_{Th}$), implement the IVB of the MRC. The gain of the IVB can be calculated as [46]:

$$\frac{V_x}{V_y} = -k \sqrt{\frac{(W/L)_2}{(W/L)_1}}, \quad (3)$$

and $I_y = 0$. Selecting equal values of W/L for both transistors, the gain k of the IVB will be unity.

The input/output terminal resistances of the IVB can be found as:

$$R_y \cong \infty, \quad R_x \cong \frac{1}{g_{m1}} \| r_{o2} \quad (4)$$

(a)

(b)
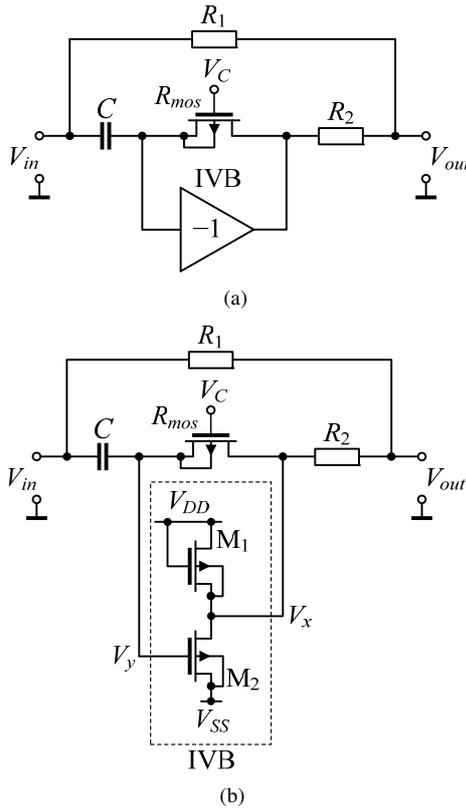
Fig. 2. (a) Proposed MOSFET-C all-pass filter, (b) its low-voltage CMOS implementation.

where g_{m1} and r_{o2} represent the transconductance and output resistance of the M_1 and M_2 transistors, respectively. From (4) it can be seen that the input terminal of IVB has high resistance (ideally infinity) while the output terminal can exhibit low resistance R_x (for ideal IVB it is zero) by selecting large transistors $M_{1,2}$.

Assuming an ideal IVB with unity-gain and with zero output resistance and considering the resistance of the MOS transistor used as VCR, which is labeled as R_{mos}, routine analysis of the proposed circuit in Fig. 2 gives the following voltage transfer function (TF):

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{-sCR_1R_{mos} + R_2(2 + sCR_{mos})}{(R_1 + R_2)(2 + sCR_{mos})}. \quad (5)$$

Here it is worth noting that it is possible to match resistors with much better precision than 0.1 % even in the IC technologies of two decades ago [47]. For the element matching condition of $R_1 = 2R_2$, the TF in (5) changes to:

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{1}{3} \cdot \frac{1 - sCR_{mos}/2}{1 + sCR_{mos}/2}. \quad (6)$$

Equation (6) represents a first-order all-pass TF. Although (6) is independent from the absolute values of R_1 and R_2, these resistance values should be chosen sufficiently high such that the output of the IVB is not loaded heavily. Fortunately, as it was mentioned, high-value resistors with good matching can be obtained in IC technology [47]. Their large tolerances in absolute values will not be a problem since (6) is independent from both R_1 and R_2.

The phase response of the TF in (6) is calculated:

$$\varphi(\omega) = -2\tan^{-1}(\omega CR_{mos}/2), \quad (7)$$

and pole (ω_p) and zero (ω_z) frequencies can be found as:

$$\omega_p = \omega_z = 2/CR_{mos}, \quad (8)$$

which clearly indicates that the ω_p can be easily tuned by adjusting the value of R_{mos}.

Considering non-ideal IVB and assuming equal W/L ratio for both transistors, (3) converts to $V_x = -\beta(s)V_y$, where $\beta(s)$ is frequency-dependent parameter of the IVB, which limits the high frequency operation of the circuit. Using a single-pole model [48] it can be defined as follows:

$$\beta(s) = \frac{\beta_o}{1 + s\tau_\beta} \quad (9)$$

where $\beta_o = 1 - \varepsilon_{\beta_v}$ is DC voltage gain of IVB and ideally it is equal to unity. Considering non-ideal IVB and assuming element matching condition of $R_1 = 2R_2$, voltage gain (6) changes to:

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{1}{3} \cdot \frac{\left(\frac{2}{CR_{mos} - \tau_\beta} - s\right)\left(\frac{CR_{mos}\tau_\beta}{CR_{mos} - \tau_\beta} + s\right)}{\left(\frac{2}{CR_{mos} + \tau_\beta} + s\right)\left(\frac{CR_{mos}\tau_\beta}{CR_{mos} + \tau_\beta} + s\right)}. \quad (10)$$

Equation (10) shows that extra pole and zero appears due to single-pole model additional to filter pole. If the frequency of these additional pole and zero are sufficiently higher than the pole of the presented all-pass filter than their effect on the frequency can be ignored.

3. Loading Effect Analysis

In this section the effect of the load at output terminal of the filter shown in Fig. 2 is investigated. Assuming an IVB with unity-gain and with non-zero output resistance R_x, which is for better understanding labeled as R_O, considering the resistance used as VCR as R_{mos}, and load R_L at output terminal of the filter, straightforward analysis gives the voltage TF (11).

Assuming $R_L \gg R_O$ and $R_1 = 2R_2 = R$, TF in (11) turns to:

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{1}{\left(\frac{R}{R_L} + 3\right)} \cdot \frac{1 - sCR_{mos}/2}{1 + sCR_{mos}/2}. \quad (12)$$

From (12) it can be observed that the load has no effect on pole (ω_p) or zero (ω_z) frequencies, but it effects the DC voltage gain of the filter. Here it is worth noting that this feature is an interesting advantage of this circuit against filter available in [44] in which the load effects the pole frequency of the circuit and it may produce a mismatch to zero frequency. To illustrate the effect of the load on the gain of the filter, it was further investigated. The calculation has been done for different values of R_L while keeping the resistor values identical with listed in the Tab. 2 (without compensation column) and results are plot in Fig. 3.

$$T(s) = \frac{V_{out}}{V_{in}} = -\frac{sC[R_1(R_{mos} - R_O) - R_2(R_{mos} + R_O) - R_{mos}R_O] - 2R_2 - R_O}{\frac{R_1}{R_L}\{sC[R_2(R_{mos}+R_O)+R_{mos}R_O]+2R_2+R_O\} + sC[(R_1+R_2)(R_{mos}+R_O)+R_{mos}R_O]+2R_1+2R_2+R_O}.$$

(11)
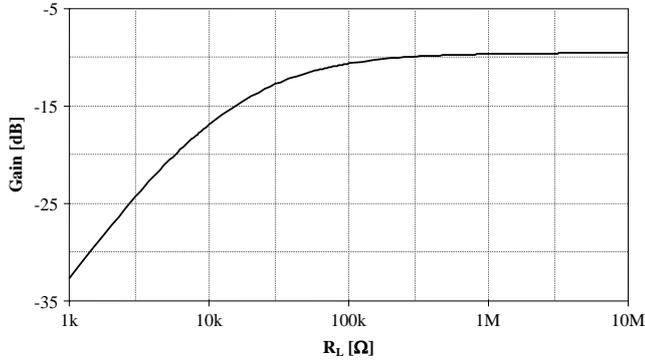
Fig. 3. Voltage gain of the APF for different values of load.

4. Compensation of the Effect of the Output Impedance

The presented APF adapts MOSFET-C technique and low-voltage technology. However, this simple MRC has an important non-ideality affecting the characteristics of the circuits, which is the non-zero output resistance of the IVB that is shown in Fig. 4. Two techniques are proposed to suppress the effect of this parasitic output resistance: (i) by changing the gain of the IVB and (ii) via resistor matching ratios.

4.1 Compensation with the Gain of the Inverting Voltage Buffer

Firstly, the change of the gain parameter of the IVB is used to compensate the unwanted effects of the parasitic output resistance. Denoting the parasitic output resistance of the IVB in Fig. 4 again as R_O and with element matching condition $R_1 = 2R_2$, the TF can be given as:

$$T(s) = \frac{V_{out}}{V_{in}} = \qquad (13)$$

$$\frac{R_O(1+sCR_{mos})+R_2[1+k+sCR_{mos}(1-2k)+3sCR_O]}{R_O(1+sCR_{mos})+3R_2[1+k+sC(R_{mos}+R_O)]}$$

where k is the gain of the IVB. For a non-zero R_O, a k value can be calculated to achieve a flat gain response of the APF as it is given in (14).

The graphical representation of k is given for various R_{mos} and R_O values for $R_2 = 1$ kΩ in Fig. 5(a) and $R_2 = 20$ kΩ in Fig. 5(b), respectively. Figure 5 shows that choosing a k value appropriately can compensate for the unwanted effects of the R_O.

(a)

(b)
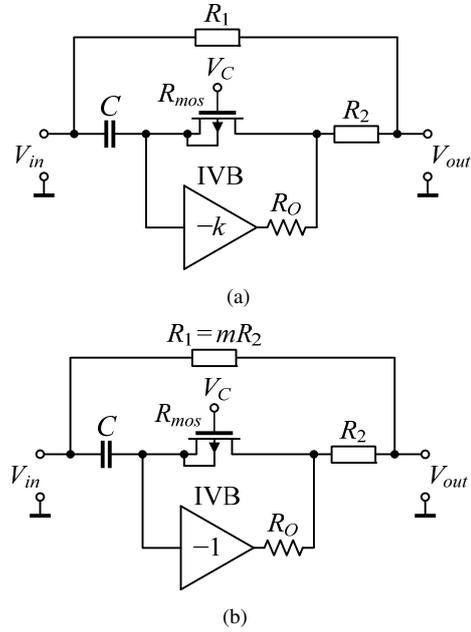
Fig. 4. The compensation for the unwanted effect of the R_O: (a) by proper gain value k, (b) with a proper resistor matching ratio m.

(a)

(b)
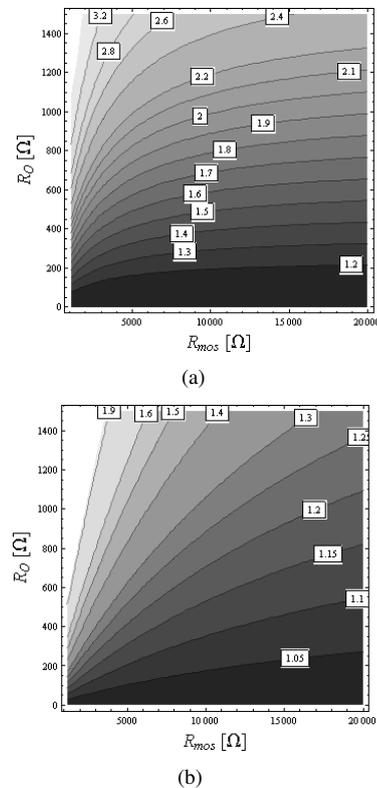
Fig. 5. Optimum gain value k (constant k-value curves) for the circuit in Fig. 4(a) (to preserve the all-pass response) versus R_{mos} and R_O: (a) for $R_2 = 1$ kΩ, (b) for $R_2 = 20$ kΩ.

$$k = \frac{R_O}{R_{mos}} + \frac{R_O}{6R_2} + \frac{\sqrt{13R_O{}^2 R_{mos}{}^2 + 48R_O R_2 R_{mos}(R_O + R_{mos}) + 36R_2{}^2 (R_O + R_{mos})^2}}{6R_2 R_{mos}}. \tag{14}$$

(a)

(b)
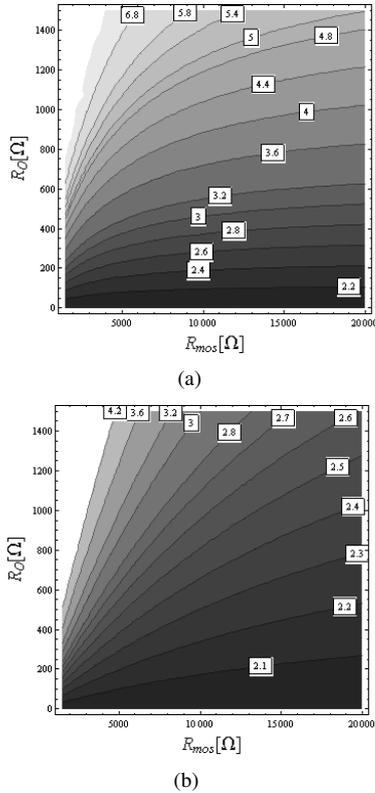
Fig. 6. Optimum resistor matching value m (constant m-value curves) for the circuit in Fig. 4(b) (to preserve all-pass response) versus R_{mos} and R_O: (a) for $R_2 = 1$ kΩ, (b) for $R_2 = 20$ kΩ.

4.2 Compensation with the Resistor Matching Ratio

Secondly, a resistor matching ratio is used to compensate the undesired effects of the non-zero R_O to achieve a flat gain all-pass response. The new transfer function of the circuit in Fig. 4(b) for the element matching condition of $R_1 = mR_2$ and with consideration R_O can be calculated as:

$$T(s) = \frac{V_{out}}{V_{in}} = \tag{15}$$

$$\frac{R_O + R_2 [2 + sCR_O (1 + m)] + sCR_{mos}(R_2 - mR_2 + R_O)}{R_O + R_2 (2 + sCR_O)(1 + m) + sCR_{mos}(R_2 + mR_2 + R_O)}.$$

The resistor matching ratio m that results an all-pass response is given in (16).

For various R_{mos} and R_O values the graphical representation of m is given for $R_2 = 1$ kΩ and $R_2 = 20$ kΩ in Figs. 6(a) and (b), respectively. Figure 6 illustrates how to select an m value for a proper design to compensate the effect of R_O.

As a summary, both methods can be used to compensate the unwanted effect of the output resistance of the IVB.

Therefore, the efficiency of both techniques is compared by simulations.

5. Limitations of the Input Signal and the Control Voltage

To employ the MOSFET in MRC as a linear resistor, the terminal and control voltages of the MOSFET must keep it in triode region. Thus, the terminal voltages V_y and V_x of the MRC shown in Fig. 1, must satisfy the following conditions:

$$V_x = -V_y, \tag{17}$$
$$|V_y| \leq V_C - V_{Th}, \tag{18}$$
$$|V_y| \leq |V_B|. \tag{19}$$

Here $V_C \geq V_{Th}$ and $V_B \leq 0$. Moreover, V_{Th} is given by:

$$V_{Th} = V_{Th0} + \gamma' \cdot \left(\sqrt{2\Phi_f + V_B} - \sqrt{2\Phi_f} \right) \tag{20}$$

where V_{Th0} is the threshold voltage for $V_B = 0$, Φ_f is a physical parameter with $(2\Phi_f)$ typically 0.6 V, γ' is a fabrication-process parameter [47].

Since the conditions in (17)–(19) impose a limitation on the terminal voltages of the MRC, it is clear that they also impose a limitation on the amplitude of the filters input signal V_{in}. The relation between the magnitudes of V_y (the voltage at the inverter input terminal) and V_{in} in Fig. 2(a) is $|V_y(j\omega)| = R_{mos}C\omega / \sqrt{4 + R_{mos}{}^2 C^2 \omega^2}|V_{in}(j\omega)|$. Furthermore from the conditions in (17)–(19) it is obvious that $|V_y(j\omega)| \leq V_m$, where $V_m = \min\{|V_C - V_{Th}|, |V_B|\}$. Therefore one can obtain the limitation for V_{in} as:

$$|V_{in}| \leq V_m \sqrt{\frac{4 + R_{mos}{}^2 C^2 \omega^2}{R_{mos}{}^2 C^2 \omega^2}}. \tag{21}$$

Equation (21) shows that the input signal limitation is $|V_{in}| \leq V_m$ in Fig. 2(a) and it occurs at the sufficiently high frequency region. On the other hand much wider input dynamic signal is possible at low frequencies.

6. Simulation and Experimental Results

To verify the theoretical analyses, the proposed VM APF circuit is simulated using the SPICE simulation program with DC power supply voltages equal to $+V_{DD} = -V_{SS} = 0.45$ V. In the simulations, all n-channel MOS transistors are modeled by the Predictive Technology Model (PTM) 90 nm level-7 CMOS process BSIM3v3 parameters developed by the Nanoscale Integration and Modeling (NIMO) Group at Arizona State University ($V_{Th} = 0.2607$ V,

$$m = \frac{3R_2R_O + R_O^2 + (R_2 + R_O)R_{mos} + \sqrt{R_O^2(R_2 + R_O)^2 + R_{mos}[6R_2^2R_O - 2R_O^3 + (R_2 + R_O)(9R_2 + 5R_O)R_{mos}]}}{2R_2(R_{mos} - R_O)}. \quad (16)$$
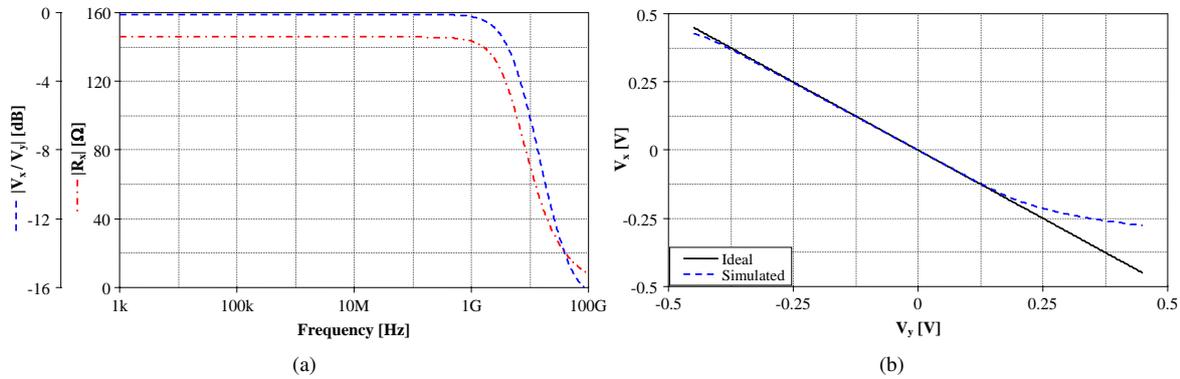
Fig. 7. (a) AC (voltage gain & output resistance vs. frequency) and (b) DC analyses of IVB.
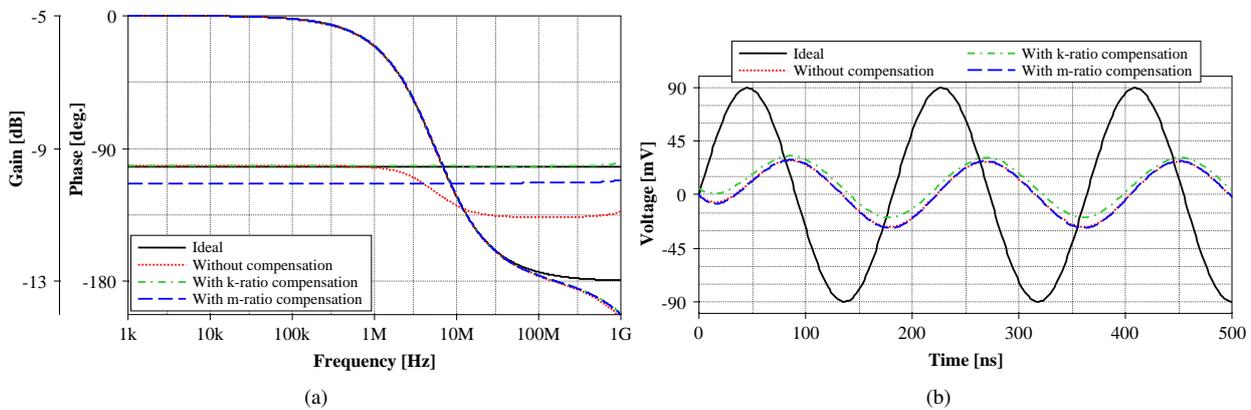
Fig. 8. Simulated (a) gain and phase responses, (b) time-domain responses of the proposed all-pass filter at 5.5 MHz.

Parameter	APF without compensation	APF with k-ratio compensation	APF with m-ratio compensation
C [pF]	5.8	5.8	5.8
R_1, R_2 [kΩ]	40, 20	40, 20	43.7, 20
W/L of VCR R_{mos} [μm/μm]	0.63/0.27	0.63/0.27	0.63/0.27
V_C of VCR R_{mos} [V]	0.51	0.51	0.51
R_{mos} [kΩ]	10	10	10
W/L of M$_1$ and M$_2$ [μm/μm]	both 54/0.27	54/0.27 and 71.82/0.27	both 54/0.27
Total power dissipation [μW]	364	418	364

Tab. 2. Design parameters of the VM all-pass filters in Figs. 2(b), 4(a), and (b) for $f_p = 5.5$ MHz.

$\mu = 0.017999999$ cm^2/(V·s), $T_{ox} = 2.5$ nm) [49]. In the design, the bulks of all NMOS transistors are connected to their relevant sources to prevent body effect.

First of all, the performance of the IVB was tested by AC and DC analyses. The aspect ratios of both M$_1$ and M$_2$ transistors were chosen as $W/L = 54$ μm/0.27 μm. Note that the W/L ratio of the transistors should be selected sufficiently high to decrease the loading effect. The AC simulation results for both voltage gain and output resistance of the

IVB are shown in Fig. 7(a). The obtained gain of the IVB voltage transfer is equal to 0.988 and its f_{-3dB} frequency is found to be 5.68 GHz while its parasitic output resistance, whose unwanted effect compensation is the aim of this paper, is equal to $R_O = 145.74$ Ω. The DC voltage characteristic of V_x against V_y is shown in Fig. 7(b). The maximum values of terminal voltages without producing significant distortion are approximately computed as -0.45 V to $+0.23$ V.

In order to compare both compensation techniques
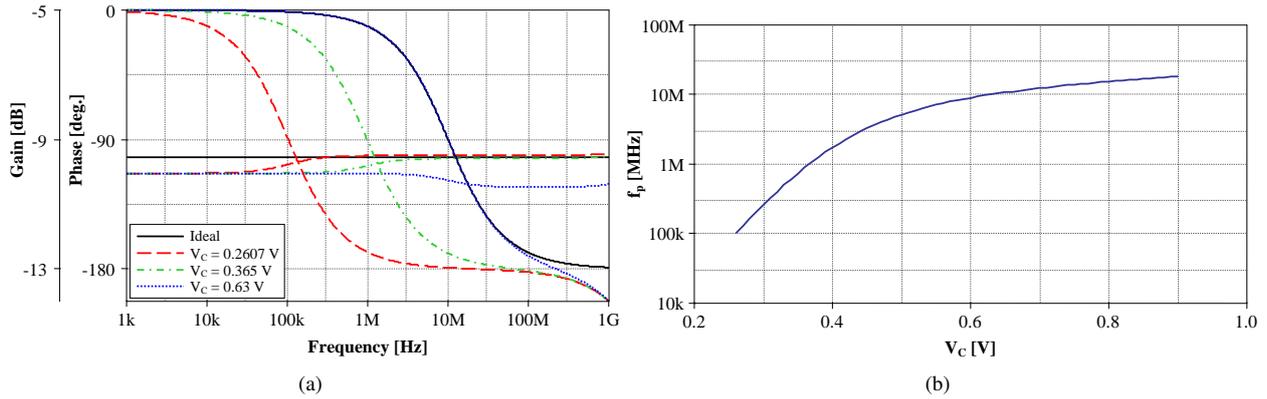
Fig. 9. Demonstration of electronical tunability of pole frequency with control voltage V_C of the all-pass filter with m-ratio compensation shown in Fig. 4(b): (a) gain and phase responses, (b) control voltage V_C vs. pole frequency.

and their efficiency on the proposed VM APF, circuits in Figs. 2(b), 4(a) and (b) have been further analyzed in SPICE software. All three variants have been proposed for $f_p \cong 5.5$ MHz, which is a typical operating frequency of wireless local area network (WLAN; IEEE 802.11b) receivers [50], and design parameters are given in Tab. 2. Figure 8(a) shows the ideal and simulated gain and phase responses of the uncompensated and compensated filters. From the results it can be observed that the deviation in gain is compensated using both techniques successfully. To compare the time-domain performance of all three filter variants, transient analysis is performed to evaluate the voltage swing capability and phase errors of the circuits as it is demonstrated in Fig. 8(b). In simulations, a sine-wave input of 90 mV amplitude and frequency of 5.5 MHz was applied to the filters while keeping settings as listed in Tab. 2. In case of circuit with k-ratio compensation the offset is caused by non-equal W/L ratio of $M_{1,2}$ transistors and it can be suppressed via level shifter also used in [41]. It is worth mentioning that the total power dissipation (TPD) of the circuit with m-ratio compensation is equal to APF without compensation and found to be 364 μW. On the other hand, the TPD of the filter with k-ratio compensation is 418 μW due to larger channel width of M_2, which also increases its total area in case of on-chip fabrication. Hence, from the obtained simulation results we can conclude that the technique with m-ratio compensation is more effective. Therefore, in further analyses the behavior of the VM APF shown in Fig. 4(b) will be investigated. To demonstrate the electronic tunability of proposed filter with m-ratio compensation shown in Fig. 4(b), its ideal and simulated gain and phase responses are depicted in Fig. 9(a). The tunability performance is also illustrated in Fig. 9(b), where the control voltage V_C of VCR was tuned from V_{Th} to supply rail of IVB and the pole frequency changes from 103 kHz to 18.3 MHz successfully. The total harmonic distortion (THD) variation with respect to amplitude of the applied sinusoidal input voltage at 5.5 MHz is shown in Fig. 10. An input with the amplitude of 90 mV yields THD value of 2.23 %. Using the INOISE and ONOISE statements input and output noise variations

against frequency have also been simulated and results are tabulated in Tab. 3.

Moreover, the performance of the proposed circuit shown in Fig. 4(b) have also been tested experimentally. In measurements, for implementation of IVB and VCR, the readily available array transistors CD4007UB [51] by Texas Instruments with ± 3 V DC supply voltages have been used. In experiments the values of the passive components were selected as $C = 10$ nF, $R_1 = 220$ kΩ, and $R_2 = 100$ kΩ. The measured gain and phase responses are depicted in Fig. 11. The phase responses are depicted for three different control voltages $V_C = 1.5$ V and $V_C = 1.8$ V and the gain response is depicted for $V_C = 1.8$ V.

Frequency (Hz)	APF without compensation		APF with m-ratio compensation	
	Input noise (nV/$\sqrt{\text{Hz}}$)	Output noise (nV/$\sqrt{\text{Hz}}$)	Input noise (nV/$\sqrt{\text{Hz}}$)	Output noise (nV/$\sqrt{\text{Hz}}$)
1×10^3	45.772	15.295	49.190	15.483
1×10^4	45.772	15.295	49.190	15.483
1×10^5	45.774	15.294	49.190	15.483
1×10^6	45.995	15.281	49.156	15.473
1×10^7	51.479	14.997	48.344	15.221
1×10^8	53.346	14.923	48.075	15.139
1×10^9	52.302	14.920	47.555	15.136

Tab. 3. Input and output noises of the all-pass filters in Figs. 2(b) and 4(b) against frequency.
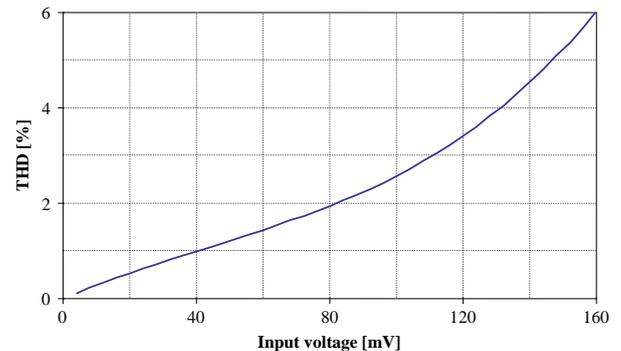
Fig. 10. THD variation of the APF with m-ratio compensation shown in Fig. 4(b) vs. applied input voltage at 5.5 MHz.
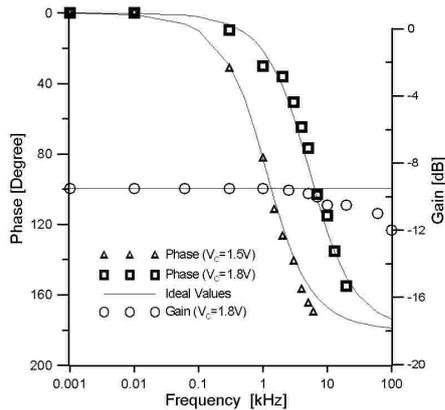
Fig. 11. Measured gain and phase characteristics of the proposed all-pass filter and illustrating the electronical tunability of pole frequency with control voltage V_C.

From the simulation results and experimental measurements it can be seen that the final solution is in good agreement with the theory.

7. Conclusions

In this paper a voltage-mode first-order all-pass filter circuit employing only three NMOS transistors, two resistors, and a single capacitor is proposed by MOSFET-C technique. Simplicity, tunability, and low-voltage operation features make the circuit attractive for contemporary technologies. In order to suppress the effect of non-zero output resistance of the IVB, two compensation techniques are investigated. Based on the simulation results we can conclude that the technique with resistor matching ratio compensation is more effective and it gives good compromise in terms of filter voltage gain compensation, DC voltage offset, TPD, and transistors total area. However, as simulation results showed that, if the filter is tuned then the optimum parameter setting cannot be respected in the full scale.

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About Authors ...

Bilgin METIN received the B.Sc. degree in Electronics and Communication Engineering from Istanbul Technical University, Istanbul, Turkey in 1996 and the M.Sc. and Ph.D. degrees in Electrical and Electronics Engineering from Bogazici University, Istanbul, Turkey in 2001 and 2007 respectively. He is currently an Assistant Professor in the Management Information Systems Department of Bogazici University. His research interests include continuous time filters, analog signal processing applications, current-mode circuits, information systems. He was given the best student paper award of ELECO'2002 conference in Turkey. He has over 60 publications in scientific journals or conference proceedings.

Norbert HERENCSAR was born in Slovak Republic in 1982. He received the M.Sc. and Ph.D. degrees in Electronics & Communication and Teleinformatics from Brno University of Technology, Czech Republic, in 2006 and 2010, respectively. Currently, he is an Assistant Professor at the Department of Telecommunications and employee at the Centre of Sensor, Information and Communication Systems (SIX) of Faculty of Electrical Engineering and Communication, Brno University of Technology, Brno, Czech Republic. During September 2009-February 2010 and February 2013-May 2013 he was an Erasmus Exchange Student and Visiting Researcher, respectively, with the Department of Electrical and Electronic Engineering, Bogazici University, Istanbul, Turkey. His research interests include analog filters, current-, voltage- and mixed-mode circuits, electronic circuit & system design, new active elements and their circuit applications, and oscillators. He is an author or co-author of 36 research articles published in SCI-E international journals, 23 articles published in other journals, and 66 papers published in proceedings of international conferences. In 2011 and 2012, he received Rector Award in the University competition "Top 10 Excelence VUT" for the 9th and 8th most productive scientist at the Brno University of Technology, category "Publications", respectively. His paper "Novel resistorless dual-output VM all-pass filter employing VDIBA", presented and published at the 7th International Conference on Electrical Electronics Engineering - ELECO 2011, Bursa, Turkey, received "The best paper award in memory of Prof. Dr. Mustafa Bayram".

Since 2008, Dr. Herencsar serves in the Organizing and Technical Committee of the International Conference on Telecommunications and Signal Processing (TSP). Since 2010 he is also Co-Chair of TSP. In 2013 he serves in the Technical Program Committee of the 8th International Conference on Electrical and Electronics Engineering (ELECO 2013). Since 2012, he is Co-Editor of the International Journal of Advances in Telecommunications, Electrotechnics, Signals and Systems. In 2011, he was Guest Co-Editor of TSP 2010 Special Issue on Telecommunications, published in the Telecommunication Systems journal of Springer. In 2011–2013, he was Guest Co-Editor of TSP 2010, TSP 2011, and TSP 2012 Special Issues on Signal Processing, published in the Radioengineering journal. He is Senior Member of the IACSIT and Member of the IEEE, IAENG, and ACEEE. He is also Committee Member of the IACSIT Electronics and Electrical Society (EES).

Oguzhan CICEKOGLU received the B.Sc. and M.Sc. degrees from Bogazici University and the PhD. degree from Istanbul Technical University all in Electrical and Electronics Engineering in 1985, 1988 and 1996 respectively. He served as lecturer at the School of Advanced Vocational Studies Electronics Prog. of Bogazici University where he held various administrative positions between 1993 and 1999. He has also given lectures at the Turkish Air Force Academy. He was with the Biomedical Engineering Institute of the Bogazici University between 1999 and 2001. Then he joined the Electrical and Electronics Engineering Department of the same university where he became a professor. Between 2007 and 2010 he served as the Dean of Engineering at Corlu Engineering Faculty of Namik Kemal University, Turkey. Since May 2013 he is appointed as the Dean of Engineering Faculty of Turkish-German University (TAÜ) in Istanbul.

Prof. Cicekoglu served in organizing and technical committees of many national and international conferences. He was the guest co-editor of two previous Special Issues of the Analog Integrated Circuits and Signal Processing Journal. One of the publications he co-authored in IEEE Transactions on Circuits and Sytems II—Analog and Digital Signal Processing is among the top cited papers listed in IEEE Circuits and Systems Society web page. He received the Research Excellence Award of Bogazici University Foundation in 2004. He served as the co-chair of Amplifiers and Comparators track in 50th IEEE Midwest-Newcas Joint Conference which is held in Montreal-Canada as a track chair in the 52th IEEE Midwest Symposium held in Cancun-Mexico. His current research interests include analog circuits, active filters, analog signal processing applications and current-mode circuits. He is the author or co-author of about 150 papers published in scientific journals or conference proceedings and conducts review in numerous journals including Analog Integrated Circuits and Signal Processing, IEEE CAS—I, IEEE CAS—II, International Journal of Electronics, International Journal of Circuit Theory and Applications, IEE Proceedings Pt.G, ETRI Journal and several others.

Prof. Cicekoglu is a member of the IEEE and is currently Associate Editor of International Journal of Electronics.