# Software Defined DCF77 Receiver

*Filip ZÁPLATA, Miroslav KASAL*

Dept. of Radio Electronics, Brno University of Technology, Technická 10, 616 00 Brno, Czech Republic

xzapla00@stud.feec.vutbr.cz, kasal@feec.vutbr.cz

**Abstract.** *This paper shows the solution of time stamp software defined receiver integration into low cost commercial devices. The receiver is based on a general purpose processor and its analog to digital converter. The amplified signal from a narrow-band antenna is connected to the converter and no complicated filtration has to be used. All signal processing is digitally provided by the processor. During signal reception, the processor stays available for its main tasks and signal processing consumes only a small part of its computational power.*

## Keywords

DCF77, time stamp transmission, software defined radio, digital receiver, Goertzel algorithm.

## 1 Introduction

Usual time stamp receivers available on the market use an analog amplitude modulation (AM) receiver concept, such as the basic single band integrated receivers [1] and [2], the dual band AM receiver [3], or a more complex solution [4]. This concept uses a loopstick antenna (ferrite antenna) connected to a preamplifier (LNA). The signal is then filtered by a Quartz filter and then demodulated. The output of the demodulator is a base-band modulation signal which is easily convertible to digital representation by a comparator. The information carried by this digital signal has to be decoded by a processor. The aim of the following solution is to move the filter and the demodulator from analog to digital domain with a slight increase of computational demands. Nowadays, processors, e.g. LPC2103 [5], commonly have analog to digital converters included as its peripherals which are fast enough. Then, the only necessary external components which remain are the antenna and the LNA.

## 2 DCF77 Standard

The DCF77 is the standard of the time stamp transmitter which is located near Frankfurt in Germany. Reception of this signal brings the ability to synchronize the receiver clock to precise time of an atomic clock. It can be used not only for synchronization of clocks to show the actual time and date, but even for synchronizing equipment for precise time measurement. The information is carried by an amplitude modulated carrier of frequency 77.5 kHz and signal bandwidth 2.4 kHz [6]. Due to such low frequency, it is possible to receive the signal many hundreds, even thousands of kilometers from the transmitter. The DCF77 is developed for Europe, but there are many standards for other regions like American WWVB or Japanese JJY, and the differences are only the carrier frequency or amplitude shift keying scheme.

Modulation is in fact an amplitude shift keying, where the carrier amplitude is reduced to 25 % for the duration of 100 ms for binary 0 and 200 ms for binary 1. The beginning of each reduction marks the precise beginning of the second. Then, one bit is carried during every second and the whole data word is carried during every minute. During the last second of a minute, there is no bit carried and amplitude is not reduced. It is the information for the receiver about minute synchronization and the mark of a new data word beginning. The modulation signal is shown in Fig. 1. This is an example of the minute sequence.

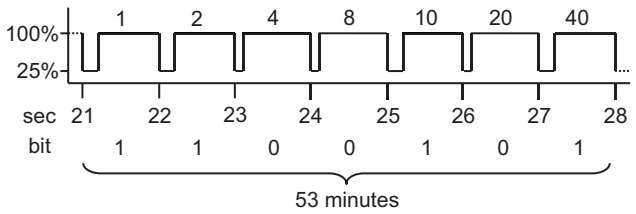


**Fig. 1.** Modulation signal example.

The carried data word is 59 bits long and contains the information of minute, hour, day, weekday, month, year and time zone, which is valid right after the minute synchronization symbol is received. The code scheme is shown in Fig. 2. More details can be found in [6], [7].

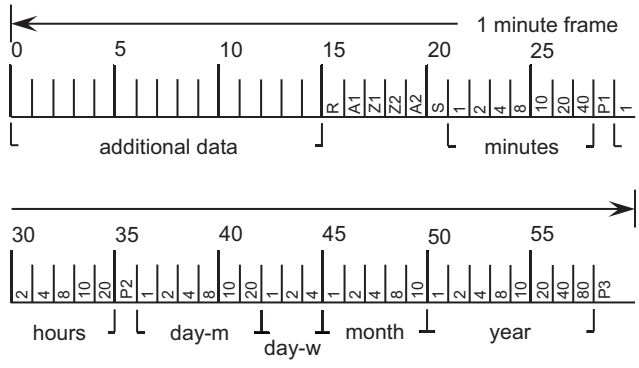


**Fig. 2.** DCF77 data description.

# 3 Hardware Overview

It is expected, that the speed of a sample and hold circuit of an analog to digital converter (ADC) in a selected embedded processor is sufficient to handle the frequencies above the carrier frequency. The converted signal is narrowband, therefore it is wise to use bandpass sampling. This technique allows maintaining the accuracy of converting high frequencies and especially reducing the number of output samples. Many converters allow to set the reference voltage by external circuits, but the radio frequency (RF) signal still needs to be amplified by over 40 dB. However, due to low frequency, such gain can be achieved by many types of circuits, even using an operational amplifier is suitable. Before digitization of an analog signal, filtration should be applied to prevent aliasing. A properly designed loopstick antenna should provide a sufficient signal to noise ratio in a useful band. If more precise filtration is necessary, an additional filter can be connected to the amplifier. Block schematic of hardware realization of the receiver is shown in Fig. 3.

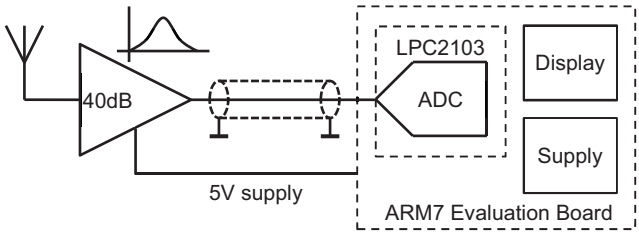


**Fig. 3.** Block schematic of testing receiver.

## 3.1 Antenna

The loopstick antenna is wired on a thick ferrite rod about 5 cm long. The ferrite material has high permeability to increase induced RF voltage. By adding a capacitor, a resonant circuit is created. Several methods are used to obtain high selectivity as similarly shows (1) [8] - signal to noise ratio calculation

$$SNR = 66.3NAE\mu\sqrt{\frac{Qf}{LB}} \qquad (1)$$

where field strength $E$, rod permeability $\mu$, receiver bandwidth $B$, operating frequency $f$ and rod cross-section $A$ are fixed. Winding should be uniformly spread along the whole length of the rod to obtain lower inductance $L$, higher number of turns $N$ and sufficient quality factor $Q$. The highest $Q$ of a short coil is in the center of the rod. Mainly at higher frequencies, $Q$ can be also increased by the use of Litz wire, which consists of strands woven into bundles. Efficiency of the antenna depends on the rod cross-section and permeability. The higher the core permeability and cross-section, the higher induced voltage in the same coil, therefore more rods tapped together then can be used as an improvement. Thickness of the rod also affects the radiation pattern of the antenna, the thicker the rod, the wider the radiation beam. Loop antennas are often electrically shielded, it helps to correct the radiation pattern and eliminate the electric noise. Load still has a major impact on $Q$ of the antenna resonant circuit, and then a high impedance amplifier stage should be used. Usual amplifier impedance $R_{load}$ can vary around 100 ÷ 500 kΩ at 77.5 kHz, the capacitance should then be about 0.5 ÷ 5 nF. This is practical experience, where compromise was picked between a high number of turns of the coil in equation (1) and high capacitance $C$ in equation (2). The core should be movable on the ferrite rod to be tuned precisely to the resonance.

$$Q = R_{load}\sqrt{\frac{C}{L}}. \qquad (2)$$

## 3.2 Amplifier

The operational amplifier (OA) MCP622 is used as a low noise amplifier. This OA from Microchip is supposed to drive analog to digital converters. Rail-to-rail output and supply range from 2.5 V to 5.5 V allows using it in single supply digital systems. The unity gain bandwidth of 20 MHz is sufficient to achieve the 40 dB gain at one stage. Both OAs are used to achieve higher overall gain. The second stage can be used for gain control in the automatic gain control loop. An additional LC filter is placed between the stages. When using an additional resonant circuit, shielding is indispensable for suppression of positive feedback. The test circuit is shown in Fig. 4.

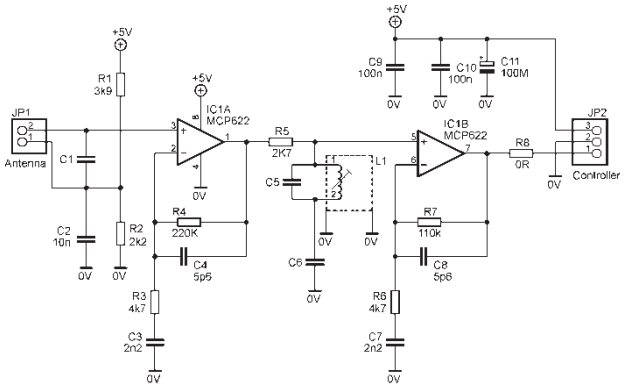


**Fig. 4.** Schematic of amplifier prototype.

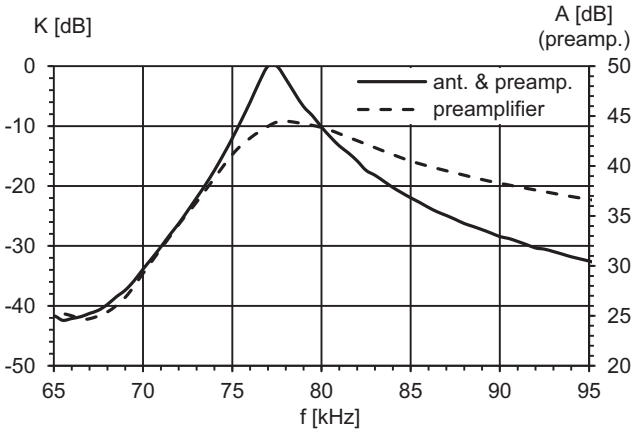


**Fig. 5.** Measured frequency response of the prototype.

The measured characteristics of the sample circuit are shown in Fig. 5. The solid curve is a normalized frequency

characteristic of a preamplifier with antenna. The dashed curve shows the characteristic of a stand-alone preamplifier. Suppression of near aliasing components is better than 25 dB at high frequencies and at low frequencies even more than 40 dB.

### 3.3 AD Conversion

Timing of the analog to digital converter is a more critical issue when providing bandpass sampling. The desired band should be placed to the center of the sampled band. The sampled band should be wider than the DCF77 signal, i.e. > 2.4 kHz. If the converter suffers from nonlinearities, another position may be preferred. Peripheral converter on LPC2103 processor is used. Timing for the converter is derived from the main clock using a Quartz oscillator and a phase locked loop. Computation of the peripheral frequency *PBCLK* is shown in (3), where *MSEL* is the register of clock phase locked loop inside the processor and *APBDIV* is the peripheral clock divider.

$$PBCLK = \frac{MSEL}{APBDIV} f_{osc} \tag{3}$$

The chosen frequency plan is shown in Fig. 6, the ADC uses the 7th Nyquist zone. By sampling at 24 kHz, the signal of frequency 77.5 kHz is shifted to a frequency of 5.5 kHz. The bandwidth is wider than 10 kHz. To reach a 24 kHz sampling frequency, the converter prescaler is set to 64, using (4). *CLKS* means the number of clock cycles for finishing the conversion of the desired bit depth; 9-bit accuracy is chosen in this case.

$$ADCDIV = \frac{PBCLK}{f_S \cdot CLKS} \tag{4}$$

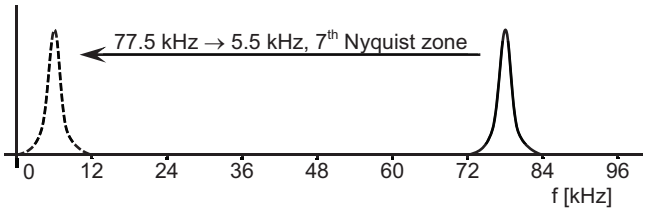


**Fig. 6.** Bandpass sampling frequency plan.

This setting is just an example, the frequency plan may be different for another SNR and also may be adaptive to the best performance. It is also wise to consider the relationship between the sampling frequency and the carrier frequency for the subsequent digital signal processing algorithms. The setting is summarized in Tab. 1.

| Parameter | Value |
|---|---|
| MSEL | 5 |
| APBCLK | 4 |
| fosc | 12288000 Hz |
| PBCLK | 15360000 Hz |
| CLKS | 9 |
| fS | 24000 Hz |
| ADCDIV | 64 |

**Tab. 1.** LPC2103 ADC setting.

## 4 Software Overview

The software part of the realization up to the decoded signal is shown in Fig. 7. First, the signal has to be filtered to select the desired narrow band. Because of many advantages, the Goertzel algorithm was chosen [9]. Then the signal can be demodulated, but in almost all cases it is better to prepend an averaging to reduce the dispersion. In addition, it can help to prevent overflowing. The baseband signal is demodulated by correlation with a step function. If a falling/rising edge comes to the correlator, a positive/negative pulse will show up on the output. These pulses are separated and detected in a peak detector. The decision level is computed right from the correlated signal by long term averaging. Peaks and their time position are the basis for the synchronization of seconds and for bit decoding.

### 4.1 Goertzel Algorithm

The Goertzel algorithm is based on the discrete Fourier transform. The algorithm computes the value only at a selected spectral position (bin) of the discrete Fourier transform, and is usually used as a tone detector in DTMF (dual tone multi-frequency) systems. The computation is based on convolution and is very similar to a recursive filter with the difference that the output value is valid only after *N* cycles, i.e. the additional feature of the Goertzel algorithm is *N*-time decimation. The signal diagram of the complex output algorithm is shown in Fig. 8 and iterative

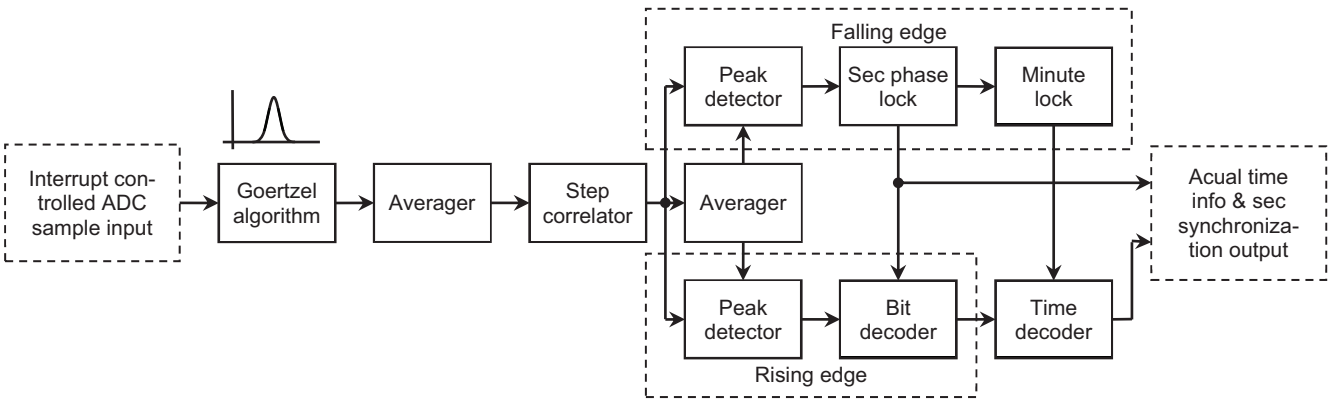


**Fig. 7.** Block schematic of software realization.

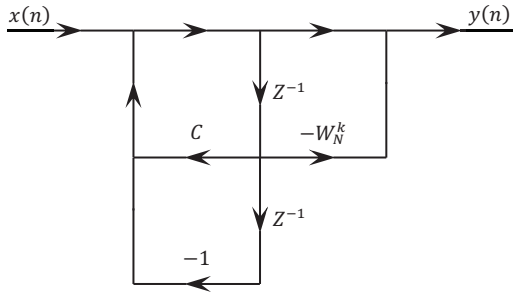


**Fig. 8.** Signal diagram of Goertzel algorithm.

computation is shown in (6). Frequency characteristics depend on the filter length $N$, and are derived from the discrete Fourier transform spectrum. Complex output values are not required in this case, therefore the power spectrum is computed and no complex twiddle factor $W_N^k$ is needed. The filter needs just one coefficient which determines the normalized frequency selection. The coefficient is computed by (5), where $k$ is bin number, $f$ is desired frequency and $f_S$ is sampling frequency. The coefficient is also used in power computation (7). In both (6) and (7), samples are indexed by $n$ and $r$ respectively.

$$C = 2\cos\left(2\pi\frac{k}{N}\right) = 2\cos\left(2\pi\frac{f}{f_S}\right), \tag{5}$$

$$D(n) = x(n) + CD(n-1) - D(n-2), \tag{6}$$

$$|y_k(r)| = D^2(rN) + D^2(rN-1) - CD(rN)D(rN-1) \tag{7}$$

Selectivity is determined by the length of filter $N$, in other words, the more samples the filter processes, the narrower the frequency response. After $N$ input samples, the output power is computed (7), filter registers are cleared and then it is prepared to process the new set of $N$ samples. These features bring advantages in releasing processor performance and easy tuning when using adaptive demodulator.

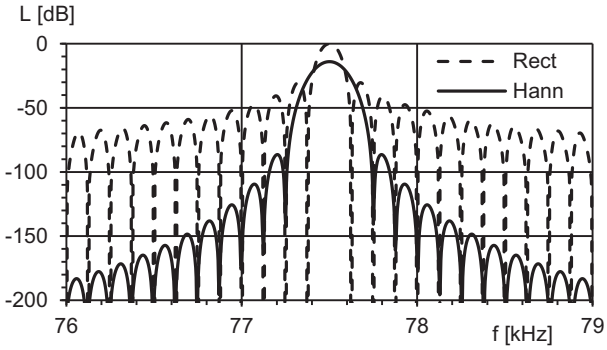


**Fig. 9.** Windowing influence on the frequency characteristic.

As well as for Fourier transform, the input set of the samples should be window-scaled to prevent spectral leakage, but pass-band is then wider as shown in Fig. 9. Useful filter lengths for a rectangular window are from 96 to 384 samples, a shorter filter would have insufficient selectivity and longer would decimate so much that it would excessively decrease the time-resolution of the filter. Overlapping would help to suppress these effects at the expense of stronger demands on the processing power and operational memory.

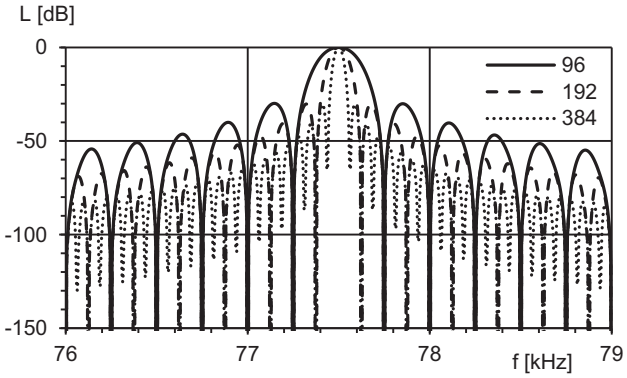


**Fig. 10.** Frequency responses of filters of different lengths.

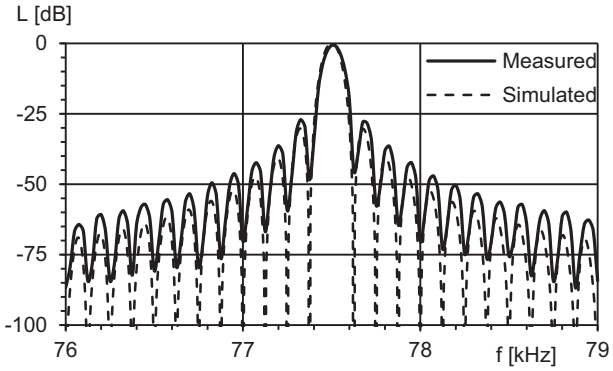


**Fig. 11.** Measured characteristic of implemented filter.

Fig. 10 shows the frequency characteristics of the simulated filters of different lengths and Fig. 11 shows the comparison of measured and ideal characteristics of the Goertzel filter of length 192.

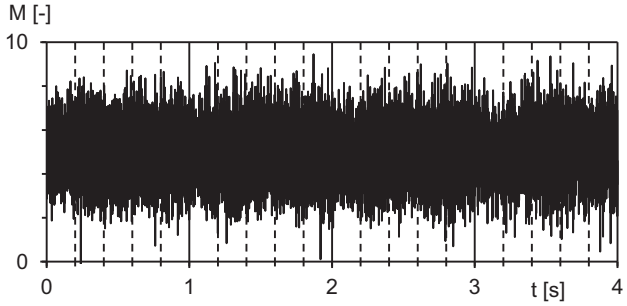


**Fig. 12.** Interfered DCF77 signal.

Fig. 12 shows the simulated DCF77 signal that is degraded by additive white Gaussian noise of SNR -3 dB and by interfering harmonic carrier. The interfering carrier is at a lower frequency by 100 Hz and has the same power as the DCF77 carrier. Such a signal is filtered by the Goertzel algorithm and the result is shown in Fig. 13.

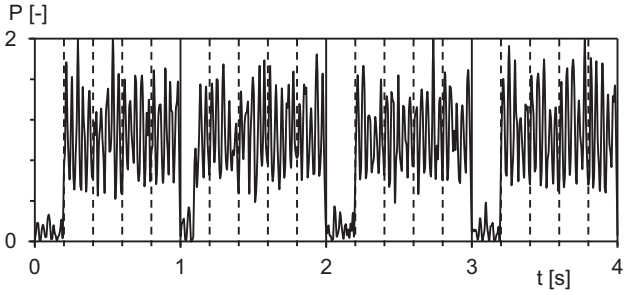


**Fig. 13.** Filtered DCF77 signal.

### 4.2 Step Correlator

Contours of the signal envelope are seen in Fig. 13, but the level of noise is still very high. The signal is therefore slightly averaged to reduce dispersion. The regular shape of the signal envelope allows using the correlator as a detector, and it also improves the signal to noise ratio. The correlation pattern is a single-step signal which is implemented as a multiplication by 1 and -1 respectively. The length of correlation is derived from the length of the shortest invariant part of the modulation signal, i.e. 100 ms for binary 0. The length of correlation *CL* is then computed from (8),

$$CL = 2 \cdot \frac{f_S \cdot t_{inv}}{GL} \cdot RF \tag{8}$$

where input parameters are ADC sampling frequency $f_S$, time of invariant part of signal $t_{inv}$, Goertzel length *GL* and reduction factor *RF*. The reduction factor is nearly one, and when the edges of the input signal are ideally sharp, then it equals one. However, a practical value is between 0.9 and 1 because of preceding averaging and limited signal bandwidth. When the signal of nearly the same shape as the correlation pattern or an inverted one (falling and rising edge respectively) comes to the input, high positive or negative peak will show up on the output of the correlator. That is clearly seen in Fig. 14; the decision levels of peak detectors are shown by dashed lines.

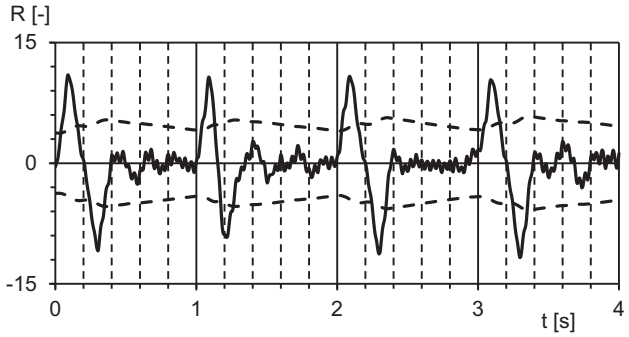


**Fig. 14.** Correlation peaks and decision levels.

### 4.3 Peak Detection

Correlation peaks can already be detected by the level comparator. The reference level is obtained by long term averaging of the correlated signal, which is first doubled and the sign is deprived. The shorter the correlation pattern, the wider and lower the correlation peak, therefore the maximum of the peak must also be found to get the precise position of the edge. The used algorithm only compares two adjacent samples, so it is very fast, but it can detect only local maxima. Since there are ripples at the maximum, the output signal of peak detector can look like a burst of spikes around the peak position, which can cause deviation from the right position. There are two solutions to this issue. The deviation can be considered to be too small to cause interference, or an additional filter removing spurious maximums can be used.

### 4.4 Averagers

Both used averagers are the realizations of an exponential moving average. The coefficient *C* is in interval $0 \div 1$ and sets the degree of averaging. The bigger the coefficient, the longer-term averaging is provided. The Signal diagram of the averager is shown in Fig. 15.

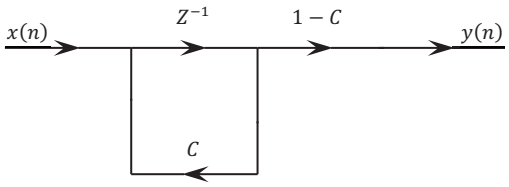


**Fig. 15.** Signal diagram of averager.

### 4.5 Data Locking

Each signal sample is marked with a time stamp of the time of acquisition. Positive peaks, falling edges, mark the start of seconds and it is wise to synchronize your own clocks to these marks, i.e. lock to seconds. Then the loss of the falling edge peak does not necessarily mean a loss of data. When a negative peak comes, it is easy to subtract the time of previous positive (second) peak from the time of coming peak and decide which data bit was probably sent. One more locking is needed to decode received bits. A minute lock is locked when no peak is received for a time longer than one second. Then data can be sent to the time decoder.

## 5 Measurement

A few measurements were done to make the system comparable with mass production receivers and to judge the implementation performance.

The prototype was put together from the previously mentioned preamplifier with a 5 cm long ferrite antenna. Such a circuit is connected to the evaluation board with an LPC2103 microcontroller on it. The preamplifier uses a 5 V on board power supply. Fig. 16 shows the picture of the prototype.

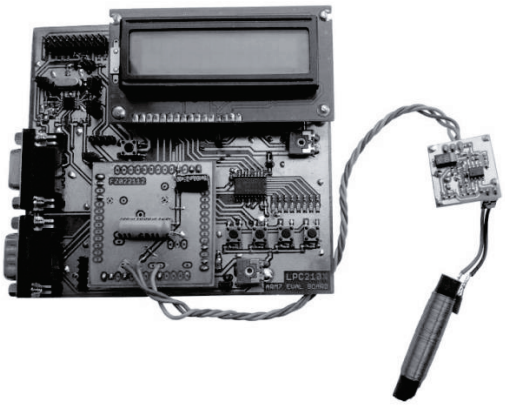

**Fig. 16.** DCF77 receiver prototype.

Program coefficients used for the tests are summarized in Tab. 2. These parameters were found experimentally.

| Goertzel length | 96 | 192 | 384 |
|---|---|---|---|
| Goertzel coefficient | 0.261 | 0.261 | 0.261 |
| pre-correlator averaging coefficient | 0.793 | 0.549 | 0.244 |
| correlation length | 50 | 24 | 12 |
| decision level averaging coefficient | 0.998 | 0.995 | 0.992 |

**Tab. 2.** Parameters used for testing application.

| Goertzel length | | 96 | 192 | 384 |
|---|---|---|---|---|
| interrupt | cycle count [-] | 14 | 14 | 14 |
| | time [µs] | 1.82 | 1.82 | 1.82 |
| | execution period [µs] | 41.7 | 41.7 | 4.17 |
| | CPU use [%] | 4.38 | 4.38 | 4.38 |
| demodulator | cycle count [-] | 157 | 99 | 70 |
| | time [µs] | 20.4 | 12.9 | 9.11 |
| | execution period [ms] | 4.00 | 8.00 | 16.0 |
| | CPU use [%] | 0.51 | 0.16 | 0.06 |
| decoder | cycle count [-] | 55 | 55 | 55 |
| | time [µs] | 7.16 | 7.16 | 7.16 |
| | execution period [ms] | 4.00 | 8.00 | 16.0 |
| | CPU use [%] | 0.18 | 0.09 | 0.04 |
| total CPU use [%] | | 5.07 | 4.63 | 4.48 |
| processing speed [cycle/s] | | 7680000 | | |
| interrupt period [µs] | | 41.7 | | |

**Tab. 3.** Computational demand measurement.

The first test was the measurement of computational demands on the processor. Testing was based on the measurement of cycle count by a peripheral counter afterwards converted into time. The program had to be divided into three parts to give precise results, therefore interrupt, demodulator and decoder subprograms were tested separately. The next parameter needed to be known was the period of execution of each part, which was derived from the ADC timing. Involving system parameters to the calculations gives the total CPU usage. All these measured values are summarized in Tab. 3. For comparison, tests were made for three values of Goertzel length. From results, it is seen that the computational demands of around 5 % are really low. The influence of variable Goertzel length is not significant. It is due to the concept where the Goertzel algorithm is processed within the interrupt section, which makes this section dominant in the issue of computational time demandingness.

Sensitivity is one of the most significant parameters of the receiver. To be able to compare results with datasheet parameters of available chips, the sensitivity was measured as a bit error ratio (BER) as a function of input voltage. A special program running on another evaluation board was developed to generate a testing DCF77 modulation signal. The signal was modulated to the carrier of 77.5 kHz by a low frequency function waveform generator. The RF signal was then attenuated and driven to the input of the preamplifier instead of the antenna. The measured characteristic is plotted in Fig. 17. Due to a low bit rate, which is characteristic for the DCF77 signal, evaluation of each point took several hours to get sufficient results. That is why the characteristic is not as accurate as expected from other systems.

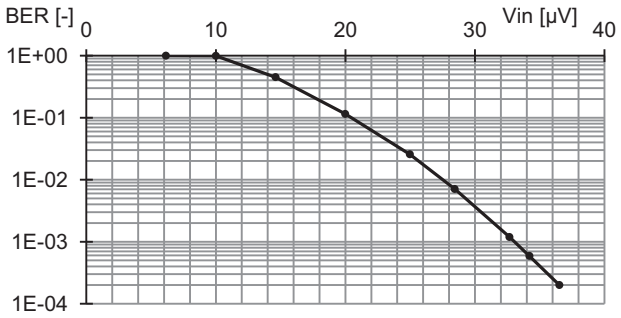


**Fig. 17.** Measured bit error ratio.

| Device | Supply range | Frequency range | Input voltage |
|---|---|---|---|
| U4221B | 2.4 ÷ 5.5 V | 60 ÷ 80 kHz | 1.75 µV ÷ 40 mV |
| MAS6180 | 1.1 ÷ 3.6 V | 40 ÷ 100 kHz | 1 µV ÷ 20 mV |
| CME8000 | 1.2 ÷ 5 V | 40 ÷ 120 kHz | 0.8 µV ÷ 50 mV |
| UE6005 | 1.1 ÷ 3.6 V | 40 ÷ 120 kHz | 0.6 µV ÷ 50 mV |
| SDR prototype | 5 V | 77.5 kHz | 28 µV ÷ 20 mV |

**Tab. 4.** Parameters of available receivers.

Since the data frame of the DCF77 system is fixed to 59 bit length, the BER for an errorless message should be higher than $1.13 \cdot 10^{-2}$. The value of the lowest input voltage can be derived from such. The value of the highest input voltage is specified by the maximal ADC saturation voltage and the preamplifier gain at carrier frequency. The test results are summarized in Tab. 4 and are compared with the integrated circuits available on the market.

The sensitivity of the prototype is quite poor. That is because of low gain of the preamplifier. Nevertheless, this solution subjectively gives highly sufficient results for distances over 500 km and the development of the analog front end is not the objective of this article. When used in a noisy environment or in more distant locations, it is necessary to improve the LNA. The proposed LNA can be replaced by a variable gain amplifier to perform automatic gain control (AGC). Texas Instruments produces the digitally controlled amplifier PGA202 [10], which is up to 60 dB instrumentation amplifier with high impedance differential input. Also, Linear Technology offers digital controlled gain amplifiers such as LTC6910 [11] with a low impedance input. For continuous gain control, AD604 [12] from Analog Devices is available.

# 6 Conclusion

The result of the provided experiments is a functional receiver prototype. It uses a low cost microcontroller in

combination with a tuned amplifier designed from common operational amplifiers. The advantage of the software defined DCF77 receiver is the ability to adapt easily to another modulation and coding scheme.

Using the Goertzel algorithm has the advantage of highly selective filtration combined with decimation. Implementation of such an algorithm even saves computational power due to its simplicity. Correlation used as a detector of edges allows to divide the signal into separate parts used for synchronization and data detection respectively and additionally improves the signal to noise ratio. CPU usage of around 5 % indicates that the core of the processor is idle most of the time. Therefore the microcontroller can be also used in more complicated systems where the DCF77 receiver acts only as an add-on, or the DCF77 application can be implemented into less powerful processors, e.g. an 8-bit microcontroller.

# References


[1] HKW-Elektronik GmbH, Germany. *UE6005 Time-Code Receiver IC (datasheet)*. 14 pages. [Online]. 2001, Rev. A10, Cited 2011-12-19. Available at: http://www.datasheetarchive.com/dl/Datasheets-316/627876.pdf

[2] TEMIC TELEFUNKEN microelectronic GmbH, Germany. *U4221B Radio Controlled Clock Receiver (datasheet)*. 12 pages. [Online]. 1996, Rev. A1, Cited 2012-6-20. Available at: http://www.datasheetcatalog.org/datasheet/Temic/mXyzuryz.pdf

[3] Micro Analog Systems Oy, Finland. *MAS6180 AM Receiver IC (datasheet)*. 14 pages. [Online]. 2011, Rev. DA6180B.002, Cited 2012-11-8. Available at: http://www.mas-oy.com/uploads/Data%20sheets/da6180B.pdf

[4] C-MAX Time Solutions GmbH, Germany. *CME8000 RC Receiver IC (datasheet)*. 21 pages. [Online]. 2005, Rev. B.11, Cited 2012-11-8. Available at: http://datasheet.octopart.com/CME8000-DDTB-C-Max-datasheet-46588.pdf

[5] NXP B. V., *UM10161 LPC2101/02/03 User Guide (datasheet)*. 292 pages. [Online]. 2009, Rev. 4, Cited 2011-07-16. Available at: http://www.nxp.com/documents/user_manual/UM10161.pdf

[6] BAUCH, A., HETZEL, P., PIESTER, D. Time and frequency dissemination with DCF77: From 1959 to 2009 and beyond. *PTB-Mitteilungen: Amts- und Mitteilungsblatt der Physikalisch-Technischen Bundesanstalt*, 2009, No. 3. ISSN 0030-834X. [Online] Available at: http://www.ptb.de/cms/fileadmin/internet/fachabteilungen/abteilung_4/4.4_zeit_und_frequenz/pdf/PTBM_50a_DCF77_engl.pdf

[7] MORALES, M. A. V., Cypress MicroSystems, Inc., *Radio Controlled Calendar Clock. (Application note)*. 12 pages [Online]. 2010, Rev. A, Cited 2011-12-19. Available at: http://www.cypress.com

[8] STRAW, R. D. *The ARRL antenna book*. 21st ed. Newington (CT, USA): ARRL, 2007.

[9] OPPENHEIM, A. V., SCHAFER, R. W., BUCK, J. R. *Discrete-time signal processing*, 2nd ed. Upper Saddle River (NJ, USA): Prentice Hall, 1999.

[10] TEXAS INSTRUMENTS, *PGA202 (datasheet)*. 11 pages. [Online]. 2000, Cited 2013-02-26. Available at: http://www.ti.com/lit/ds/symlink/pga202.pdf

[11] LINEAR TECHNOLOGY, *LTC6910 (datasheet)*. 24 pages. [Online]. 2002, Rev. A, Cited 2013-02-26. Available at: http://cds.linear.com/docs/en/datasheet/6910123fa.pdf

[12] ANALOG DEVICES, *AD604 (datasheet). 32 pages.* [Online]. 2010, Rev G, Cited 2013-02-26. Available at: http://www.analog.com/static/imported-files/data_sheets/AD604.pdf


# Acknowledgements

The research was performed in laboratories supported by the SIX project no. CZ.1.05/2.1.00/03.0072, the operation program Research and Development for Innovation and by the Wireless Communication Teams project no. EE2.3.20.0007.

# About Authors ...

**Filip ZÁPLATA** was born in Chrudim, Czech Republic in 1987. He received the M.Sc. degree in 2011 in Electronics and Communications from the Brno University of Technology (BUT). From 2011, he was a combined Ph.D. student and simultaneously working as an R&D Engineer in Vesla s.r.o. Since 2012 he has been a full-time Ph.D. student at the Department of Radio Electronics, BUT. His research interests include digital signal processing algorithms for software defined radio and digital receiver technology.

**Miroslav KASAL** was born in Litomysl, Czech Republic, graduated in Communication Engineering from the Faculty of Electrical Engineering, Brno University of Technology, in 1970. In 1984 he obtained his Ph.D. degree in metering engineering. He was the head of the NMR Department and Electronics Laboratory of the Institute of Scientific Instruments, Academy of Science of the Czech Republic (1991-2002). Since 2002 he has been with the Department of Radio Engineering, Faculty of Electrical Engineering and Communication, Brno University of Technology as professor. He is a senior member of the IEEE. In 2007 prof. Kasal received the Prize for research of the Minister of Education of the Czech Republic.