Package and PCB Effects Shift Intermodulation Notch in an RF Common-Emitter Amplifier

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Abstract. A Taylor series analysis is conducted to study the effects of the package and printed circuit board (PCB) on the intermodulation nulling of an RF common-emitter amplifier. The equivalent parasitic element of the package and PCB interconnects is extracted from the impedance and admittance parameters, which are obtained using a three-dimensional (3-D) electromagnetic simulation tool. The theoretical analysis reveals that the effects of the package and PCB on the intermodulation nulling of common-emitter amplifiers is to shift the intermodulation notch; that the third-order intermodulation (IM3) products under an original bias condition cannot be suppressed and that the linearity of common-emitter amplifiers is thereby degraded. A comparison between theory and simulation reveals good agreement in the predicted locations of the intermodulation notch in the absence and presence of a package and PCB.

Keywords
Package and printed circuit board (PCB) effects, intermodulation nulling, common-emitter amplifier, Taylor series.

1. Introduction

The most important parameter that determines the linearity of RF amplifiers is the third-order intermodulation distortion. The transistors are essential to RF amplifiers. An intermodulation nulling technique can be used to cancel out the third-order and fifth-order nonlinear terms of a transistor to create an intermodulation notch to suppress the third-order intermodulation (IM3) products, increasing the linearity of the amplifier [1]. Therefore, the intermodulation nulling technique is commonly applied in small-signal amplifiers [2], driver amplifiers [3], power amplifiers [4], and low-noise amplifiers [5], [6].

Most manufactured RF amplifiers must be packaged for use on a printed circuit board (PCB). A package structure must be small and highly integrated, and exhibit low parasitic and high thermal dissipation to meet the demands of RF applications [7]. In practice, wirebond packages typically act as low-pass filters that reduces the operating bandwidth [8], [9]. Wirebond packages also shift the input impedance of a low-noise amplifier away from the optimum point in noise-figure matching [10], [11]. The package and PCB increase the error vector magnitude (EVM) and degrade the sideband suppression of a quadrature modulator [12]. In an upconverter, the package and PCB reduce the conversion gain and the adjacent channel power ratio (ACPR) [13]. The effects of the package and PCB on intermodulation nulling of the amplifier have been rarely discussed.

This study investigates the effects of the package and PCB on the intermodulation nulling of a 2.4 GHz common-emitter amplifier. The common-emitter amplifier is designed by an InGaAs heterojunction bipolar transistor (HBT) foundry process with an $f_T$ of up to 30 GHz. In Section 2, a Taylor series is used to analyze the intermodulation nulling in the common-emitter amplifier with or without inclusion of the package and PCB parasitic elements. Then, Section 3 demonstrates the careful extraction of the equivalent parasitic element of the package and PCB interconnects from the impedance and admittance parameters, which are obtained using ANSYS’s High Frequency Structure Simulator (HFSS). Next, Section 4 compares the theoretical results with the simulation results and presents a discussion of these results. Finally, Section 5 draws conclusions.

2. Intermodulation Nulling Analysis

Fig. 1 shows a common-emitter amplifier in conjunction with the parasitic elements of package and PCB interconnects. Notably, $Q$ is the bipolar transistor in the common-emitter configuration. $V_{BB}$ and $V_{CC}$ are the base bias voltage and collect bias voltage, respectively. $v_i$ represents the signal input voltage. $v_{BB}$ is the base-emitter voltage. $i_c$ is the collector current. Its direct current (DC) component is represented by $I_c$. $R_b$ and $R_e$ are the base intrinsic resistance and emitter intrinsic resistance, respectively. $L_C$ is the RF choke. $C_B$ is the DC-block capacitor.

In Fig. 1, the equivalent parasitic circuit that is connected to the input terminal of the common-emitter ampli-
The $i_c$ can be expressed as a function of $v_s$ by substituting (2) into (1), and is represented by $i_c(v_s)$. To analyze the intermodulation distortion, $i_c(v_s)$ is written as a Taylor series expansion about the $V_{BB}$ up to fifth order. The term $n$ is said to denote the order of a Taylor series. A Taylor coefficient is defined as the $n$th derivative of $i_c(v_s)$ with respect to $v_s$ at $V_{BB}$ divided by the factorial of $n$. This definition of Taylor coefficient is further derived in terms of circuit elements as:

$$G_{1,p} = \frac{d i_c(v_s)}{dv_s} \bigg|_{v_s = V_{sa}}$$

$$= \frac{1}{Y_p Z_s + 1} V_T + I_C N$$

$$G_{2,p} = \frac{1}{2!} \frac{d^2 i_c(v_s)}{dv_s^2} \bigg|_{v_s = V_{sa}}$$

$$= \frac{1}{2 Y_p Z_s + 1} \left( V_T + I_C N \right)^2$$

$$G_{3,p} = \frac{1}{3!} \frac{d^3 i_c(v_s)}{dv_s^3} \bigg|_{v_s = V_{sa}}$$

$$= \frac{1}{3 Y_p Z_s + 1} \left( V_T + I_C N \right)^3$$

$$\times \left[ G_{2,p} \left( V_T + I_C N \right) - \left( G_{1,p} \right)^2 N \right]$$

$$G_{4,p} = \frac{1}{4!} \frac{d^4 i_c(v_s)}{dv_s^4} \bigg|_{v_s = V_{sa}}$$

$$= \frac{1}{4 Y_p Z_s + 1} \left( V_T + I_C N \right)^2$$

$$\times \left[ G_{3,p} - \frac{2 G_{1,p} G_{2,p} N}{V_T + I_C N} + \left( G_{1,p} \right)^3 N^2 \right]$$

$$G_{5,p} = \frac{1}{5!} \frac{d^5 i_c(v_s)}{dv_s^5} \bigg|_{v_s = V_{sa}}$$

$$= \frac{1}{5 Y_p Z_s + 1} \left( V_T + I_C N \right)^2$$

$$\times \left[ G_{4,p} - \frac{2 G_{1,p} G_{2,p} N + \left( G_{1,p} \right)^2 N}{V_T + I_C N} \right]$$

$$+ \frac{3 \left( G_{1,p} \right)^2 G_{2,p} N^2}{\left( V_T + I_C N \right)^2} - \left( G_{1,p} \right)^4 N^3 \right]$$

The $i_c$-v$_{BE}$ characteristic of the bipolar transistor $Q$ is an exponential function and can be expressed as

$$i_c = I_s \exp(v_{BE}/V_T)$$

(1)

where $I_s$ represents the saturation current. In (1), $V_T$ is the thermal voltage, which is approximately 0.026 V at room temperature. In the circuit that is shown in Fig. 1, the formula that relates $v_{BB}$ to $v_s$ is determined from Kirchhoff's Voltage Law (KVL), and is derived as

$$v_{BE} = \frac{1}{Y_p Z_s + 1} v_s - \left( \frac{Z_s}{Y_p Z_s + 1} + R_b \right) \frac{i_c}{\beta}$$

(2)

where $\beta$ is the common-emitter current gain and $\alpha$ is the common-base current gain. Notably, (2) relates $v_{BB}$ to $v_s$ in terms of the parasitic elements of the package and PCB interconnects. Such a formula for a bare chip, which is one without package and PCB can be obtained by setting $Z_s$, $Y_p$, and $Z_g$ to zero in (2).
where

\[ N = \frac{Z_s}{Y_p Z_s} + 1 \frac{R_b}{\beta} + \frac{R_e + Z_g}{\alpha}. \]  \hspace{1cm} (8)

Notably, (3)-(8) give first-order to fifth-order coefficients of a Taylor series expansion including the parasitic elements of the package and PCB interconnects. Again, the formulas without package and PCB effects are obtained by setting \( Z_s, Y_p, \) and \( Z_g \) to zero in (3)-(8). Their coefficients of a Taylor series up to the fifth order are \( G_{1,c}, G_{2,c}, G_{3,c}, G_{4,c}, \) and \( G_{5,c}. \)

The time-dependent input voltage is a cosine function. A two-tone input voltage, therefore, can be expressed as \( A (\cos \omega_1 t + \cos \omega_2 t) \), where \( A \) is the amplitude, and \( \omega_1 \) and \( \omega_2 \) are two closely spaced angular frequencies, respectively, and \( t \) is time. A Taylor series expansion of \( i_c(t) \) up to fifth order yields the IM3 products of \( i_c \) excluding and including the package and PCB interconnects as

\[
i_{c,IM3} = \left( \frac{3A^3}{4} \left[ G_{3,c} \right] + \frac{50A^5}{16} \left[ G_{5,c} \right] \right) \cos (2\omega_1 - \omega_2) t. \] \hspace{1cm} (9)

This expansion clearly reveals that the IM3 products are closely related to the third-order and fifth-order coefficients of the Taylor series. Intermodulation nulling occurs when the amplitude of the IM3 product is zero such that

\[
\begin{bmatrix}
G_{3,c} \\
G_{3,p}
\end{bmatrix} = \frac{-25A^2}{6} \begin{bmatrix}
G_{5,c} \\
G_{5,p}
\end{bmatrix}.
\] \hspace{1cm} (10)

From (10), one important condition of the intermodulation nulling is that the third-order and fifth-order Taylor coefficients have opposite signs.

Finally, in this Taylor series analysis, \( G_{3,c}, G_{5,c}, G_{3,p}, \) and \( G_{5,p} \) are calculated using the following parameters that are obtained using the HBT foundry SPICE model, with \( I_s \) equal to \( 10^{-24} \) A, \( R_b \) equal to 18 \( \Omega \), \( R_e \) is 0.8 \( \Omega \), \( \beta \) equal to 120, and \( \alpha \) equal to 0.99. The equivalent parasitic element of the package and PCB interconnects is extracted below.

3. Extraction of Parasitic Elements of Package and PCB Interconnects

Generally, manufactured RF amplifiers must be packaged for use on test boards. Fig. 2 shows the three-dimensional (3-D) configuration of the bondwire in a package and the metal trace on a PCB, which is connected to the input terminal of the common-emitter amplifier. It is established in the HFSS to extract their equivalent parasitic elements. The HFSS is an electromagnetic (EM) simulation tool that is based on 3-D full-wave methodology. The bondwire in a package is made of gold. The diameter and length of the bondwire are set to 0.025 mm and 1.28 mm, respectively. The metal on the PCB is copper and its thickness is 0.035 mm. Fig. 2 presents the dimensions of a metal trace on a PCB. The FR-4 glass epoxy panel of a PCB has a thickness of 1.6 mm. Fig. 3 shows the two-port lumped-element equivalent circuit of the bondwire and metal trace interconnects. The figure presents the equivalent circuit of the bondwire and metal trace interconnects, obtained from Fig. 1 to derive the formulas for the equivalent parasitic elements, \( R_i, C_i, \) and \( L_i. \)

![Fig. 2. 3-D configuration of package and PCB interconnects shown in HFSS for evaluating equivalent bond-wire and metal trace parasitic elements.](image)

![Fig. 3. Two-port lumped-element equivalent circuit of bond-wire and metal trace interconnects.](image)

Based on the definitions of the impedance parameters of two-port networks, \( Z_{11}, \) and \( Z_{22}, \) the input impedances looking into ports 1 and 2, respectively, are

\[
Z_{11}(\omega) = R_i + j \left( \omega L_i - \frac{1}{\omega C_i} \right), \] \hspace{1cm} (11)

\[
Z_{22}(\omega) = -\frac{j}{\omega C_i}. \] \hspace{1cm} (12)

Resonance occurs when the imaginary part of \( Z_{11} \) is zero. The resonant angular frequency \( \omega_{0,i} \) can be derived as

\[
\omega_{0,i} = \frac{1}{\sqrt{L_i C_i}}. \] \hspace{1cm} (13)

\( Z_{11} \) at \( \omega_{0,i} \) is \( R_i \), which is a purely real impedance. Hence, \( R_i \) at resonance is

\[
R_i = \left| Z_{11}(\omega = \omega_{0,i}) \right|. \] \hspace{1cm} (14)

From (12), taking the imaginary part of \( Z_{22} \) and rearranging yields \( C_i \) in the following form:

\[
C_i = \frac{-1}{\omega \text{Im} \{ Z_{22}(\omega) \}}. \] \hspace{1cm} (15)
Squaring both sides of (13) and rearranging to find $L_i$ yields

$$L_i = \frac{1}{\omega_{0,i}^2 C_i}. \quad (16)$$

The impedance parameters for bondwire and metal trace interconnects of the package and PCB, shown in Fig. 2, can be evaluated by performing an HFSS simulation. Fig. 4 plots the imaginary part of $Z_{11}$ to determine the resonant frequency ($f_{0,i}$). $f_{0,i}$ is found to be 6.84 GHz. Fig. 5 plots the magnitude of $Z_{11}$, which gives $R_i$. According to (14), $R_i$ is the absolute value of $Z_{11}$ at $f_{0,i}$, and in this case is 1.076 $\Omega$. Fig. 6 plots the imaginary part of $Z_{22}$ to obtain $C_i$. As indicated in Fig. 6, the imaginary part of $Z_{22}$ at 2.4 GHz is $-123 \Omega$. Then, $C_i$ is calculated as 0.539 pF by (15). Substituting $f_{0,i}$ and $C_i$ into (16) yields an $L_i$ of 1.01 nH.

Fig. 7 presents the 3-D configuration of ground for package and PCB interconnects, which is connected between the ground terminal of the common-emitter amplifier and the bottom ground plane of the PCB. Fig. 7 presents the dimensions of the ground interconnects. The radius of the via is set to 0.15 mm. Fig. 8 shows the one-port lumped-element equivalent circuit of the ground interconnects. Again, the figure presents the equivalent circuit of the ground interconnects, obtained from Fig. 1 to derive clearly the extraction formulas for equivalent parasitic elements, $R_g$, $C_g$, and $L_g$.

![Fig. 7. 3-D configuration of package and PCB interconnects shown in HFSS used to evaluate equivalent ground parasitic elements.](image)

![Fig. 8. One-port lumped-element equivalent circuit of ground interconnects.](image)

In Fig. 8, $Y_{11}$ is the input admittance looking into port G. The $Y_{11}$ is obtained by connecting $R_g$ and $L_g$ in series and then shunting $C_g$:

$$Y_{11}(\omega) = \frac{1}{R_g + j\omega L_g} + j\omega C_g = \frac{R_g + j\omega(\omega^2 C_g L_g^2 - L_g + C_g R_g^2)}{R_g^2 + (\omega L_g)^2}. \quad (17)$$

At low frequency, $Y_{11}$ is simplified to

$$Y_{11}(\omega) \approx \frac{1}{R_g} \quad \text{for low } \omega. \quad (18)$$

At high frequency, $Y_{11}$ is simplified to

$$Y_{11}(\omega) \approx j\omega C_g \quad \text{for high } \omega. \quad (19)$$

From (18), taking the real part of $Y_{11}$ and then rearranging yields $R_g$:

$$R_g \approx \frac{1}{\text{Re}\{Y_{11}(\omega)\}} \quad \text{for low } \omega. \quad (20)$$
According to (19), $C_g$ is obtained by taking the imaginary part of $Y_{11}$ and rearranging as

$$C_g \approx \frac{1}{\omega} \text{Im} \{Y_{11}(\omega)\} \quad \text{for high } \omega. \quad (21)$$

Resonance occurs when the imaginary part of $Y_{11}$ is zero:

$$\omega_{0,g}^2 C_g L_g^2 - L_g + C_g R_g^2 = 0 \quad (22)$$

where $\omega_{0,g}$ represents the resonant angular frequency of the ground for the package and PCB interconnects. Notably, (22) for $L_g$ is quadratic, so its solution is

$$L_g = \frac{1 \pm \sqrt{1 - 4(\omega_{0,g}^2 C_g R_g)^2}}{2\omega_{0,g}^2 C_g} \quad (23)$$

If $1 \gg 4(\omega_{0,g}^2 C_g R_g)^2$, then $1 - 4(\omega_{0,g} C_g R_g)^2 \approx 1$, allowing (23) to be simplified to the following form to yield $L_g$:

$$L_g \approx \frac{1}{\omega_{0,g}^2 C_g} \quad (24)$$

The $Y_{11}$ of the ground interconnects of the package and PCB, shown in Fig. 7, can be obtained from the EM-simulated admittance parameters using the HFSS. Fig. 9 plots the real part of $Y_{11}$ to obtain $R_g$. As presented in the figure, the real part of $Y_{11}$ at 1 MHz is 107 $\Omega$. From (20), $R_g$ is the reciprocal of the real part of $Y_{11}$, which, in this instance, is 9.346 m$\Omega$. Fig. 10 plots the first resonant frequency ($f_{0,g}$). The $f_{0,g}$ is obtained as 15.643 GHz.

To extract $C_g$ accurately, Fig. 11 plots the imaginary part of $Y_{11}$ with much higher frequency than $f_{0,g}$. Fig. 11 reveals that the imaginary part of $Y_{11}$ at 17.18 GHz is 0.049 $\Omega$. $C_g$ is then found to be 0.454 pF using (21). Substituting $f_{0,g}$ and $C_g$ into (24) yields $L_g$ as 0.228 nH. Tab. 1 lists the extracted parasitic elements of the package and PCB interconnects.

![Fig. 9. Determination of $R_g$ from real part of $Y_{11}$.](image)

![Fig. 10. Determination of $f_{0,g}$ from imaginary part of $Y_{11}$.](image)

![Fig. 11. Determination of $C_g$ from imaginary part of $Y_{11}$ with much higher frequency than $f_{0,g}$.](image)

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<thead>
<tr>
<th>$R$</th>
<th>$C_g$</th>
<th>$L_g$</th>
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<tbody>
<tr>
<td>1.076 $\Omega$</td>
<td>0.539 pF</td>
<td>1.01 nH</td>
</tr>
<tr>
<td>9.346 m$\Omega$</td>
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Tab. 1. Extracted parasitic elements of package and PCB interconnects.

4. Results and Discussion

Tab. 1 presents the parasitic elements, which can be used to calculate the third-order and fifth-order Taylor coefficients with the package and PCB effects using (3) to (8). Notably, the third-order and fifth-order Taylor coefficients without the package and PCB interconnects can be easily obtained by setting all values of the parasitic elements to zero in (3)-(8). Fig. 12 plots the calculated $G_{3,c}$ and $G_{5,c}$ versus $V_{BB}$. The figure reveals that $G_{3,c} = -6.805$ and $G_{5,c} = 619.41$ at $V_{BB} = 1.36$ V. $G_{3,p}$ and $G_{5,p}$ have opposite signs, satisfying the intermodulation nulling condition in (10). Fig. 13 plots the calculated $G_{3,p}$ and $G_{5,p}$ versus $V_{BB}$. At $V_{BB} = 1.36$ V, $G_{3,p} = -0.34$ and $G_{5,p} = -3.164$. $G_{3,p}$ and $G_{5,p}$ have the same sign, not satisfying the intermodulation nulling condition that is constrained by (10). Additionally, $G_{3,c}$ is less than $G_{3,p}$ while $G_{5,c}$ greatly exceeds $G_{5,p}$. The parasitic elements of the package and PCB interconnects vary not only in sign but also in their first-order to fifth-order Taylor coefficients, shifting the intermodulation notch at $V_{BB} = 1.36$ V.

To create an intermodulation notch for the common-emitter amplifier, $V_{BB}$ is set to 1.36 V. A $V_{CC}$ of 3 V is used with a current consumption of 22.36 mA. In a two-tone test, the central frequency and frequency spacing are set to 2.4 GHz and 5 MHz, respectively. The amplitude of a two-tone input voltage is set to 0.051 V. Figs. 14 and 15 compare the theoretical and simulated output powers of the IM3 products ($P_{IM3}$) in the common-emitter amplifier without
and with the package and PCB effects, respectively. The theoretical $P_{\text{IM3}}$ are calculated as follows.

$$P_{\text{IM3}} = \frac{1}{2} \left( i_{C,\text{IM3}} \right)^2 Z_L$$  \hspace{1cm} (25)

where $Z_L$ is the output load impedance of the common-emitter amplifier, which, in this instance, is 50 $\Omega$. (9) gives the $i_{C,\text{IM3}}$. The simulation results are generated using an Agilent’s Advanced Design System (ADS). Theory and the simulation agree closely in their predictions of the location of intermodulation notches without and with the package and PCB effects.

Fig. 14 presents that, as $V_{BB}$ is swept, the IM$_3$ products encounter a notch at 1.36 V. However, this intermodulation notch is shifted down to 1.297 V when the package and PCB effects are included, as shown in Fig. 15. In Fig. 14, the theoretical result shows that the IM$_3$ power at $V_{BB} = 1.36$ V is $-56.77$ dBm. Fig. 15 indicates that the theoretical IM$_3$ power at $V_{BB} = 1.36$ V increase to $-44.61$ dBm after including the package and PCB effects. Therefore, under an original bias condition, the IM$_3$ products cannot be suppressed when the intermodulation notch is shifted. The package and PCB actually worsen the third-order intermodulation distortion and reduces linearity.

5. Conclusions

The intermodulation nulling of RF common-emitter amplifiers with the package and PCB effects was studied using a Taylor series. An analysis verified by simulation reveals that the dominant effect is the shift in the intermodulation notch of common-emitter amplifiers. The shifted intermodulation notch cannot suppress the IM$_3$ produces at an original bias condition so the linearity is degraded.

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References


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