Tunable Balun Low-Noise Amplifier in 65 nm CMOS Technology

Johannes STURM[1], *Marcus GROINIG*[1], *Xinbo XIANG*[1,2]

[1]Dept. of Integrated Systems and Circuits Design, Carinthia University of Applied Sciences, Villach, Austria
[2]Lantiq A GmbH, Villach, Austria

j.sturm@cuas.at

Abstract. *The presented paper includes the design and implementation of a 65 nm CMOS low-noise amplifier (LNA) based on inductive source degeneration. The amplifier is realized with an active balun enabling a single-ended input which is an important requirement for low-cost system on chip implementations. The LNA has a tunable band-pass characteristic from 4.7 GHz up to 5.6 GHz and a continuously tunable gain from 20 dB down to 2 dB, which enables the required flexibility for multi-standard, multi-band receiver architectures. The gain and band tuning is realized with an optimized tunable active resistor in parallel to a tunable L-C tank amplifier load. The amplifier achieves an IIP3 linearity of -8 dBm and a noise figure of 2.7 dB at the highest gain and frequency setting with a low power consumption of 10 mW. The high flexibility of the proposed LNA structure together with the overall good performance make it well suited for future multi-standard low-cost receiver front-ends.*

Keywords

Low-noise amplifier, LNA, variable gain, tunable band, multi-standard receiver.

1. Introduction

Modern wireless communication systems including multimedia capabilities are developing at high pace, with an increasing number of wireless standards for mobile cellular communication (eg. GSM/EDGE, UMTS, LTE), broadcast applications like DVB-SH, and short-range data communication standards like the IEEE 802.11 WLAN or Bluetooth. To take advantage of the services provided by these mobile communication standards, the integration of multi-standard, multi-band terminals in a single radio architecture with a minimized number of external RF components is necessary. This requires novel RF architectures in advanced low-cost CMOS technologies, based on software defined radio and cognitive radio concepts. The wide spread of frequency bands from 0.1 GHz up to about 6 GHz, in combination with the high number of concurrent applications, makes the classical integration approach of independent parallel receiver-frontends more and more inefficient and technically demanding. Reusability and tunability of RF key-building blocks like low-noise amplifiers (LNA) will be a mandatory requirement for future RF transceivers. To reduce the RF performance limitations of modern CMOS technologies like low-gain, low supply voltage and high technology variations, new digitally assisted RF radio solutions can be used to leverage the signal-processing and integration capabilities of CMOS technologies.

Wideband CMOS LNAs with high linearity and gain as a main building block for multi-standard RF front-ends were strongly researched during the past years [1, 2, 3, 4, 5]. A main issue for wide-band LNAs in multi-standard radios is strong blockers of neighboring bands, which require high-quality external RF filters and very high LNA linearity. Some selectivity of the LNA gain would relax the external filter quality, reducing the costs significantly. This can be achieved by a tunable band-pass characteristic of the LNA gain as it will be discussed in this paper.

To minimize the costs of external components, a differential LNA input should be avoided by using an integrated balun. As on-chip baluns either passive transformers or active baluns can be used. Passive transformers usually consume large area and the gain loss limits the overall noise figure (NF). Furthermore passive baluns are usually narrow-band devices which make them unusable for reconfigurable multi-band solutions. In contrast, an active balun LNA can provide a wide-band input impedance matching with improved power and area.

Due to the mentioned variety of wireless applications, the LNA gain should ideally be programmable over a wide range, with a high granularity. For wideband LNAs usually common-gate amplifiers or negative feedback common-source stages with integrated noise cancelation techniques are used [1, 5]. A programmable gain is typically implemented by switchable resistors and inductors or programmable transistor transconductance [7, 6], where high gain granularity can only be achieved by complex switching networks causing performance degradation. Also resistive or capacitive ladder attenuators in combination with multiple amplifier configurations are reported [8]. Distributed amplifiers can be used to create multi-gain LNAs [9] with

the drawback of significant area consumption. All mentioned methods allow only a limited number of gain steps, since complex switching networks would degrade the amplifier performance and increase chip area.

In this paper, we will present a strongly re-configurable balun LNA with a tunable band-pass filter characteristic from 4.7 GHz to 5.6 GHz, which should mainly cover the upcoming 801.11ac WLAN band. The proposed LNA has also a tunable gain over a wide range from about 2 dB up to 20 dB. This unique flexibility makes the LNA well-suited for future multi-band RF frontends. The LNA achieves a NF of 2.7 dB with a low power consumption of 10 mW at a single 1.2 V supply. In Section 2, two different balun LNA topologies will be compared, leading to the proposed solution of the source degeneration LNA. The tunable gain strategy is presented in Section 3 while the circuit implementation of the proposed LNA is presented in Section 4. Measurement results and comparison with recent publications are summarized in Section 5 and Section 6.

2. Proposed Balun Topology

A classical solution for baluns are transformer based inductors, which usually consume a large silicon area. Two different topologies of active balun LNA's to convert a single-ended LNA input signal to a balanced differential output signal are shown in Fig. 1.

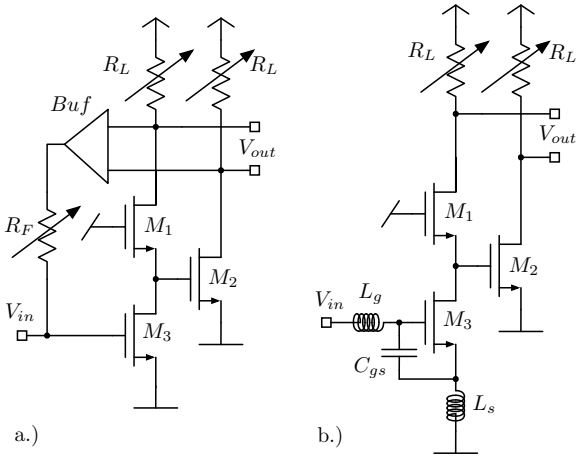


Fig. 1. Balun LNA topologies based on buffered resistive feedback (a) and inductive source degeneration input (b).

A wide-band single-ended to differential conversion LNA topology based on resistive feedback is shown in Fig. 1(a) [1, 4]. The circuit includes a common-source amplifier (M_3) as input stage. For single-ended to differential conversion a common-gate stage M_1 in combination with a common-source stage M_2 is used. The amplifier includes noise cancelation for the transistor M_1 channel noise. Careful biasing can also provide a good amplifier linearity by distortion cancelation. To match the input impedance of the CS amplifier, Fig. 1(a) uses a resistive buffered feedback amplifier configuration, providing wide-band input impedance matching by negative shunt feedback. The noise of this circuit can be minimized by a high feedback resistor R_F, thus leading to a high LNA closed-loop gain. Another dominant noise factor is the CS input transistor M_3, which can be optimized by a high transconductance g_m.

An alternative solution of an integrated balun LNA implementation is shown in Fig. 1(b). This LNA employs inductive source degeneration at the input transistor M_3 in combination with a common-source, common-gate balun stage [10]. For this topology noise matching and impedance matching can be simultaneously optimized. To improve the noise figure, the transconductance g_{M3} of the input transistor should be as high as possible. This also reduces the noise contribution as well as gain/phase mismatch of the second stage. The amplifier voltage gain is defined as [12]

$$A_V = g_{m,eff} R_{load} = Q_{in} g_{M3} 2R_L \tag{1}$$

where Q_{in} is the effective quality factor of the LNA input matching network, at series resonance. The input impedance defined by transistor M_3 and the inductors L_g and L_s is

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \frac{g_{M3} L_s}{C_{gs}}. \tag{2}$$

With careful dimensioning of L_g, L_s, and g_{M3} the LNA input impedance can be matched to 50 Ω with minimized noise figure. Inductive source degeneration structures can be optimized to the lowest noise levels for a given power consumption [11], with the disadvantage of large area due to inductors L_s and L_g.

For implementation of a tunable amplifier gain, the topology in Fig. 1(a) has the disadvantage, that both, feedback resistor R_F (closed-loop gain) and amplifier open-loop gain needs to be carefully tuned simultaneously to keep input impedance matching for each gain setting. In comparison, the gain tuning for an inductive source degeneration LNA in Fig. 1(b) can be realized by simply tuning the amplifier load impedance, while the input impedance keeps matched. The noise performance of Fig. 1(b) can be optimized to good values with a low power consumption. Therefore the proposed LNA circuit is based on inductive source degeneration concept and will be introduced in Section 4.

The following Section will present the implementation of a tunable load impedance based on an active MOS resistor to realize a tunable gain LNA.

3. Tunable Active Resistor

A basic gain control concept for source degeneration LNA is indicated in Fig. 1(b). The realization of variable gain requires tunable resistors with excellent noise, linearity, and bandwidth performance. The amplifier gain is mainly defined by the effective transconductance of the amplifier $g_{m,eff}$ and the load resistor R_L as indicated in (1). With a tunable load resistor R_L the LNA gain can be tuned without significantly degrading the input impedance matching. In the

proposed implementation, quasi-floating gate bi-directional MOS resistors are used to enable continuously tunable amplifier gain over a wide range. Even the field of continuously tunable active MOS resistors is already well established for low frequency variable gain amplifiers and filters [13], we have also demonstrated their usability for RF-applications [20].

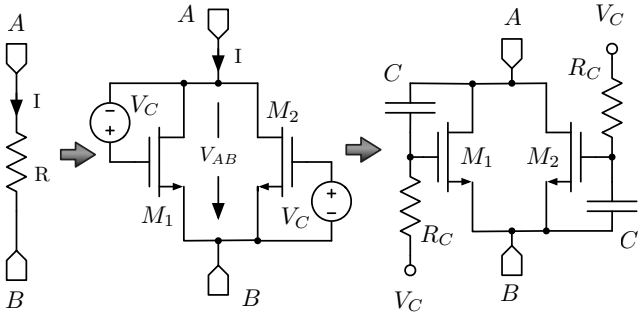


Fig. 2. Tunable active resistor (ACR) concept for R_L with linearity optimized MOS resistors and quasi floating gate implementation.

A linearity optimized active resistor can be implemented with two parallel MOS transistors $M1$ and $M2$ biased in triode region as shown in Fig. 2 [14]. To compensate for non-linearity, the quasi-floating transistor gates are connected with a high value resistor R_C to a control voltage V_C and are AC-coupled to the resistor pins A and B. Assuming both transistors $M1$ and $M2$ have the same dimensions, the operating conditions are restricted to

$$V_{AB} \leq (V_C - V_{FB} - 2\phi_F) \tag{3}$$

where V_{FB} is the transistor flat-band voltage and Φ_F is the Fermi potential. If V_A is higher than V_B (as shown in Fig. 2), the current I flowing from node A to node B can be calculated as

$$I = \frac{2W_{1,2}}{L_{1,2}} K_P \left\{ (V_C - V_{FB} - 2\phi_F) V_{AB} - \cdots \right. \\ \left. \frac{2}{3}\gamma \left[(2\phi_F + V_A)^{\frac{3}{2}} - (2\phi_F + V_B)^{\frac{3}{2}} \right] \right\} \tag{4}$$

where γ is the body-effect constant and K_P is the gain factor of the transistors. The second order non-linearity of a single MOS transistor is mainly canceled in the current equation. The nominal conductance g of this active resistor (ACR) structure is almost independent on voltage $V_{A,B}$ and can be tuned by a control voltage V_C according to

$$g = \frac{1}{R} \approx 2\frac{W_{1,2}}{L_{1,2}} K_P (V_C - V_{FB} - 2\Phi_F). \tag{5}$$

Assuming a small signal amplitude compared to the DC voltage at nodes A and B and the Fermi potential Φ_F, the 2nd and 3rd order harmonics of the resistor current are

$$HD_2 \approx \frac{1}{2} \left| \frac{\gamma}{\left(4\sqrt{2\Phi_F + V_{B,DC}}\right)(V_C - V_{FB} - 2\Phi_F)} \right| V_{AB}, \tag{6}$$

$$HD_3 \approx \frac{1}{96} \left| \frac{\gamma}{(2\Phi_F + V_{B,DC})^{\frac{3}{2}} (V_C - V_{FB} - 2\Phi_F)} \right| V_{AB}^2 \tag{7}$$

where $V_{B,DC}$ is the DC voltage on node B, which is assumed to be the lower resistor terminal voltage. Equation (6) shows that the 2nd order harmonic will decrease for 12 dB while the 3rd order harmonic is the same as for a single MOS resistor. Since the 3rd order harmonic is negligibly small compared to 2nd order harmonic, the structure provides a significant linearity improvement compared to a single MOS transistor in triode region [15].

The ACR noise characteristic is mainly defined by the noise spectral density of the MOS transistors in triode region, assuming zero drain-source voltage,

$$\overline{i_{n,d}^2} = 4kTK_p \frac{W}{L}(V_{GS} - V_{FB} - 2\Phi_F)df \tag{8}$$

where T is the absolute temperature and k is Boltzmann's constant. The equation shows that the ACR noise is the same as for a passive resistor with the same resistance value. Since we are targeting high frequency RF applications, the flicker noise can be neglected. In addition the transistor gate resistance also generates thermal noise, but this is only a minor contribution and can be neglected for small transistor W/L ratios.

3.1 Active Resistor Implementation

The target LNA gain is continuously tunable from about 2 dB up to 20 dB, which requires an ACR resistor tuning range from about 30 Ω to 600 Ω. The floating gate ACR structure from Fig. 2 enables a tuning range of only 12 dB, which does not cover this specification. The proposed ACR circuit is a modified version of the basic floating gate implementation. To increase the tuning range, 3 ACR slices are connected in parallel, enabled by switches S_1, S_2 as shown in Fig. 3. For highest resistance value, Slice1 (PMOS transistor M_1) is enabled with the external control voltage V_{C1} applied to the gate of transistor M_1 only. To reduce the resistance, V_{C1} is decreased from V_{dd} down to the minimum control voltage of 0 V. To further reduce the resistance with a monotonic tuning behavior, Slice1 is kept at the minimum resistance value with lowest V_{C1} by permanently connecting the gate of transistor M_1 to 0 V, while Slice2 (PMOS transistor M_2) is enabled with a maximum control voltage V_{C1} (highest resistance) in parallel to Slice1. Now the resistance of Slice2 can be reduced from almost infinity to a low value. The same procedure is applied for Slice3 to reach the minimum possible resistance value. During the tuning procedure, the transistors might be biased in sub-threshold or weak inversion region, which means that the non-linearity cancelation will not work properly. By careful transistor dimensioning of each slice, a linearity degradation can be almost avoided. A higher number of slices would lead to better linearity over the whole resistance range but increases the complexity for switches and control logic and therefore degrades the overall speed performance.

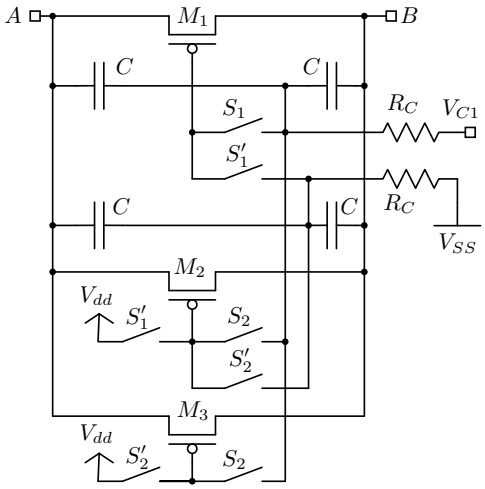


Fig. 3. Active resistor implementation with 3 parallel slices to increase tuning range. The slices are enabled via switches S_1, S_2 and the resistance is controlled by an analog control voltage V_{C1}, tunable between 0 V and V_{dd}.

The active resistor structure was implemented and fabricated in a 65 nm CMOS technology. The layout and chip photograph is shown in Fig. 4. The ACR has an area of 39 μm x 37 μm which is about 50 % larger compared to a switchable passive poly resistor array with only 5 programmable values in the same resistance range. For a higher number of resistance values, the proposed ACR has significant advantages with respect to area as well as speed performance.

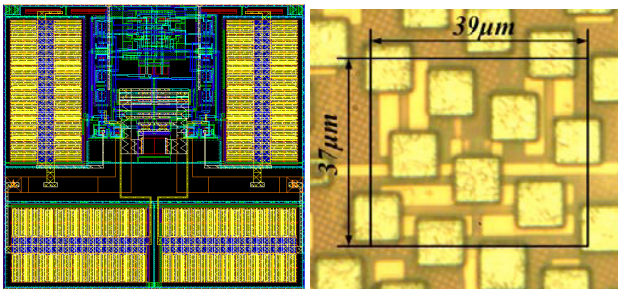


Fig. 4. Active resistor layout (left) and photograph (right).

The active resistor high frequency noise was verified by simulation and compared to a standard poly resistor with the same value at a frequency of 1 GHz. The comparison for different resistance values is shown in Tab. 1. The noise performance of the proposed ACR is only 2 % worse compared to a poly resistor for highest resistor value. The highest noise degradation is 9.4 % which happens when the 3rd ACR slice slightly enters the weak inversion region. The simulated ACR bandwidth is 6 GHz for the highest resistor value.

$R\,(\Omega)$	Noise ACR $(\mathrm{nV}/\sqrt{\mathrm{Hz}})$	Noise Poly $(\mathrm{nV}/\sqrt{\mathrm{Hz}})$	$\frac{\overline{v_{ACR}^2}}{\overline{v_{poly}^2}}$
631	3.30	3.24	1.019
406	2.75	2.60	1.058
152	1.74	1.59	1.094
37	0.846	0.79	1.071

Tab. 1. Noise comparison of proposed ACR resistor and Poly resistor at 1 GHz.

A linearity comparison between the ACR and a standard MOS transistor with the same resistance value shows that the ACR 2nd order distortion (HD2) is about 18 dB lower compared to a simple MOS resistor, while the 3rd order distortion (HD3) is approximately the same which fits well to the analysis in Equation 6 and 7. An ACR linearity measurement for a resistance value of 600 Ω is shown in Fig. 5. The 2nd and 3rd order harmonic distortions are shown in dependence on the RMS input voltage v_{in}. For the measurement a low signal frequency of 30 MHz was necessary, since the resistor pins are not 50 Ω impedance matched and the bonding-pad parasitic capacitances are limiting the speed for high resistor values. For small input signals, the measured HD3 reaches the spectrum analyzer noise floor.

Overall the simulated and measured ACR performance shows a high tuning range with a good noise and linearity performance, which makes the proposed active resistor a suitable solution for tunable LNA implementations.

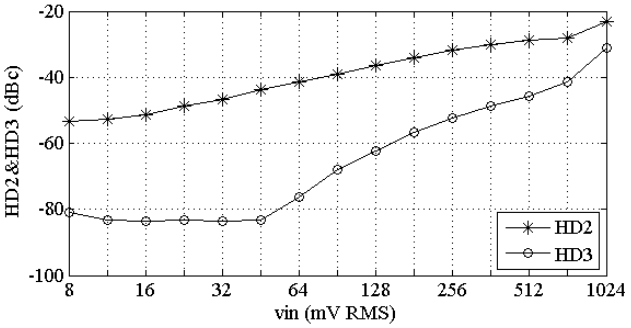


Fig. 5. Measurement results of 2nd order (HD2) and 3rd order (HD3) harmonic distortion for active resistor (ACR) in dependence on the signal level.

4. Proposed LNA Implementation

The proposed LNA is implemented as inductive source degeneration amplifier, due to an overall good noise and linearity performance with a low power consumption. Also the realization of gain and band tuning can be achieved with reasonably low circuit effort. A disadvantage of the source degeneration concept compared to feedback based LNAs is the high area consumption of integrated inductors. Furthermore the amplifier is intrinsically narrow-band due to the resonant input impedance matching.

The proposed LNA shown in Fig. 6 is realized as two-stage amplifier. It is based on an inductive degenerated common-source amplifier M_1 with L_s in combination with the gate series inductor L_g to tune-out the gate-source capacitance C_{gs1} of transistor M_1 creating the required 50 Ω impedance matching. The capacitor C_x in parallel to C_{gs1} is used to realize simultaneously noise and impedance input matching [16].

The LNA specification requires a tunable narrow-band behavior which is programmable over a range of about

5 GHz to 6 GHz. This requirement is contra-dictionary to the resonant narrow-band input impedance matching. To solve this problem, the input matching network needs to be programmable by e.g. tuning the capacitor C_x. For proposed implementation the impedance matching over the 1 GHz band is reasonably good, due to the rather low-quality factor of inductor L_s. Therefore no additional tuning of C_x is included. Since the dominant noise contribution is coming from transistor M_1, the g_{M1} is increased. Also the gate series resistance of M_1 is a dominant factor. Therefore the transistor layout as well as the resistance (quality factor) of inductor L_g is optimized.

The second stage of the LNA is implemented as common-gate (M_2) - common-source (M_3) topology to realize the balun functionality as discussed in Section 2. The two transistors are dimensioned to perform cancelation of transistor M_2 thermal channel noise [4]. The L-C tank load (L_d-C_L) connected to the differential output provides a tunable bandpass characteristic from 4.9 GHz to 5.8 GHz using tunable MOS varactors. The 6 turns differential, center-tapped inductor has an inductance of 2.75 nH with a simulated Q of about 13 and is optimized for highest inductance to area ratio. The center-tapped inductor in this design also guarantees a good output voltage balance which is a typical problem for resistive load circuits optimized for noise cancelation.

Due to high quality factors of capacitors in the L-C tank load, the open-loop gain of the LNA can be calculated as

$$A_v = g_{m,eff} R_{L,fr} = Q_{in} g_{M1} 2\pi f_r L_d \left(Q_d + \frac{1}{Q_d} \right) \quad (9)$$

where L_d and Q_d are the inductance and the quality factor of the load inductor at the resonance frequency f_r. The resonance frequency is given by,

$$f_r = \frac{1}{2\pi\sqrt{L_d C_{load}}} \quad (10)$$

where C_{load} represents the equivalent LNA load capacitance which includes the parasitic drain capacitors from the two transistors M_2, M_3. Since the LNA has no strong narrow-band requirement, the inductor L_d was optimized to small area.

The g_{M2} and g_{M3} have only a minor impact on the overall amplifier gain and can therefore be optimized to small values, which reduces the power consumption. This is also supported by the high output common-mode voltage of the center-tapped inductive load, which also makes the amplifier suitable for low supply voltages of 1.2 V. To further optimize the power consumption, a current re-use technique is implemented by inductor L_1 and C_P [10] which blocks the AC-signal to the source of transistor M_2, but enables the DC-current of both transistors M_2 and M_3 flowing through the input transistor M_1. For the amplifier a distortion cancelation together with optimization of the bias point for each transistor in the amplification path is employed. The devices are biased at the minimum 3rd - order parameter operational point [4], while threshold variations are compensated via bias generation.

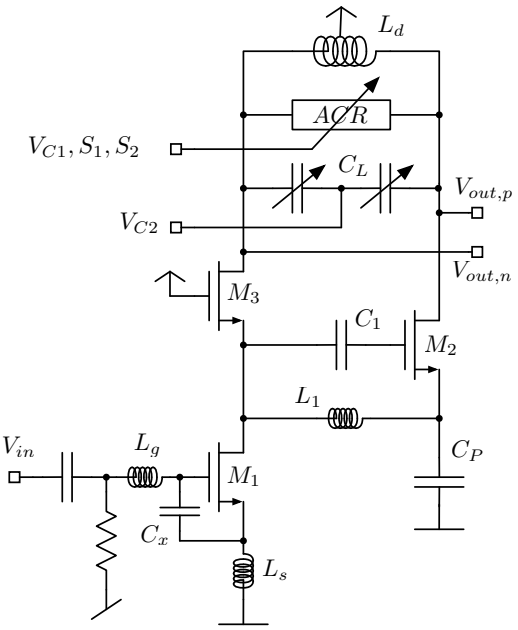


Fig. 6. LNA with tunable gain, where V_{C1} is the gain tuning control voltage for the active resistor (ACR), S_1, S_2 are digital gain control signals and V_{C2} is the control voltage for band setting

To realize a continuously tunable LNA gain, the proposed ACR structure presented in Section 3 is connected in parallel to the LNA L-C tank load. The ACR resistance is degrading the Q-factor for lower gains which is resulting in a LNA gain tuning.

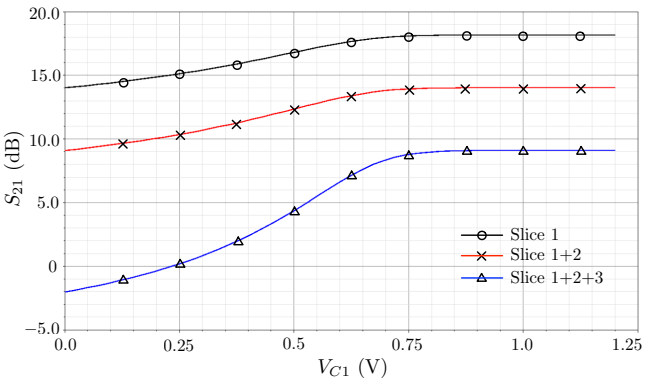


Fig. 7. Simulated small-signal gain (S_{21}) in dependence on the gain control voltage V_{C1} for the 3 slices.

The maximum LNA gain is defined by the L-C tank load, with the highest ACR resistance value (all transistors M_1, M_2 and M_3 are turned off).

In the following section simulation results of the proposed LNA circuit are presented. The LNA is realized in a low-power 65 nm CMOS technology. All results are based on ideal circuit simulations. The most important layout parasitics for metal wiring of sensitive nodes and parasitics for ESD protection and pads are estimated and manually included. The simulation of the gain tuning behavior is presented in Fig. 7. It shows the small-signal gain S_{21} in dependence on the gain control voltage V_{C1} for all three slices.

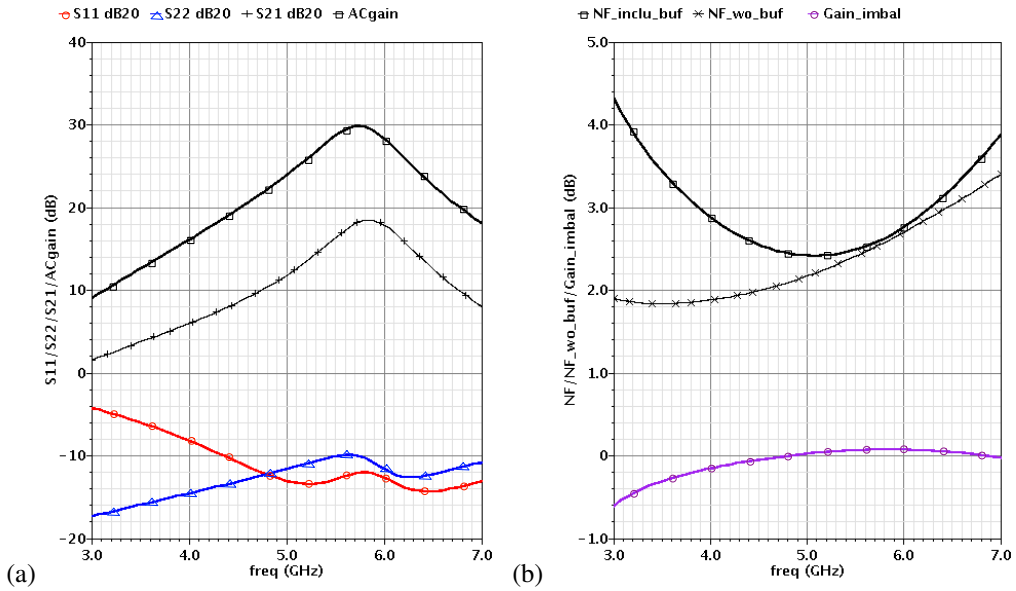


Fig. 8. Simulated s-parameters S_{21}, S_{11}, S_{22} (a), noise figure NF and gain imbalance (b) for highest gain and band settings. The measurement buffer loss is de-embedded for S_{21} and NF.

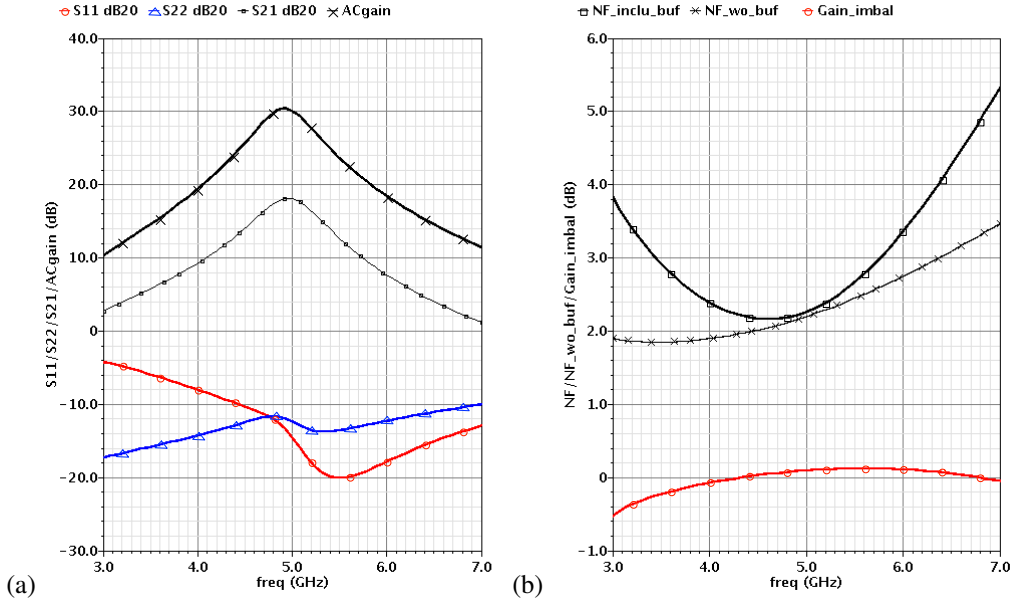


Fig. 9. Simulated s-parameters S_{21}, S_{11}, S_{22} (a), noise figure NF and gain imbalance (b) for highest gain and lowest band settings. The measurement buffer loss is de-embedded for S_{21} and NF.

The gain is continuously tunable from -2 dB to 18 dB with monotonic behavior at the slice switching point. The tuning gap between two slices is below 0.3 % and should be therefore no problem for applications. The simulated gain includes a measurement buffer which introduces a gain loss of about 10 dB. The simulation results of s-parameters S_{21}, S_{11}, S_{22}, the noise figure NF and the gain imbalance for the highest band and highest gain settings are shown in Fig. 8. The same simulations for the lowest band setting are shown in Fig. 9. The simulated gain with de-embedded measurement buffer loss reaches 30 dB. The band is tunable between a maximum frequency of 5.8 GHz and a minimum frequency of 4.9 GHz. The simulated NF for highest gain is 2.7 dB at 5.8 GHz and 2.1 dB at 4.9 GHz band setting. The gain imbalance from the single-ended input to the differential outputs is below 0.1 dB.

5. Measurement Results

The proposed LNA including the ACR structure has been implemented in 65 nm CMOS technology. The LNA circuit is using a single core-supply voltage of 1.2 V. For measurement, a source follower buffer is included to the LNA output. A chip photograph detail of the LNA is shown in Fig. 10. The active LNA area is 0.16 mm^2 including measurement buffer. For lab measurements the LNA chip was directly bonded on a FR4 evaluation board.

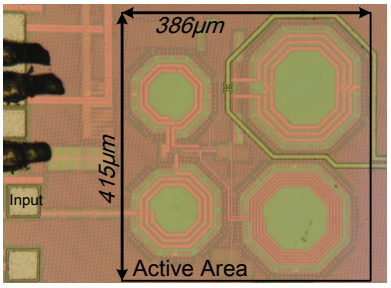


Fig. 10. LNA chip photograph detail.

Fig. 11 shows the measured LNA small-signal voltage gain in dependence on the control voltage V_{C1} for different slice enable settings. The gain is continuously tunable from about 2 dB up to 20 dB with a monotonic behavior at slice switching. The intrinsic LNA gain was extracted by de-embedding the measurement buffer loss from the measured gain data.

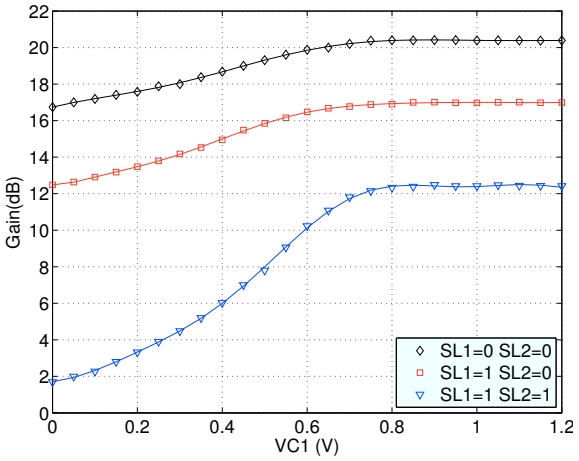


Fig. 11. Measured LNA gain tuning characteristics in dependence on control voltage V_{C1} and ACR slice enable settings.

The s-parameters S_{21} and S_{11} for different band-settings at the highest gain setting are shown in Fig. 12 (a). The band can be tuned from a frequency of 4.7 GHz up to a maximum of 5.6 GHz, which mainly covers the upcoming 801.11ac WLAN standard. Both measured LNA gain and intrinsic LNA gain with de-embedded buffer loss is shown in the figure. Although the gain setting was fixed for this measurement, the maximum gain is decreasing with a decreasing frequency band. This can be explained by a de-centered input impedance matching network, which can also be seen in the S_{11} measurements, compared to the simulations in Fig. 8 and 9. The modeling of the ESD, pad parasitics and bond-wires during the design phase was not accurate enough.

The measured s-parameters S_{21} and S_{11} for different gain settings at the highest frequency band are shown in Fig. 12 (b). The gain can be tuned from a maximum of about 20 dB down to 2 dB with de-embedded measurement buffer loss. Compared to the simulation results, the measured gain values are about 10 dB smaller. We expect a coupling of the load inductor with neighboring inductors or bond-wires and a smaller quality factor due to the high layout density which decreases the maximum gain compared to the simulations. Overall we were able to demonstrate the expected gain and frequency tuning behavior.

The IIP3 linearity measurements at the highest band setting (5.6 GHz / 5.604 GHz) and for the highest gain are shown in Fig. 13 (a), while the highest band and lowest gain setting is shown in Fig. 13 (b). The input power for 3rd-order interpolation was selected for worst case IIP3. The measured IIP3 for highest gain is -8 dBm while it is increasing to +4.6 dBm for the lowest gain. The integrated measurement buffer loss is de-embedded in the presented IIP3 measurements. Considering the circuit flexibility and the low supply voltage of the CMOS process, the measured linearity values are quite acceptable.

The LNA noise figure NF could not be verified by measurements due to limitations of the measurement equipment. The LNA power consumption is 10 mW.

6. Conclusion

An inductive source degeneration based balun LNA with L-C tank load including a tunable band-pass characteristic from 4.7 GHz to 5.6 GHz is presented. In addition the LNA also provides a continuously tunable gain from 2 dB up to 20 dB based an active resistor implementation. The LNA shows a very good IIP3 linearity of -8 dBm for highest gain and band setting while the linearity is increasing to +4.6 dBm at the lowest gain. The simulated LNA noise figure NF is 2.1 dB and 2.7 dB for the lowest and highest gain respectively. The LNA has a low power consumption of 10 mW with a die area of 0.16 mm^2.

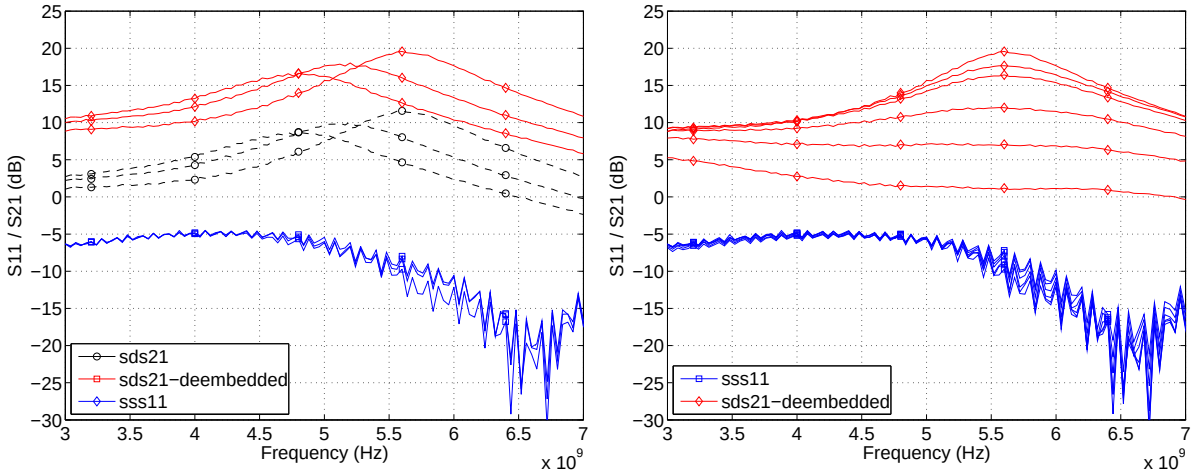
With the combination of continuous gain- and band-tuning, the proposed LNA enables a unique flexibility for future multi-standard, multi-band wireless receiver concepts. A performance comparison with state-of-art publications is listed in Tab. 2. Our proposed design has the highest flexibility with respect to band and gain tuning, with a comparable linearity, noise, and power performance.

Acknowledgements

This work was supported in part by ENIAC JU Project ARTEMOS project number 270683-2. The authors would like to thank Lantiq Austria for assistance and support in testchip fabrication.

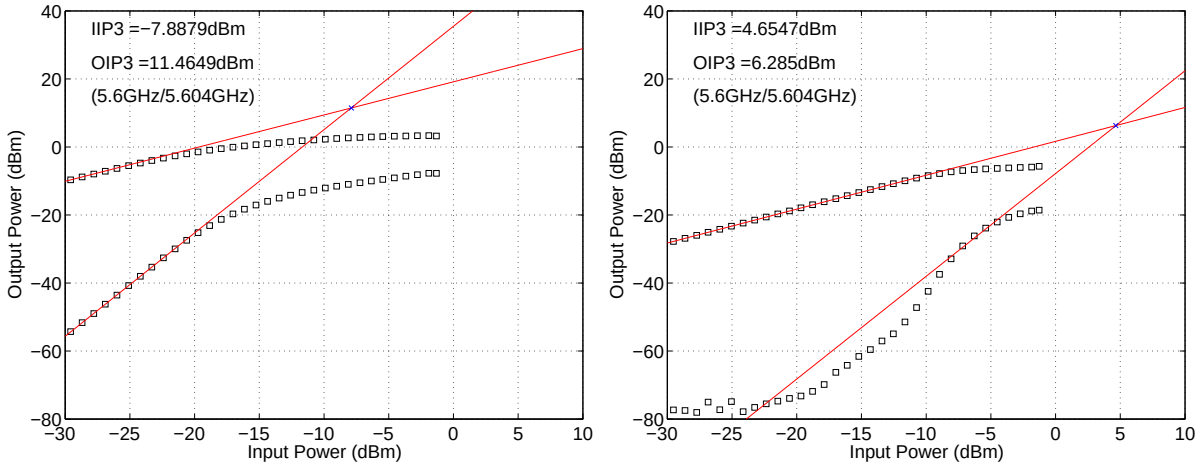
References

[1] BRUCCOLERI, F., KLUMPERINK, E. A. M., NAUTA, B. Wide-band CMOS low-noise amplifier exploiting thermal noise canceling. *IEEE Journal of Solid State Circuits*, 2004, vol. 39, no. 2, p. 275 - 282.



(a) (b)

Fig. 12. Measured s-parameters S_{21} and S_{11} for different band-settings at the highest gain (a) and for different gain-settings at the highest frequency band (b). The measurement buffer loss is de-embedded.



(a) (b)

Fig. 13. Measured LNA IIP3 for the highest gain and highest band setting (a) and for the lowest gain and highest band setting (b). The measurement buffer loss is de-embedded.

[2] IM, D. NAM, I., LEE, K. A. CMOS active feedback balun-LNA with high IIP2 for wideband digital TV receivers. *IEEE Transactions on Microwave Theory and Techniques*, 2010, vol. 58, no. 12, p. 3566 - 3579.

[3] PERUMANA, B. G., ZHAN, J. C., TAYLOR, S. S., CARLTON, B. R., LASKAR, J. Resistive-feedback CMOS low-noise amplifiers for multiband applications. *IEEE Transactions on Microwave Theory and Techniques*, 2008, vol. 56, no. 5, p. 1218 - 1225.

[4] BLAAKMEER, S. C., KLUMPERINK, E. A. M., LEENAERTS, D. M. W., NAUTA, B. Wideband balun-LNA with simutaneous output balancing, noise-canceling and distortion-canceling. *IEEE Journal of Solid-State Circuits*, 2008, vol. 43, no. 6, p. 1341 - 1350.

[5] WANG, X., AICHHOLZER, W., STURM, J. A 0.1 – 4 GHz resistive feedback LNA with feedforward noise and distortion cancelation. In *Proceedings of IEEE European Solid-State Circuits Conference (ESSCIRC)*. 2010, p. 406 - 409.

[6] ROBERT, S., ABED-MERAIM, O., LO COCO, L. Wide-band variable-gain LNA in 65 nm CMOS with inverter based amplifier for multi-tuners cable TV reception. In *Proceedings of IEEE ESSCIRC*. Athens (Greece), 2009, p. 104 - 107.

[7] GEIS, A., ROLAINY, Y., VANDERSTEENY, G., CRANINCKX, J. A 0.045 mm^2 0.1 – 6GHz reconfigurable multi-band, multi-gain LNA for SDR. In *IEEE RFIC Symposium Digest*. 2011.

[8] AZUMA, S., KAWAMURA, H., KAWAMA, S., TOYOYAMA, S., HASEGAWA, T., KAGOSHIMA, K., KOUTANI, M., KIJIMA, H., SAKUNO, K. IIZUKA, K. A Digital terrestrial television (ISDB-T) tuner for mobile applications. In *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*. 2004, vol. 1, p. 278 - 528.

[9] ZHANG, F., KINGET, P. R. Low-power programmable gain CMOS distributed LNA, I. *EEE Journal of Solid State Circuits*, 2006, vol. 41, no. 6, p. 1333 - 1343.

[10] JI, Y., WANG, C., LIU, J., LIAO, H. 1.8 dB NF 3.6 mW CMOS active balun low noise amplifier for GPS. *Electronics Letters*, 2010, vol. 46, no. 3, p. 251 - 252.

[11] BELOSTOTSKI, L., HASLETT, J. W. Sub-0.2 dB noise figure wide-band room-temperature CMOS LNA with non-50Ω signal-source impedance. *IEEE Journal of Solid State Circuits*, 2007, vol. 42, no. 11, p. 2492 - 2502.

References	Band (GHz)	Gain (dB)	NF (dB)^A	IIP3 (dBm)^A	Power (mW)	Technology	Variable gain
This work	4.7 ... 5.6	2 ... 20	2.7	-8	16	65 nm	Y
[2]	TV (< 1 GHz)	3 ... 18	2.5 ... 3	-0.5	30	0.13 μm	Y
[3]	4 ... 8	24.4	2 ... 2.4	-2.9	9.2	90 nm	N
[4]	0.2 ... 5.2	15.6	<3.5	>0	14	65 nm	N
[6]	TV (< 1 GHz)	3 ... 15	5.7	+15.2^B	65	65 nm	Y
[9]	0.04 ... 7	-10 ... 8	4.2	+4.2	9	180 nm	Y
[17]	TV (< 1 GHz)	15	4.2	2.6	10	0.18 μm	N
[18]	0.2 ... 3.2	15.5	1.76	-9	25	90 nm	N
[19]	2/5	23/20	2.1	-16/-10	3.8	0.13 μm	N
[20]	0.05 ... 2	0 ... 24	2.5	-8	12	65 nm	Y

^{A} ... highest gain ^{B} ... lowest gain

Tab. 2. LNA performance comparison.

[12] KO, J., KIM, J., CHO, S., LEE, K. A 19-mW 2.6-mm^2 L1/L2 dual band CMOS GPS receiver. *IEEE Journal of Solid-State Circuits*, 2005, vol. 40, no. 7, p. 1414 - 1425.

[13] TORRALBA, A., LUJIAN-MARTINEZ, C., CARAVAJAL, R. G., GALAN, J., PENNISI, M., RAMIREZ-ANGULO, J., LOPEZ-MARTIN, A. Tunable linear MOS resistors using quasi-floating-gate techniques. *IEEE Transactions on Circuits and Systems II*, 2009, vol. 56, no. 1, p. 41 - 45.

[14] XIANG, X., STURM, J. Tunable linear MOS resistor for RF applications. In *IEEE 12th Topical Meeting on Silicon Monolithic Intergrated Circuits in RF Systems (SiRF).* Santa Clara (CA, USA), 2012, p. 37 - 40.

[15] WAMBACQ, P., SANSEN, W. *Distortion Analysis of Analog Integrated Circuits.* Dordrecht (the Netherlands): Kluwer Academic Publishers, 1998.

[16] NGUYEN, T.-K., SU, Y.-M., LEE, S.-G. A power-constrained simultaneous noise and input matching low noise amplifier design technique. In *Proceedings of International Symposium on Circuits and Systems (ISCAS)*. 2004, p. 281 - 284.

[17] HAN, K., ZOU, L., LIAO, Y., MIN, H., TANG, Z. A wideband CMOS variable gain low noise amplifier based on single-to-differential stage for TV tuner applications. *IEEE Solid-State Circuits Conference (ASSCC)*. 2008, p. 457 - 460.

[18] CHANG, T., CHEN, J., RIGGE, L. A., LIN, J. ESD-protected wideband CMOS LNAs using modified resistive feedback techniques with chip-on-board packaging. *IEEE Transactions on Microwave Theory and Techniques*, 2008, vol. 56, no. 8, p. 1817 - 1826.

[19] BORREMANS, J., WAMBACQ, P., SOENS, C., ROLAIN, Y., KUIJK, M. Low-area active-feedback low-noise amplifier design in scaled digital CMOS. *IEEE Journal of Solid State Circuits*, 2008, vol. 43, no. 11, p. 2422 - 2433.

[20] STURM, J., XIANG, X., PRETL, H. A 65 nm CMOS wide-band LNA with continuously tunable gain from 0 dB to 24 dB. In *Proceedings of International Symposium on Circuits and Systems (ISCAS).* 2013, p. 733 - 736.

About Authors...

Johannes STURM was born in Villach, Austria. He received the M.Sc. degree in Physics from the Graz University of Technology in 1995 and his Ph.D. degree from Vienna University of Technology in 2006 respectively. In 1996 he joined the Siemens-Semiconductor-Group and later Infineon Technologies in Villach, Austria, working as analog designer, concept engineer and project leader for analog, mixed signal ASIC projects in the field of optical sensor ICs and high-speed CMOS circuits. Since 2006 he has been employed as Professor for analog circuit design at the Carinthia University of Applied Sciences, Villach, Austria. His research interests are in the field of CMOS RF integrated circuits and integrated sensor design. He has been responsible for several national and European funded research projects and holds 7 patents in the field of microelectronics.

Marcus GROINIG was born in Villach in 1983. He received the M.Sc. degree from Graz University of Technology in Electrical Engineering and the B.Sc. in Biomedical Engineering. After working as an R&D engineer in hyperspectral near-infrared camerasystems in Graz he joined the Carinthia University of Applied Sciences in 2013 as RF research assistant.

Xinbo XIANG received the B.Sc. degree in Information Engineering from Chengdu University of Technoly in Chengdu, China. He joined the Carinthia University of Applied Sciences in Villach, Austria, received his Master degree in 2010 and continued working as a researcher for RF circuit design. Currently he is working in an RF design group at Lantiq A GmbH in Villach. His current research interests are in the area of radio-frequency integrated receivers.