High Gain Amplifier with Enhanced Cascoded Compensation

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Abstract. *A two-stage CMOS operational amplifier with both, gain-boosting and indirect current feedback frequency compensation performed by means of regulated cascode amplifiers, is presented. By using quasi-floating-gate transistors (QFGT) the supply requirements, the number of capacitors and the size of the compensation capacitors respect to other Miller schemes are reduced. A prototype was fabricated using a 0.5 μm technology, resulting, for a load of 45 pF and supply voltage of ±1.65 V, in open-loop-gain of 129 dB, 23 MHz of gain-bandwidth product, 60º phase margin, 675 μW power consumption and 1% settling time of 28 ns.*

Keywords

Gain boosting, frequency compensation, regulated cascode, quasi-floating gate transistors.

1. Introduction

The voltage amplifier is one of the most important functional blocks in analog signal processing. It is widely used as basic building block towards the design of many complex functions, for instance: high-order filters, analog to digital (A/D) and digital to analog (D/A) converters, to name a few. It is well known that the performance of a voltage amplifier is related to some established characteristics, such as: gain-bandwidth product, phase margin, and DC open loop gain [1]. Unfortunately, the severe degradation of the gain when modern technologies are employed is a limiting factor for the accuracy and resolution in many applications [2]. It is a consequence of large channel length reduction and shrinking of power supplies. Besides, the intrinsic gain, the signal headroom and the threshold voltage are also affected [3], hindering the design of high-gain amplifiers by traditional gain enhancement techniques. For instance, cascode amplifiers have been commonly used for high frequency applications because of their single parasitic pole. However, cascode transistors require large power supply and present limited output swing. Another common approach to boost the voltage gain is by cascading gain stages. This strategy allows to achieve a larger signal swing at the output node, but requires utilization of complex and difficult-to-design nested compensation networks to guarantee closed-loop stability [4, 5, 6]. Also, due to the reduction of the transistor intrinsic gain, the overall gain for two-stages could be not enough for many applications [7]. Other strategy is the use of regulated cascode stages (gain-boosted stages) [8], which employ local feedback to increase the output resistance and the gain of a cascode amplifier without compromising stability. Unfortunately, the required power supply increases and the output swing decreases, as in the case of cascode structures. It was proposed in [2] the use of floating-gate transistors to reduce the power supply requirements of gain-boosted amplifiers, but the number of required capacitors can be prohibitive since silicon area reduction is a crucial trend in modern applications. Having identified these three important issues: gain reduction, complex frequency compensation and large supply requirements, this paper proposes an alternative that combines a gain-boosted telescopic amplifier with reduced supply requirements and a second gain stage with current feedback frequency compensation. By using quasi-floating-gate transistors (QFGT) the number of capacitors is reduced by 50 % with respect to the amplifier proposed in [2], while the current feedback improves the settling time.

2. Gain Boosted Amplifier with QFGT

Unlike the conventional gain-boosted telescopic amplifier, the proposed topology, shown in Fig. 1, incorporates a floating battery F_B of value V_{bat} in order to reduce the required voltage at node Y to maintain M_1, M_2 and M_3 operating in saturation mode. Assuming I_{b1} and I_{b2} with infinite output resistance, the common source amplifier M_3-I_{b2} boosts the effective gain of the cascading transistor M_2 by a factor $g_{m3}r_{ds3}$, where g_m denotes transconductance and r_{ds}

$$\begin{bmatrix} 2g_m^2 r_o + s(C_1+C_C) & 0 & 0 & -sC_C \\ -g_m^2 r_o & \frac{1}{g_m^2 r_o^3} + sC_2 & -g_m^2 r_o & 0 \\ 0 & 0 & 2g_m^2 r_o + s(C_1+C_C) & -sC_C \\ -sC_C & g_{m10} & -sC_C & \frac{1}{r_o} + s(C_L+2C_C) \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_{out} \end{bmatrix} = \begin{bmatrix} -g_m V_{in} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{3}$$

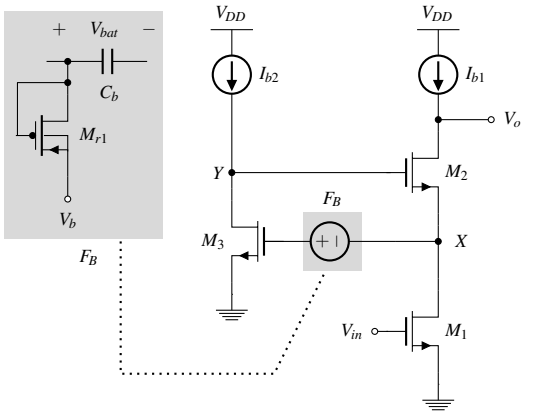

Fig. 1. Floating battery gain-boosted telescopic amplifier (FBGBTA).

drain-to-source resistance. Besides, the resistance at node V_o achieve a high value $R_o \approx (g_{m3} r_{ds3})(g_{m2} r_{ds2}) r_{ds1}$ and the corresponding voltage gain from V_{in} to V_{out}, A_V, becomes

$$A_V \approx -g_{m1} g_{m2} g_{m3} r_{ds1} r_{ds2} r_{ds3}. \tag{1}$$

Without F_B, the minimum supply voltage requirements of the amplifier is the sum of the supply voltage requirements of the cascode current source I_{b2} and the gate to source voltages of M_2 and M_3, i.e $V_{DD}^{min} > V_{sat,Ib2} + 2V_{THn} + V_{sat,m2} + V_{sat,m3} \approx 4V_{sat} + 2V_{THn}$, where V_{sat} and V_{THn} are the overdrive and threshold voltages, respectively. With F_B, the minimum required supply voltage is reduced to $V_{DD}^{min} > 4V_{sat} + 2V_{THn} - V_{bat}$. This floating battery is implemented by means of a quasi-floating gate transistor conformed by M_{r1} and C_b [9], as illustrated in Fig. 1. Here, M_{rl} is connected as an inverted P-N junction, i.e, as a quasi-infinite resistor in the range of Gohms used to weakly connect the gate of M_3 to the bias voltage V_b [9]. As a result, the drain to source voltage of M_1 is not dependent on the gate to source voltage of M_3, resulting V_{DS1}=V_{DS3}-$V_{sat,m2}$-V_{THn}. Therefore, V_b can be chosen such that V_{DS1} is close to its minimum value $V_{DS1}^{min} = V_{sat,m1}$. In this way, the range of negative output signal swing increases, because M_3 stills remains in saturation when the output voltage is below V_{GS3}. If I_{b1} is a cascode current source, the amplifier output swing is given by V_{out}^{swing}=V_{DD}-$V_{sat,m1}$-$V_{sat,m2}$-$2V_{sat}$. Also, the gain boosting produces a large reduction of the impedance at node X which will be used in the next section to establish the frequency compensation. This impedance can be expressed as

$$Z_X = \frac{1}{(g_{m3} r_{ds3} + 1) g_{m2} + \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}}} \approx \frac{1}{g_{m2} g_{m3} r_{ds3}}. \tag{2}$$

3. High-Gain Two-Stage Amplifier

Figure 2 illustrates the proposed high-gain two-stage amplifier. The first stage is a differential realization of a Floating Battery Gain-Boosted Telescopic Amplifier (FBGBTA). In this amplifier, M_b and V_b establish a tail current of value $2I_b$, M_1 and M_2 conform the differential pair and transistors M_3 to M_8 are used to implement the cascode active load. The effective gains of the cascode transistors M_3, M_4, M_7 and M_8 are boosted by a factor $g_m r_{ds}$ by means of the common source amplifiers M_{GB1}-I_b, M_{GB2}-I_b, M_{GB3}-I_b and M_{GB4}-I_b, respectively. As was explained in section 2, the voltage requirements of these gain boosting arrays are relaxed by means of the floating batteries F_B realized with transistors M_{rl} and capacitors C_b. The bias voltages V_{bn} and V_{bp} adjust the floating batteries to V_{bat_n} and V_{bat_p}. The second stage is a common source structure conformed by transistors M_9 and M_{10}. It has a maximum output swing given by V_{out}^{swing}=V_{DD}-$V_{sat,m9}$-$V_{sat,m10}$. C_L is the total load capacitance to be driven by the amplifier. Besides, the proposed frequency compensation array consists of two compensation capacitors C_C connected between the output node and two internal low impedance nodes of the first gain stage, labeled as node 1 and node 3. This compensation strategy is similar to the scheme reported in [4, 5]. The currents through the capacitors form indirect feedback currents that boost the non-dominant pole and the left half plane zero to higher frequencies, as will be analyzed in Section 4.

4. Small Signal Analysis

The small signal model of the proposed amplifier is depicted in Fig. 3. Here $R_1, R_2, R_3, R_L, C_1, C_2 (\approx C_{gs,10}), C_3$ and C_L denote the overall resistances and capacitances at nodes 1, 2, 3 and V_{out}, respectively. In order to simplify the analysis it is assumed that transistors M_1 to M_9 have transconductances g_m and drain-to-source resistances r_o, while transistor M_{10} has transconductance g_{m10} and drain-to-source resistance r_o. Besides, the gain boosting arrays are modeled as voltage controlled current sources with gain $g_m^2 r_o$. It is also considered $R_1 \approx R_3 \approx 1/(g_m^2 r_o)$, $R_2 \approx g_m^2 r_o^3$, $R_L \approx r_o$, and $C_1 \approx C_3$. Now, by performing a nodal analysis of this circuit, it is obtained the linear system (3) and by solving it the transfer function of the amplifier becomes

$$\frac{v_{out}}{v_{in}} = \frac{N(s)}{D(s)} \approx \frac{A_o(-n_2 s^2 - n_1 s + 1)}{d_3 s^3 + d_2 s^2 + d_1 s + 1} \tag{4}$$

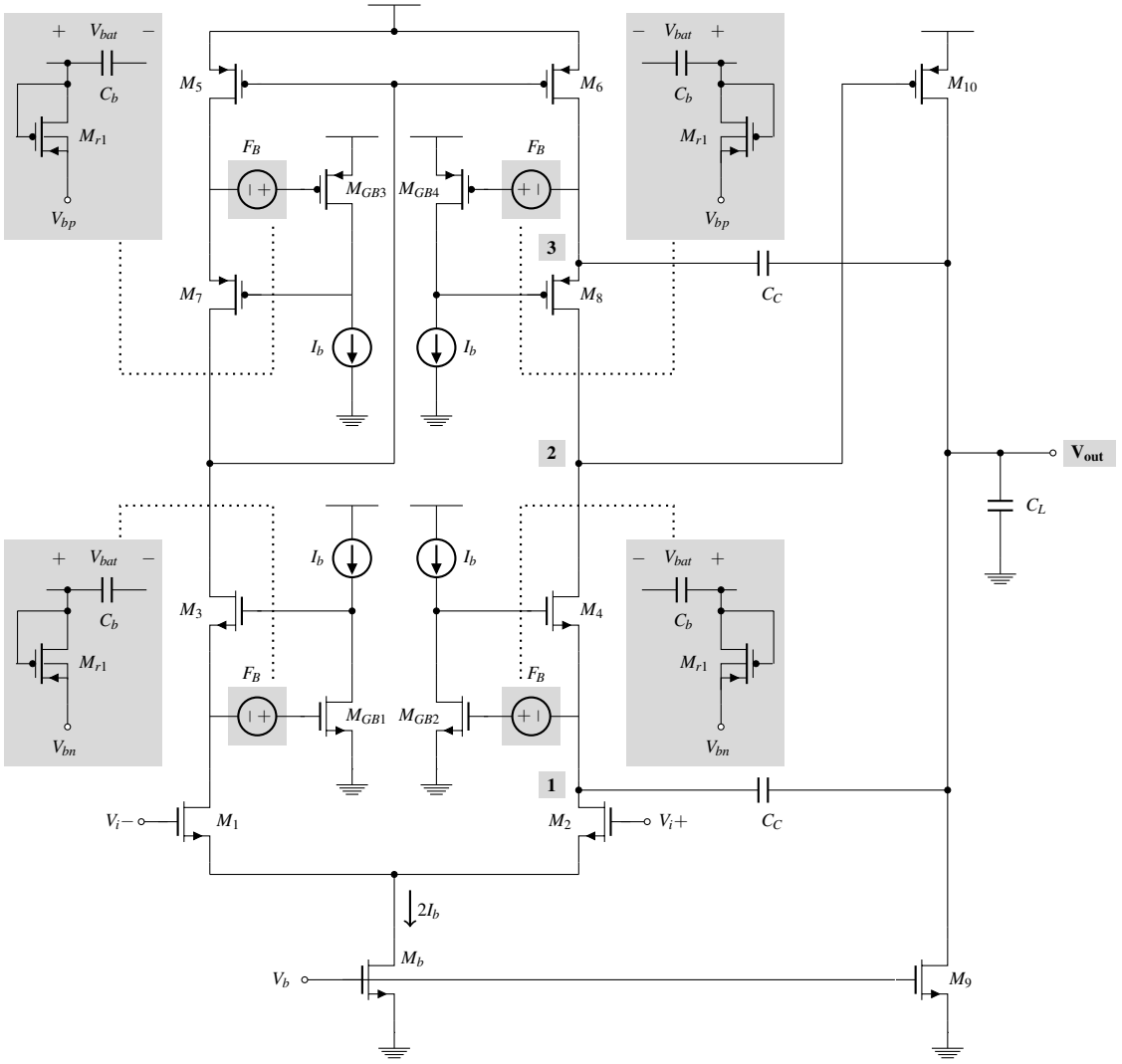

Fig. 2. Floating Battery Gain-Boosted Telescopic Amplifier (FBGBTA).

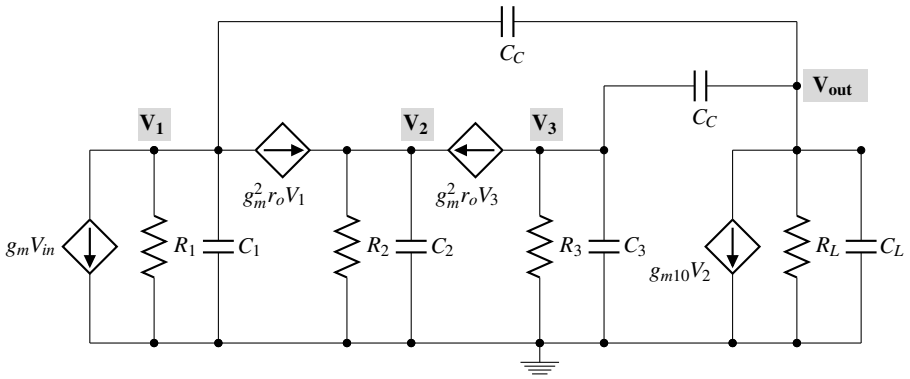

Fig. 3. Small signal model of the Two-Stage Amplifier.

with

$$A_o \approx \frac{1}{2} g_{m10} g_m^3 r_o^4, \quad (5)$$

$$n_1 \approx \frac{C_C}{g_{m10} g_m^4 r_o^4}, \quad (6)$$

$$n_2 \approx \frac{C_2 C_C}{g_{m10} g_m^2 r_o}, \quad (7)$$

$$d_1 \approx g_{m10} g_m^2 r_o^4 C_C, \quad (8)$$

$$d_2 \approx g_m^2 r_o^4 C_2 (C_L + 2C_C), \quad (9)$$

$$d_3 \approx \frac{1}{2} r_o^3 C_2 C_L C_C. \quad (10)$$

In this way, the amplifier presents three poles and two zeros. First, the effect of the poles will be analyzed. Then it will be demonstrated that the zeros have no effect in the phase margin. Considering that $d_3 s^3 << d_2 s^2 + d_1 s + 1$ at the frequencies of interest, the amplifier can be analyzed as a system with two poles. Assuming that the dominant pole s_{p1} and the non-dominant pole s_{p2} are separated from each other, one obtains

$$s_{p1} \approx \frac{-1}{d_1} = \frac{-1}{g_{m10} g_m^2 r_o^4 C_C}, \quad (11)$$

$$s_{p2} \approx \frac{-d_1}{d_2} = \frac{-g_{m10} C_C}{C_2 (C_L + 2C_C)}. \quad (12)$$

According to (11) and (12), to satisfy $s_{p1} << s_{p2}$ it is required that

$$g_{m10} g_m^2 r_o^4 C_C^2 \approx A^4 C_C^2 >> C_2 (C_L + 2C_C) \quad (13)$$

where $A = g_m r_o$ is the intrinsic gain of a transistor. This condition fulfills because typically $C_C^2 > C_2 (C_L + 2C_C)$ and $A >> 1$. Now, by combining (5) and (11) the gain-bandwidth product results in

$$f_{GBW} = \frac{1}{2} \frac{g_m}{C_C} \quad (14)$$

and f_{GBW} is similar to the obtained with conventional Miller compensation. Besides, it is well known that for a two-stage amplifier in which the frequency behavior can be assumed with a single non-dominant pole, the phase margin is expressed by [10],

$$M_\phi = 90^o - arctan\left(\frac{f_{GBW}}{s_{p2}}\right). \quad (15)$$

For instance, a phase margin of 60^o means a s_{p2}/f_{GBW} value of about 1.7. By combining (12) and (14) and by considering $C_L >> C_C$,

$$C_C = 0.92 \sqrt{\frac{g_m C_2 C_L}{g_{m10}}} \quad (16)$$

which represents a smaller capacitor C_C respect to the required with Miller compensation

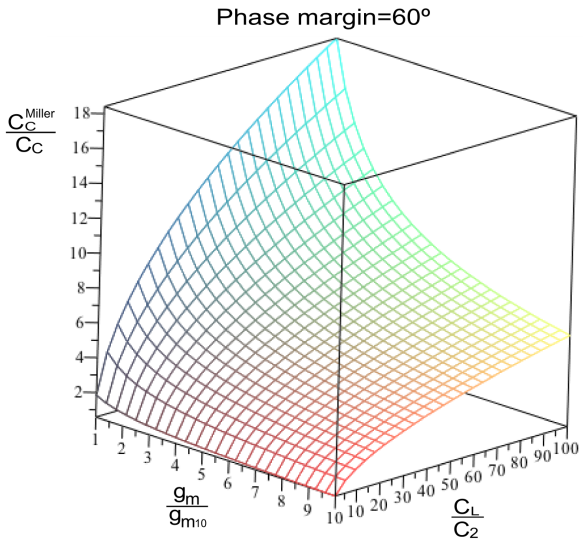

Fig. 4. Reduction of C_C respect Miller compensation.

$$C_C^{Miller} = 1.7 \frac{g_m}{g_{m10}} C_L. \quad (17)$$

Figure 4 depicts the dependence of C_C^{Miller}/C_C with respect to g_m/g_{m10} and C_L/C_2 for a phase margin of 60^o. It is obtained by comparing (16) and (17). As can be observed, the proposed frequency compensation reduce the size of the required capacitors, allowing an increase of the gain-bandwidth product and reducing the settling time respect to the Miller compensation.

The effect of the zeros over the frequency response is analyzed by solving $N(s) = 0$, where $N(s)$ was defined in (3). Here, it is concluded that the term $-n_1 s$ of $N(s)$ is negligible. Therefore, (3) can be simplified as

$$\frac{v_{out}}{v_{in}} = \frac{N(s)}{D(s)} \approx \frac{A_o (1 - n_2 s^2)}{d_3 s^3 + d_2 s^2 + d_1 s + 1} \quad (18)$$

with

$$z_{1,2} \approx \pm g_m \sqrt{\frac{g_{m10} r_o}{C_2 C_C}} \quad (19)$$

and the proposed frequency compensation produces two identical real zeros, one in the left half and the other one in the right half of the complex plane. In consequence, the phase effects of these zeros cancel each other out. Besides, the magnitude response of these zeros do not affect the stability because of $|z_{1,2}| > f_{GBW}$.

Design remarks: (i) Restrictions (13) and (16) must be satisfied in order to ensure stability with 60^o of phase margin. (ii) To reduce the voltage supply requirements, V_{bn} and V_{bp} must be chosen such that V_{DS,MGB_i} be close to their minimum values V_{sat,MGB_i}.

	Aspect ratios and values
$M_1 - M_4$	30 μm/0.6 μm
$M_5 - M_8$	157.5 μm/0.6 μm
$M_{GB1} - M_{GB2}$	60 μm/0.6 μm
$M_{GB3} - M_{GB4}$	126 μm/0.6 μm
M_{Rl}	1.5 μm/0.6 μm
M_B, M_9	62.4 μm/0.6 μm
M_{10}	315 μm/0.6 μm
V_{DD}	$\pm$1.65 V
I_b	50 μA
C_b, C_C, C_L	1 pF, 2.5 pF, 45 pF

Tab. 1. Aspect ratios of transistors and bias details.

Parameter	Calculated	Simulated	Measured
C_C	2.8 pF	2.5 pF	$--$
f_{GBW}	28.4 MHz	22 MHz	20 MHz
M_ϕ	54^o	60^o	59^o

Tab. 2. Calculated, simulated and measured parameters.

5. Results

A two-stage amplifier using the structure shown in Fig. 2 was simulated in HSPICE using BSIM4.6 level 49 models of a double-poly, three metal layers, 0.5 μm CMOS technology from ON-Semi foundry ($V_{TH_n} = 0.65$ V, $|V_{TH_p}| = 0.95$ V). The aspect ratio of the transistors and the bias of the circuit are detailed in Tab. 1. Dimensioning of the circuit was done considering the equations presented in Section 4 for $f_{GBW} = 28$ MHz and with $C_L = 45$ pF and $I_b = 50$ μA, resulting $g_m = 0.001$ A/V, $g_{m10} = 0.0024$ A/V, $C_2 = 0.52$ pF and $C_C = 2.8$ pF. For the simulations, a dual power supply of $V_{DD} = \pm 1.65$ V and a bias current of $I_b = 50$ μA were employed, while the values of the used capacitors were $C_b = 1$ pF, $C_L = 45$ pF and $C_C = 2.5$ pF (12.75 times lower than with Miller compensation). A comparison of the calculated, simulated and measured parameters C_C, f_{GBW} and M_ϕ is summarized in Tab. 2. According to the obtained results and despite the simplified small signal analysis, we conclude that the behavior of the amplifier follows the course anticipated in the synthesis of the circuit performed in Section 4.

Figure 5 shows the simulated input-output DC transfer characteristics for selected values of gain, where no variations of an offset of 3.7 μV were found. Figure 6 shows the open loop simulation of magnitude and phase of the proposed amplifier, and its comparison with other cascode conventional compensated structure [11] and the conventional Miller compensated two-stage with telescopic input stage amplifier. Because of the impedance reduction at nodes 1 and 3 used in the indirect compensation scheme, a lower degradation is observed in the phase margin when compared with other previously reported amplifiers. The proposed amplifier presents a DC gain of 129 dB, unity-gain frequency of 22 MHz and phase margin of 60^o.

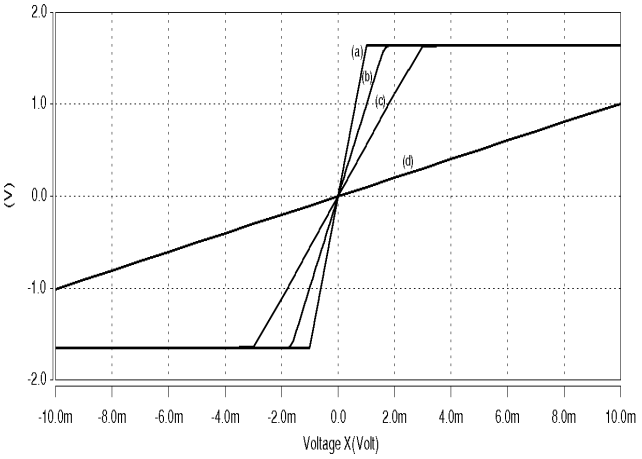

Fig. 5. Input Output DC transfer characteristic for a) 74 dB Gain, b) 60 dB Gain, c) 54.9 dB and d) 40 dB

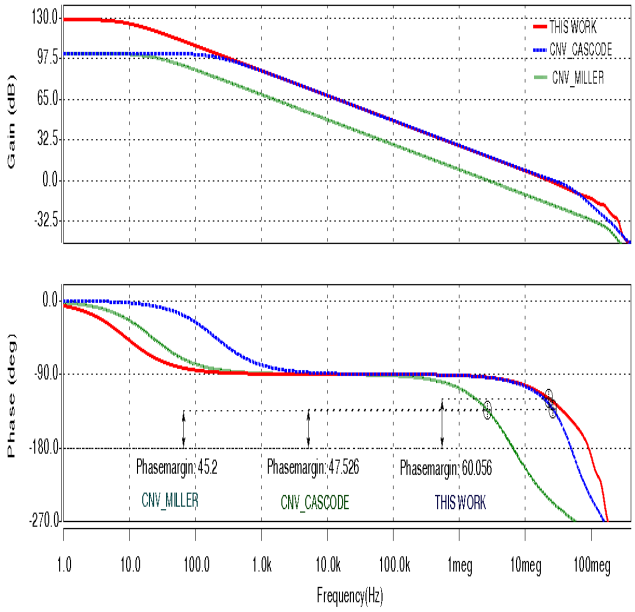

Fig. 6. Frequency response of Proposed, Conventional Cascode and conventional Miller two stage amplifiers with $C_L =$ 45 pF.

The simulated step response of the proposed amplifier in non-inverting unity-gain configuration is shown in Fig. 7. Here, an input step of 100 mV with 1 ns rise time was used. The amplifier presents a settling-time of 28 ns which is 439 ns lower than with the compensated Miller and 19 ns lower than with the compensated conventional cascode.

To estimate the sensitivity to tolerances of the proposed amplifier, a Monte Carlo simulation for 100 samples was performed using the Pelgrom's model [12] and maximum tolerances of 5% for capacitors. Figure 8 shows a f_{GBW} mean value of 22.9 MHz with a standard deviation of 189 kHz, while M_ϕ presents a mean value of 60^o with a standard deviation lower than 1^o. A summary of the simulation results of the three compared amplifiers and a two-stage OPAMP with Miller compensation [13] is shown in Tab. 3.

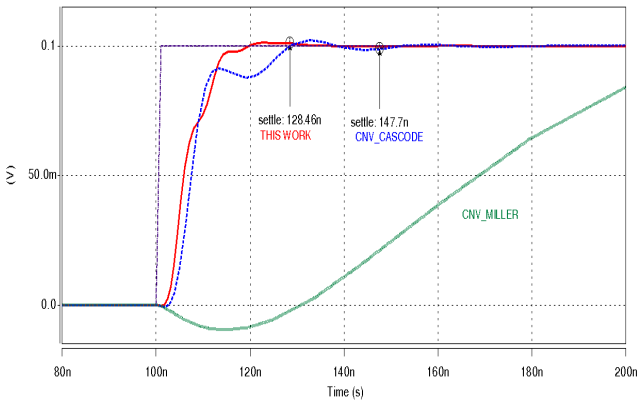

Fig. 7. Settling time simulation results.

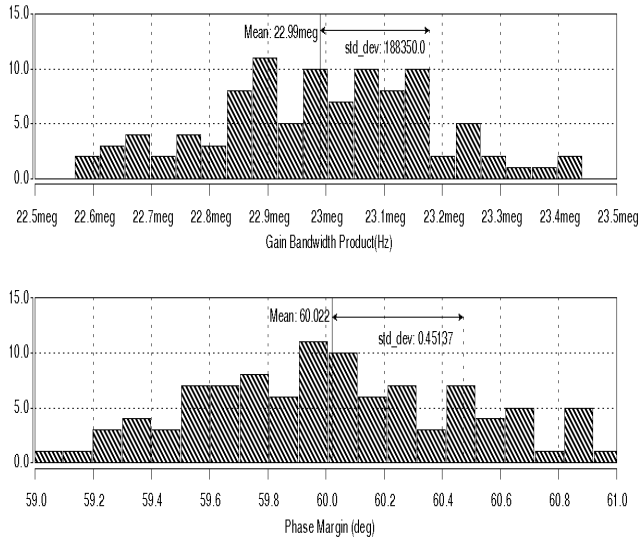

Fig. 8. Phase Margin Monte Carlo simulation

	FBGBTA	CNV-CAS	CNV MILLER	[13]
Gain (dB)	129	101	101	83
GBW (MHz)	23	26	2.7	5.4
Phase Margin (Deg)	60	47	45	67
1% Settling time (ns)	28	47	467	–
Power Consumption (μW)	675	253	253	207
Supply Voltage (V)	$\pm$1.65	$\pm$1.65	$\pm$1.65	$\pm$1.65
Cc (pF)	2.5	2.5	45	2.5 @ $C_L = 5\ pF$
Chip area (mm^2)	0.0269	0.0197	0.0661	–

Tab. 3. Simulation results.

To validate the proposed circuit, a prototype was fabricated using the ON Semiconductor 0.5 μm CMOS technology through MOSIS. Figure 9 shows the circuit microphotography. The amplifier active area is of 124 μm x 217 μm. The circuit was measured with $C_L = 45$ pF, $V_{DD} = \pm 1.65$ V and $I_b = 50\ \mu$A. The measured closed-loop configuration by using a feedback resistor $R_f = 560$ kΩ and an input resistor $R_i = 1$ kΩ leads to a lower frequency gain of $R_f/R_i = 54$ dB.

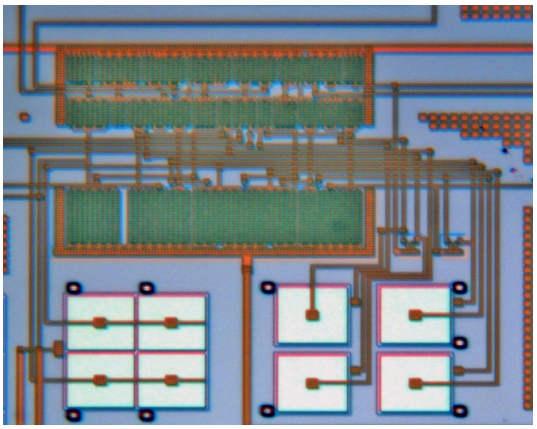

Fig. 9. Microphotography (124 μm x 217 μm).

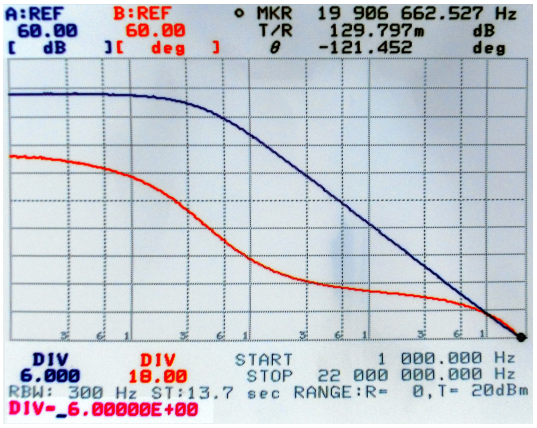

Fig. 10. Measured magnitude and phase responses in closed-loop configuration.

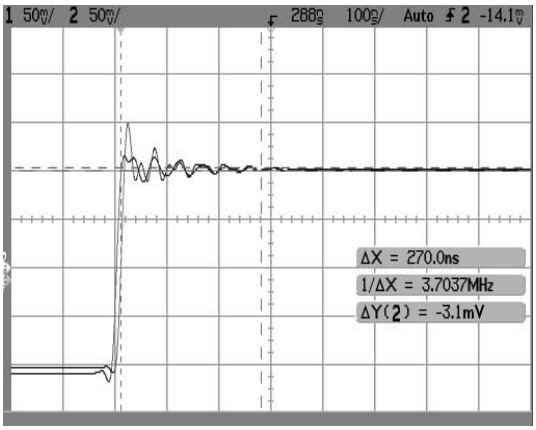

Fig. 11. Experimental step response for a non-inverting unity-gain configuration.

The measured frequency response is depicted in Fig. 10. As can be noticed, a f_{GBW} of 20 MHz and a M_ϕ of 59^o were obtained, which are consistent with the calculated and simulated results of Tab. 2. The measured step response is shown in Fig. 11. A settling time of 270 ns for an input step of 0.1 V with a settle band at 1% of amplitude was obtained. The difference between simulations and measurements of the settling time are basically due to the measurement setup, because in a transient it is not possible to perform the de-embedding of parasitic capacitances, as for

example, wire bonding, package, PCB, connectors, which was estimated in the order of 40 pF.

6. Conclusion

In this paper, a two-stage high-gain CMOS operational amplifier with gain-boosting performed by means of regulated cascode amplifiers was presented. The gain-boosting enhances the low frequency gain and reduces the power supply requirements, while the low impedance nodes created in the first stage are used to implement an indirect current feedback frequency compensation. It produces dominant and non-dominant poles separated from each other, and two zeroes with phase effects that cancel each other out. This frequency compensation also reduces the size of the required capacitors by an order of magnitude, saving silicon area, increasing phase margin and reducing the settling time respect to other Miller compensation schemes. By performing Monte Carlo simulations it was demonstrated that the proposed amplifier is not greatly affected by process variation, preserving stability. Experimental results of a prototype fabricated in an ON Semi 0.5 μm technology validate the synthesis of the circuit performed in Section 4.

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