Low-Voltage High-Linearity Wideband Current Differencing Transconductance Amplifier and Its Application on Current-Mode Active Filter

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Abstract. *A low-voltage high-linearity wideband current differencing transconductance amplifier (CDTA) is presented in this paper. The CDTA consists of a current differencing circuit and a cross-coupling transconductance circuit. The PSPICE simulations of the proposed CDTA show a good performance: -3dB frequency bandwidth is about 900 MHz, low power consumption is 2.48 mW, input current linear range is ±100 μA and low current-input resistance is less than 20 Ω, high current-output resistance is more than 3 MΩ. PSpice simulations for a current-mode universal filter and a proposed high-order filter are also conducted, and the results verify the validity of the proposed CDTA.*

Keywords

Current mode, CDTA, universal filter, high-order filter.

1. Introduction

Recent decades, current-mode circuit techniques have become an important research direction in the field of integrated circuits due to its excellent performance of high slew rate, wide bandwidth, low voltage and low power consumption etc. Many current-mode active elements such as operational transconductance amplifier (OTA) [1], second generation current conveyor (CCII) [2] and current differencing buffered amplifier (CDBA) [3], have been introduced to response these demands [4-7]. Usually current-mode circuits based on CCII, OTA do not have low-input impedance characteristic (passive components connected to the input port), and impedance matching is necessary when it is cascaded. In addition, CCII and OTA's ports have serious parasitic effects. Nowadays, a novel current-mode active element, which is called current differencing transconductance amplifier (CDTA) [8], has been introduced. As the latest development in current mode device, CDTA is the current mode circuit in strict sense and inherits various advantages of the current-mode circuit. From the reported literature, CDTA has been widely used in current-mode signal processing circuit, such as inductance simulator circuits [9], sinusoidal oscillator circuits [10-15], and it especially is a promising choice for realizing the current-mode filters [16-48].

Usually, CDTA can easily be constructed using various techniques, such as CMOS and bipolar technologies [43-48]. Some kinds of CDTA which are formed with a current differencing circuit and a transconductance circuit have been proposed in the literature [44-46]. They are designed applying CMOS technology and share the simple structure. A CMOS current controlled current differencing transconductance amplifier (CCCDTA) has been proposed by literature [47]. This circuit's parasitic resistances at two current input ports can be controlled by an input bias current. Meanwhile, the number of active element in the circuits which use CCCDTA is less than those circuits involving some other active elements. A bulk-driven CDTA, which adopts bulk-driven MOS transistor and shares low-voltage (0.6 V), has been proposed in literature [48].

However, there are some drawbacks for above these circuits: **(a)** Those circuits don't apply all NMOS techniques in AC equivalent circuit, so their bandwidth (frequency characteristic) is limited. In literature [47], frequency range is 100 MHz for I_x/I_n, I_x/I_p and that is less than 300 MHz in [44]. In literature [48], the CDTA is constituted with bulk-driven MOS transistors and frequency range is less than 50 MHz. In addition, its structure is complex and it adopts some extra passive components. For a typical n-well CMOS process, the unity gain frequency of NMOS devices is approximately twice that of PMOS devices. In addition, assuming that the PMOS and NMOS transistor have the same gate length, in order to realize the same transconductance, a PMOS gate length must be 3 times wider than a NMOS [49]. Therefore, in order to avoid the limitation of the high frequency operational by PMOS transistors, a CDTA circuit should be designed so that AC signals pass through only NMOS transistors (circuit's frequency characteristic, slew rate are affected circuit's AC path). In addition, the technology of all NMOS is beneficial to integrated circuit (IC) fabrication. **(b)** Those

circuits [43-48] do not consider improving the linearity of CDTA. Transconductance stages in CDTA circuits [44-47] all adopt source-coupled differential structure and the linear range (I_x~I_p,I_n) of most these circuits is no more than 60 μA. Analysis shows that the linearity of transconductance circuit is restricted by source-coupled differential input stage. So in order to improve the linear range of CDTA, some changes for transconductance stage are very important. **(c)** The voltage value of above those circuits [44-46] is high. Voltage values in above these circuits are 2.5 V in [44-45], 1.8 V in [46]. With the increasing demands for portable and battery-powered equipment, a low-voltage and low power consumption operating circuit becomes necessary, thus CDTA that can be operated in low supply voltage and low power consumption is preferable.

Thus a low-voltage high-linearity wideband CDTA which provides all the desirable features (a)–(c) simultaneously is presented in this paper. The composition of the circuit is based on a NMOS current differencing circuit [50] and a proposed NMOS cross-coupling transconductance circuit. The PSPICE simulations of the proposed CDTA show a good performance: wide frequency bandwidth, low power consumption, high linearity and low resistance current input terminals (p, n), high resistance current output terminals (z, x) which are highly desirable for cascading in current-mode. Meanwhile, a current-mode universal filter and a proposed high-order filter are chosen as application examples in order to demonstrate the validity of the proposed CDTA.

2. Circuit Description of Current Differencing Transconductance Amplifier (CDTA)

The circuit symbol of the CDTA is shown in Fig. 1, where p and n are positive and negative current input terminals, z and x are current output terminals.

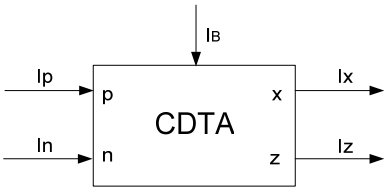

Fig. 1. Symbol for the CDTA.

Its current characteristics can be described by the following matrix equations (1).

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & \pm g_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_x \end{bmatrix} \tag{1}$$

where V_z=I_z*Z_z, g_m is the transconductance gain, and Z_z is an external impedance connected at the terminal z. According to above expression, the current through the terminal z follows the difference of the currents through the terminals p and n (I_p - I_n), and flows from the terminal z into an impedance Z_z. The voltage drop at the terminal z is transferred to a current at the terminal x (I_x) by g_m, which is electronically controllable by an external bias current (I_B).

3. Circuit Configuration

3.1 Current Differencing Circuit

Fig. 2 shows a low-input impedance unity gain current amplifier [50]. From routine circuit analysis, the output current i_{out} of this circuit can be expressed as

$$i_{out} = -\left(\frac{F}{1+F}\right) i_{in} \tag{2}$$

where $F = g_{m2}\, g_{m4}\, r_{oB} / (g_{m1} + g_{m3})$ and r_{oB} denotes the output resistance of the current source I , and g_{mi} represents the transconductance of the transistors M_i ,usually $F>>1$ then the output current i_{out} can be approximated to $i_{out} \cong - i_{in}$.

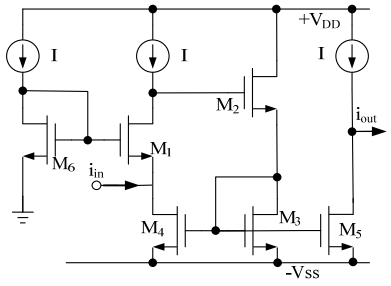

Fig. 2. Low input resistance unity gain current amplifier.

Based on the use of low-input impedance unity gain current amplifier, a NMOS-based current differencing circuit can be shown in Fig. 3.

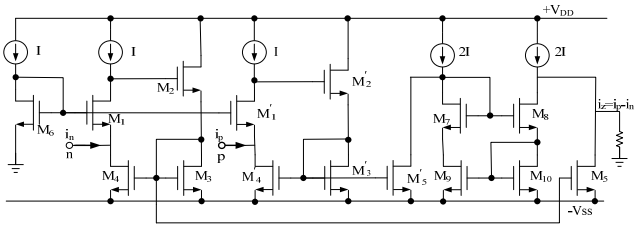

Fig. 3. NMOS-based current differencing circuit.

The current source I and transistor M_6 are used to bias the terminals p and n at ground potential. Groups of transistors (M_1 – M_5) and (M'_1 - M'_5) form two unity-gain current amplifiers that produce the currents ($I + I_n$) and ($I + I_p$) at the drains of M_5 and M'_5, respectively. Let α_p and α_n are the current gains for the inputs from the terminals p and n, respectively. From routine circuit analysis, the output current I_z can be given by

$$i_z = \alpha_p i_p - \alpha_n i_n \tag{3}$$

where
$$\alpha_p = \left(\frac{g_{m7}g_{m8}}{g_{m9}g_{m10}}\right)\left(\frac{F_p}{1+F_p}\right), \quad (4)$$

$$\alpha_n = \left(\frac{F_p}{1+F_p}\right), \quad (5)$$

$$F_p = \left(\frac{g'_{m2}\, g'_{m4}\, r_{oB}}{g'_{m2}+g'_{m3}}\right), \quad (6)$$

$$F_n = \left(\frac{g_{m2}g_{m4}r_{oB}}{g_{m2}+g_{m3}}\right). \quad (7)$$

Since $F_p >>1$, $F_n >>1$, and $g_{m7} \cong g_{m8} \cong g_{m9} \cong g_{m10}$, the current gains are approximated to $\alpha_p \cong \alpha_n \cong 1$.

The input resistances of the terminals p and n can also be

$$r_p = \left(\frac{1}{g'_{m1}}\right)\left(\frac{1}{1+F_n}\right), \quad (8)$$

$$r_n = \left(\frac{1}{g_{m1}}\right)\left(\frac{1}{1+F_p}\right). \quad (9)$$

3.2 Operational Transconductance Circuit

Based on literature [51], a NMOS-based operational transconductance circuit shown in Fig. 4 has been proposed. Transistors M_{11} – M_{14} form cross-coupling transconductance input stage. A unity-gain NMOS-based negative current mirror is formed by transistors M_{15} – M_{18} and current source 2*I*.

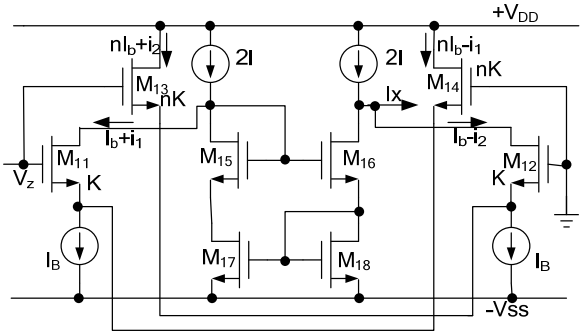

Fig. 4. Proposed NMOS-based operational transconductance circuit.

Here, i_1 and i_2 are AC current signal, supposing $I_b = I_B/(n+1)$ (introduced by subsequent analysis). Supposing M_{11} - M_{14} have same channel length L and the channel width W of M_{13}, M_{14} is *n* times larger than M_{11}, M_{12}. Then M_{11}, M_{12}'s bias current is $I_B/(n+1)$ (I_b); M_{13}, M_{14}'s bias current is $nI_B/(n+1)$ (nI_b). From routine circuit analysis, the relationship of output current I_x and voltage V_z is

$$I_x = i_1 + i_2 = \left(\frac{4n}{n+1}\right)\sqrt{1-\frac{n}{(n+1)^2}\left(\frac{V_z}{\sqrt{I_b/k}}\right)^2}\sqrt{kI_b}V_z \quad (10)$$

where *k* is transistor's (M_{11} – M_{14}) transconductance parameter, $K = \mu_n C_{ox} W/2L$. μ_n, C_{ox} represent transistor's surface mobility, gate oxide capacitance per unit area respectively. The relationship between transconductance of M_{11}, M_{12} and *k* is

$$g_{m11} = g_{m12} = \sqrt{kI_b} \quad (11)$$

and the transconductance of M_{13}, M_{14} is

$$g_{m13} = g_{m14} = \sqrt{nkI_b}\ . \quad (12)$$

When $n >> 1$, equation (10) can be rewritten as follows:

$$I_x = 4\sqrt{kI_b}V_z = 4\sqrt{kI_B/(n+1)}V_z\ . \quad (13)$$

It is also easy to get:

$$I_x = 4\sqrt{kI_B/(n+1)}Z_z(I_p - I_n)\,. \quad (14)$$

Considering the frequency characteristic these functions [52], the error functions can be analyzed as follows:

$$I_x(s) = \frac{4\sqrt{kI_B/(n+1)}V_z}{1+s/\omega_\beta}, \quad (15)$$

$$I_x(s) = 4\sqrt{kI_B/(n+1)}Z_z\left[\frac{1}{1+s/\omega_p}I_p - \frac{1}{1+s/\omega_n}I_n\right] \quad (16)$$

where ω_β, ω_p, and ω_n denote these transfers' corresponding poles. From above these equations, in the case of small signal, the transfer characteristics of I_x and V_z approximates linear relationship. Therefore, the transconductance circuit's linearity is greatly improved. It is also apparent that the transconductance gain of OTA can be adjusted properly by I_B.

The output resistance looking into the z terminal (r_z), the x terminal (r_x) can be expressed as follows, respectively. r_{oi} is the drain-source resistance of the transistor M_i seen at output terminal.

$$r_z \approx \frac{r_{oB}r_{o8}r_{o10}g_{m8}r_{o5}}{r_{oB}r_{o8}r_{o10}g_{m8} + r_{o5}(r_{oB}+r_{o8}r_{o10}g_{m8})}, \quad (17)$$

$$r_x \approx \frac{r_{oB}r_{o16}r_{o18}g_{m16}r_{o12}}{r_{oB}r_{o16}r_{o18}g_{m16} + r_{o12}(r_{oB}+r_{o16}r_{o18}g_{m16})}. \quad (18)$$

3.3 Proposed Low-voltage High-linearity Wideband CDTA

The proposed CDTA consists of two principal building blocks: a NMOS current differencing and a proposed NMOS cross-coupling transconductance circuit. The former can realize current differential function and has low current input resistance and high current output resistance. The latter shares high linearity, transconductance adjustable. Especially, they all share low voltage, wide frequency characteristic. The current differencing circuit consists of

$M_1 - M_{10}$, $M'_1 - M'_5$ and current source. The transconductance amplifier circuit is realized using transistors $M_{11} - M_{18}$, $M'_{11} - M'_{18}$ and current source. Both of the two part of the circuit all share the same voltage source V_{DD} and V_{SS}. It is easy to know that several identical this circuit of transconductance stage can be parallel connected (copied) in the z port, so the number of x port (including x_+, x_-) of the CDTA can be chosen reasonably as actually needed.

Taking into account in real case, ideal current source often is realized by PMOS-based bias current mirrors, a PMOS-based actual bias current mirror circuit has been proposed in Fig. 5. In this case, considering the non-ideal characteristics of actual PMOS-based bias current mirrors (the non-ideal output current caused by the limited impedance of PMOS), so the whole circuit's frequency characteristic be affected. However, these non-ideal characteristics effects are limited and slight. Fig. 6 shows the proposed low-voltage high-linearity wideband CDTA actual circuit.

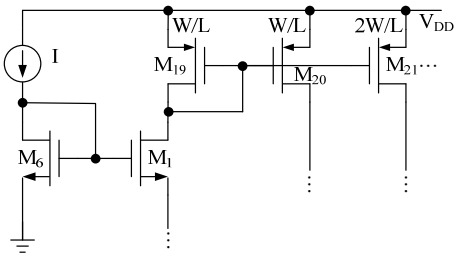

Fig. 5. PMOS-based actual bias current mirror circuit.

4. Simulation Result

The proposed CDTA is suitable for integrated circuit implementation in a CMOS technology. It is simulated by PSPICE software with the parameters of the 0.5 μm (level 3) MIETEC transistor model which is given in Tab. 1. The dimensions of the MOS transistors are listed in Tab. 2. The parameter n used is 85. The supply voltages used are $+V_{DD} = -V_{SS} = 1.25$ V. The constant bias current I, I_B is 30 μA, 314.76 μA respectively. The CDTA's simulation based on PMOS bias circuit has been shown in Fig. 7 to Fig. 13.

CMOS transistors	W(um)/L(um)
M_1-M_{10}, M'_1-M'_5, M_{15}-M_{18} , M'_{15}-M'_{18}	20/1
M_{11}-M_{12} , M'_{11}-M'_{12}	1/1
M_{13}-M_{14} , M'_{13}-M'_{14}	85/1
M_{19}-M_{20}	40/1
M_{21}-M_{24} , M'_{23}-M'_{24}	80/1

Tab. 1. The model parameters of simulation.

The device's DC transfer characteristics given in Fig. 7 proves that the proposed circuit exhibits a very good performance (the simulation value of R_z is 10 k, R_x is 1 k in Fig. 7). In Fig. 7 (a), when V_z changes from -1.0 V ~ 1.0 V, I_x linearly changes in the range of -70 ~ 70 μA. It can easily be seen that the OTA stage of CDTA has a high linearity over the entire dynamic range. In addition, $I_x \sim I_p$, I_n also

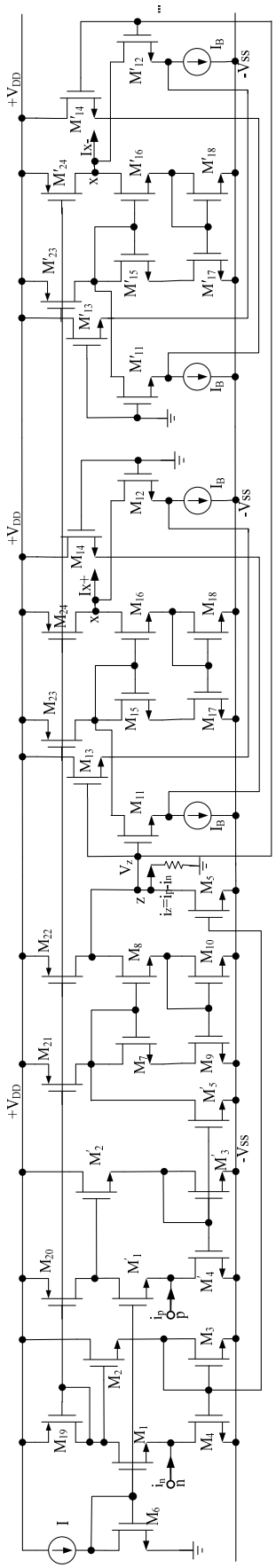

Fig. 6. Proposed low-voltage high-linearity NMOS-based CDTA.

show a good linear characteristic. In Fig. 7(b), when I_p, I_n change from -100~100 µA, I_x linearly changes in the range of -19 ~ 19 µA. It is also found that the circuit power consumption is 2.48 mW.

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.MODEL MOD NMOS LEVEL=3 UO=460.5 TOX=1.0E-8 TPG=1
VTO=.62 JS=1.8E-6 XJ=.15E-6 RS=417 RSH=2.73 ETA=0 LD=0.04E-6
NSUB=1.71E17 VMAX=130E3 PB=0.761 THETA=0.129
GAMMA=0.69 KAPPA=0.1 AF=1 WD=0.11E-6 CJ=76.4E-5 MJ=0.357
CGSO=1.38E-10 KF=3.07E-28 MJSW=0.302 DELTA=.42 NFS=1.2E11
CGDO=1.38E-10 CGBO=3.45E-10 CJSW=5.68E-10 PHI=0.905

.MODEL MOD PMOS LEVEL=3 UO=100 TOX=1.0E-8 TPG=1
VTO=-0.58 LD=0.03E-6 THETA=0.120 ETA=0 VMAX=113E3
RSH=1.81 NSUB=2.08E17 PB=0.911 WD=0.14E-6 JS=0.38E-6 CJ=85E-
5 PHI=0.905 XJ=0.1E-6 CGSO=1.38E-10 RS=886 AF=1 GAMMA=0.76
KAPPA=2 MJ=0.429 CGBO=3.45E-10 CGDO=1.38E-10 KF=1.08E-29
CJSW=4.67E-10 MJSW=0.631 DELTA=.81 NFS=0.52E11
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Tab. 2. Dimensions of the MOS transistors.

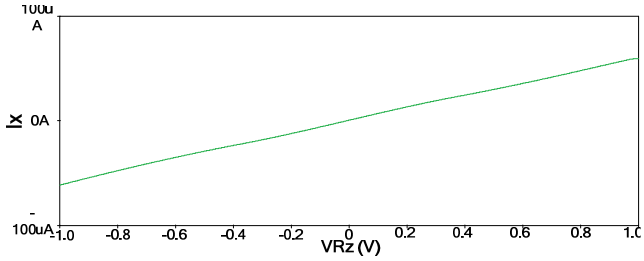

Fig. 7. **(a)** DC transfer characteristics of the proposed CDTA.

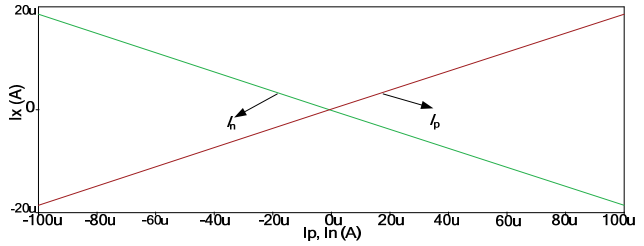

Fig. 7. **(b)** DC transfer characteristics of the proposed CDTA.

In order to further reduce the current gain ripple caused by circuit's internal pole, a frequency compensation has been researched. A compensation capacitor with the value of 0.026 p has been added in the Z port in simulation. Fig. 8 illustrates the AC transfer characteristics of the proposed CDTA. The current transfer ratios, α_p, α_n and transconductance g_m are found to be 1.003, 1.003, 64.8 µS (the simulation value of R_z is 1 k in Fig. 8), respectively.

From Fig. 9, it can be found the proposed CDTA has low current input resistance and high current output resistance in a wide frequency range. The impedance of current input terminal-p and terminal-n are equal to 7.03 Ω, 15.18 Ω in a wide frequency range. It can also be seen from Fig. 9 that the impedances of current output terminal z and x are 3.69 MΩ, 9.35 MΩ in very wide frequency range.

Fig. 10 shows the transient response of the proposed CDTA. Fig. 10(a) is the square wave transient response of CDTA. The input I_p is square wave signal (with amplitude

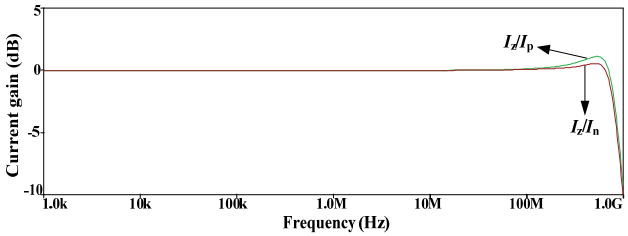

Fig. 8. **(a)** AC transfer characteristics of the proposed CDTA.

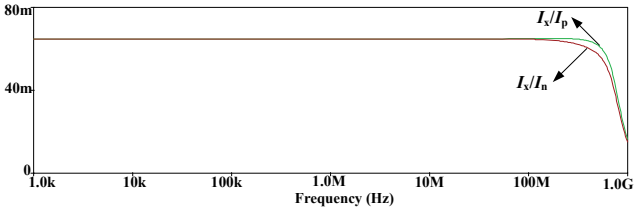

Fig. 8. **(b)** AC transfer characteristics of the proposed CDTA.

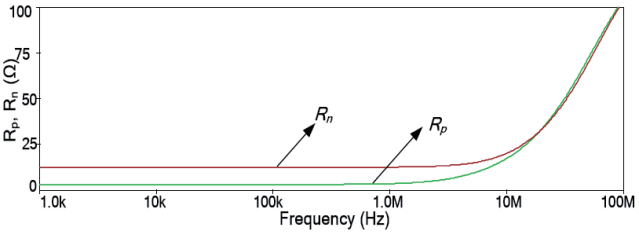

Fig. 9. **(a)** Frequency characteristics of R_p, R_n terminal resistances of the proposed CDTA.

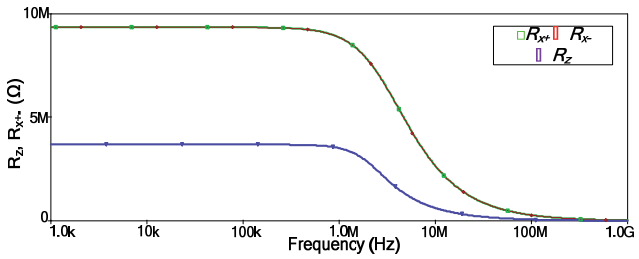

Fig. 9. **(b)** Frequency characteristics of Rz, Rx+- terminal resistances of the proposed CDTA.

of 20 µA, period of 20 ns). This result in Fig. 10(a) confirms that the switching delay time of the CDTA is approximately 3 ns. The circuit's harmonic distortion analysis is made in Fig. 10(b). A sinusoidal current (30 µA/10 kHz, $I_{in} = 30$ µA* $\sin(2\pi*10^4 t)$) as input signal, R_z is 10k, R_x is 1k in this simulation (g_m is 64.8 µS). The input and output of sine signal in Fig. 10(b) show output signal does not appear distortions in amplitude and phase. Simulation file result also shows that circuit's harmonic distortion is low, it is 0.75 %. In addition, for the study of the circuit's harmonic distortion under different amplitude input signals, circuit's total harmonic distortion (THD) figure (sinusoidal current at 10 kHz as input signal, it amplitude changes within the range from 0 to 150 µA) is shown in Fig. 11. It is easy to know that the circuit's THD is less than 1.5% when current doesn't exceed 80 µA. It is noted that the theoretical and simulation results are in good agreement.

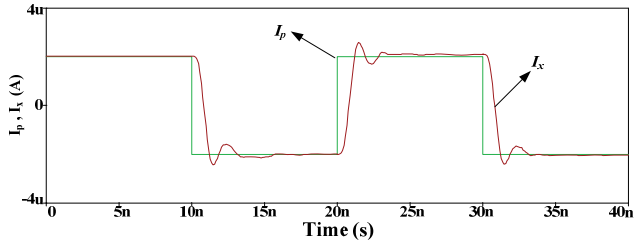

Fig. 10. (a) Square waveforms transient response of the proposed CDTA.

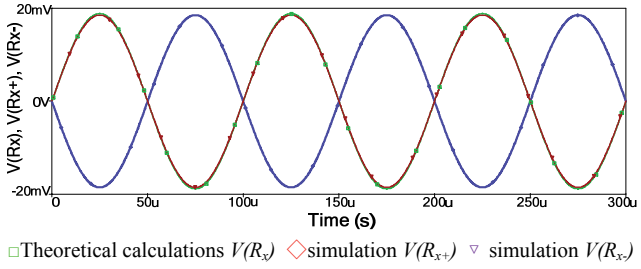

Fig. 10. (b) The sinusoidal waveforms transient response of the proposed CDTA.

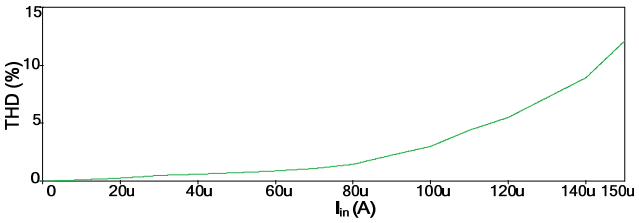

Fig. 11. Total harmonic distortion of the CDTA.

Transconductance controllability of the proposed CDTA has been analyzed in Fig. 12, 13 (the simulation value of R_z is 1k). According to six different bias current, Fig. 12 shows the corresponding AC transfer characteristics. The expected and simulated values of Fig. 12 have been shown in Tab. 3. A range of transconductance value controllability is achieved as shown in Fig. 13 when I_B is varied from 0.01 µA to 1.5 mA. It should be observed that the range of transconductance controllability is wide.

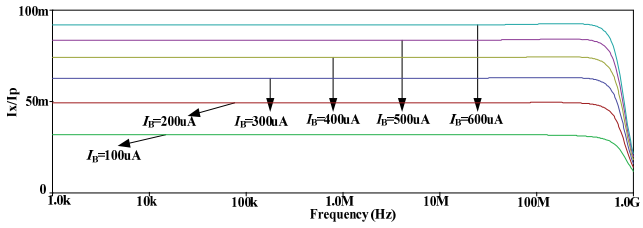

Fig. 12. AC transfer characteristics of the proposed CDTA according to different I_B.

I_B(µA)	100	200	300	400	500	600
I_x/I_p (expected values)	33.3m	49.6m	64.1m	74.8m	82.3m	93.6m
I_x/I_p (simulated values)	33.9m	49.8m	64.8m	75.2m	82.9m	94.1m

Tab. 3. The expected and simulated values of Fig. 12.

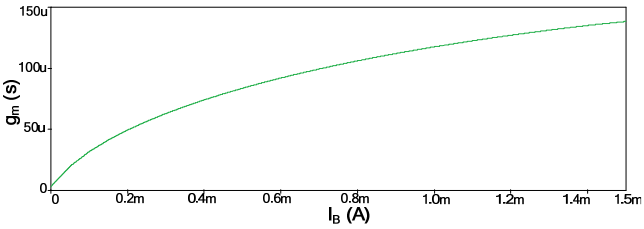

Fig. 13. Transconductance value g_m relative to I_B.

For the purpose of actual application, relevant CADENCE simulations have been made. The layout of the proposed CDTA has been shown in Fig. 14.

Fig. 15 illustrates the AC transfer characteristics of the proposed CDTA based on CADENCE. The simulations show a good feature. The total simulation results are summarized in Tab. 4. Some performance comparisons are summarized in Tab. 5.

Parameter	Simulation results
Supply voltage (V)	±1.25
Bias current, I (µA)	30
Power dissipation (mW)	2.48
Current transfer ratio	
I_z/I_p, I_z/I_n	1.003,1.003
I_x/I_p, I_x/I_n (R_z=1K)	64.80m,64.76m
Current transfer BW (MHz)	
I_z/I_p, I_z/I_n	953.6, 959.6
I_x/I_p, I_x/I_n	926.88, 930.5
Terminal-p, n resistance (Ω)	7.03, 15.18
Terminal-z, x resistance (M Ω)	3.69, 9.35
Input current linear range (I_x ~ I_p, I_n) (uA)	-100 to 100
Voltage linear range (I_x ~ V_z) (V)	-1 to +1
Switching delay time (ns)	3
OTA gain g_m (uS)	64.8(Using in simulation example)
	0.84 ~ 138.34(Adjustable range)

Tab. 4. Performance of the proposed CDTA.

Parameter	Ref[20]	Ref[22]	Ref[23]	This work
Supply voltage	±2.5 V	±1.8 V	±1.5 V	±1.25 V
Current linear range	±60 µA	±80 µA	±80 µA	±100 µA
Bandwidth(I_x/I_p)	—	1011 MHz	142 MHz	927 MHz
Whether all NMOS in AC	NO	NO	NO	Yes
Gm adjustable range	—	—	0.25–1 mS	0.8–138.4 µS
Power dissipation	4.4 mW	6.31 mW	1.48 mW	2.48 mW
Terminal-p, n impedance	645, 506	1.92, 1.92	821–25.1k	7.03, 15.18
Terminal-z, x impedance	1 GΩ , R_x no give	338 kΩ , 16.3 MΩ	1.03 MΩ 999 kΩ	3.7 Ω , 9.4 MΩ

Tab. 5. Performance comparison of CDTAs.

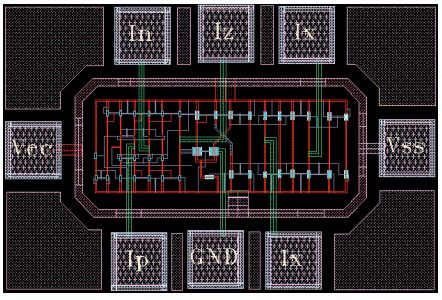

Fig. 14. The layout of the proposed CDTA.

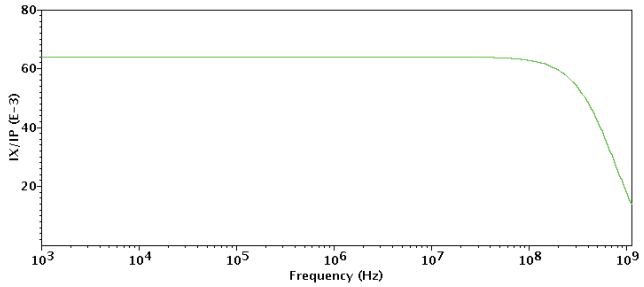

Fig. 15. AC transfer characteristics of the proposed CDTA based on CADENCE.

5. Application on Current-Mode Active Filter

To confirm the validity of the proposed building CDTA, some applications are given here to demonstrate and prove the performances of the applications of the proposed element.

5.1 Current-mode Second-order Universal Filter

The first application example of the proposed CDTA is a second-order universal filter using CDTAs, grounded capacitors are realized [38]. Here, one of the CDTAs involved in the circuit is chosen with three x ports. Supposing the natural angular frequency ω_o of the filter is 2π*30 rad/sec, quality factor Q is 1, according to the value of g_{mi} ($g_{m1} = g_{m2}$= 64.8 μS) and transfer function as follows, it is easy to get the value of C_i ($C_1 = C_2 = 2.16$ pF).

The output current function realized by this circuit configuration is:

$$I_o = \frac{I_1 \frac{g_{m1}g_{m2}}{C_1C_2} + sI_2\frac{g_{m2}}{C_2}}{s^2 + s\frac{g_{m2}}{C_2} + \frac{g_{m1}g_{m2}}{C_1C_2}} + I_3 . \quad (19)$$

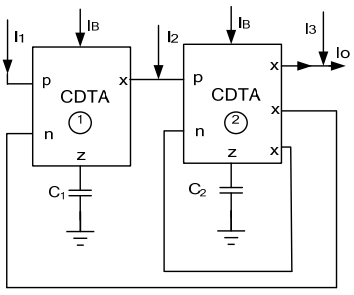

Fig. 16. CDTA-based second-order current-mode universal filter.

a) If $I_2 = I_3 = 0$ and $I_1 = I_{in}$, the LP response can be realized.

b) If $I_1 = I_3 = 0$ and $I_2 = I_{in}$, the BP response can be realized.

c) If $-I_1 = -I_2 = I_3 = I_{in}$, the HP response can be realized.

d) If $I_1 = 0$ and $-I_2 = I_3 = I_{in}$, the BS response can be realized.

e) If $I_1 = 0$, $I_2 = -2I_{in}$ and $I_3 = I_{in}$, the AP response can be realized.

The ω_o and Q of this filter are shown as follows:

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} , \quad (20)$$

$$Q = \sqrt{\frac{g_{m1}C_2}{g_{m2}C_1}} . \quad (21)$$

It is easy to know that the sensitivities of this universal filter are shown as follows:

$$S^{\omega_0}_{g_{m1},g_{m2}} = -S^{\omega_0}_{C_1,C_2} = 1/2, \quad (22)$$

$$S^{\omega_0/Q}_{g_{m2}} = -S^{\omega_0/Q}_{C_2} = 1, \quad (23)$$

$$S^{\omega_0/Q}_{g_{m1},C_1} = 0. \quad (24)$$

Fig. 17 shows the simulation results. It is noted that the theoretical and simulation results are in good agreement.

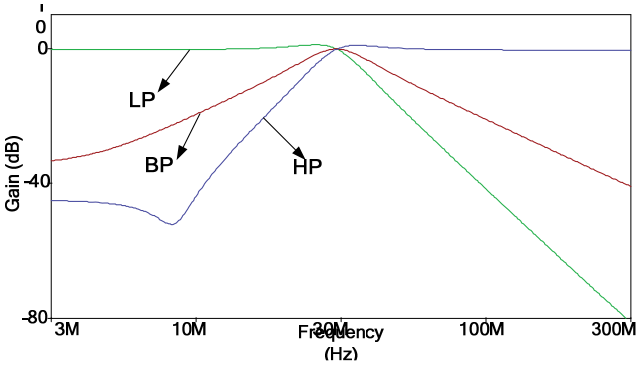

Fig. 17. (a) LP, BP, HP frequency responses of the universal filter.

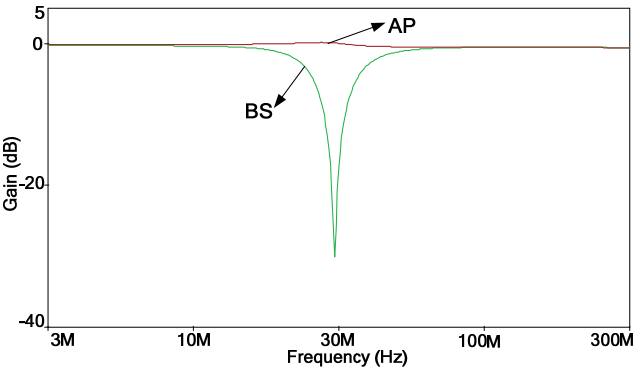

Fig. 17. (b) BS, AP frequency responses of the universal filter.

Considering the CDTA's parasitic influences, the non-ideal circuit shown in Fig. 18 has been analyzed as fol-

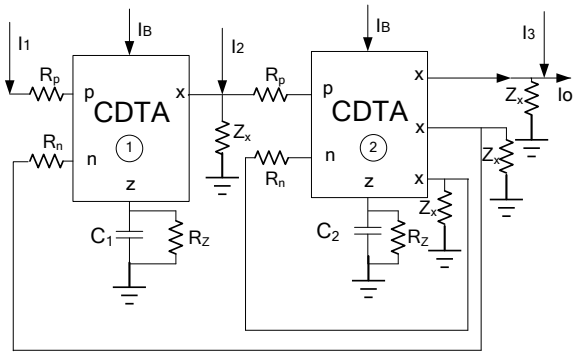

Fig. 18. Non-ideal circuit of Fig. 16.

lows: as in a non-ideal CDTA, assuming x terminals have almost the same resistors R_x and capacitors C_x, $Z_x = R_x//(1/sC_x)$; p, n terminals resistors are R_p, R_n; z terminals resistor is R_z. By routine analysis, its current can be re-described:

$$I_o = \frac{\left[\frac{g_{m1}g_{m2}}{C_1C_2}I_1 + \frac{g_{m2}}{C_2}(s+\frac{1}{R_zC_1})I_2\right]B}{F(s)} + I_3 \quad (25)$$

where

$$F(s) = s^2 + \left[\frac{1}{R_z}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)+\frac{Ag_{m2}}{C_2}\right]s + \frac{1}{C_1C_2}\left[\frac{(1+AR_zg_{m2})}{R_z^2}+ABg_{m1}g_{m2}\right] \quad (26)$$

$$A = \frac{R_x}{R_x+R_n(1+sR_xC_x)},\ B = \frac{R_x}{R_x+R_p(1+sR_xC_x)}. \quad (27)$$

Among usually A≈ B≈ 1, it is easy to get the circuit's non-ideal transfer function *H(s)* respectively:

a) $$H(s)_{LP} = \frac{g_{m1}g_{m2}/C_1C_2}{F(s)}, \quad (28)$$

b) $$H(s)_{BP} = \frac{\frac{g_{m2}}{C_2}(s+\frac{1}{R_zC_1})}{F(s)}, \quad (29)$$

c) $$H(s)_{HP} = \frac{s^2+\left[\frac{1}{R_z}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\right]s+\frac{1}{R_z^2C_1C_2}}{F(s)}, \quad (30)$$

d) $$H(s)_{BS} = \frac{\alpha_{BS}(s)}{F(s)} \quad (31)$$

where

$$\alpha_{BS}(s) = s^2 + \left[\frac{1}{R_z}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\right]s + \frac{1}{C_1C_2}\left(\frac{1}{R_z^2}+g_{m1}g_{m2}\right) \quad (32)$$

e) $$H(s)_{AP} = \frac{\alpha_{AP}(s)}{F(s)} \quad (33)$$

where

$$\alpha_{AP}(s) = s^2 + \left[\frac{1}{R_z}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)-\frac{g_{m2}}{C_2}\right]s + \frac{1}{C_1C_2}\left[\frac{(1-R_zg_{m2})}{R_z^2}+g_{m1}g_{m2}\right] \quad (34)$$

Through comparative analysis (28) to (34) and (19), it is easy to find some non-ideal terms arise in these non-ideal transfer functions. When the value of R_z tends to ideal infinite, equations (28) to (34) can be converted into ideal transfer functions which are shown in (19). From (28) to (34), it is apparent that LP response's parasitic is nil, and BS, AP's is relatively low, BP and HP's is relatively high. So it is also easy to find some parasitic in above simulation results in Fig. 17, such as the BP and HP response.

5.2 Current-Mode High-Order Filter

To further illustrate the application of the proposed CDTA device, a CDTA-based ladder filter is proposed. From literatures published in recent years, CDTA-based filter involve too many active and passive components, such as circuits [33], [37] include some excess CDTAs, circuits [36], [37] use too many resistors. In general, keeping the number of active elements at minimum has obvious practical significance in low power dissipation, smaller chip area. The proposed filter, which adopts only 4 active components, 4 capacitors and doesn't use any resistor, can realize 4th-order lowpass filter function and shares simple configuration. Meanwhile, the proposed filter circuit which adopts minimum components (doesn't involve any resistor) further reduces parasitics and can avoid the influence of resistance on the bandwidth of the circuit. Relative to some others IC based design filter, such as OTA-based filter (CA3080, $BW = 2$ MHz, $V_{pp} = \pm 15$ V), CCII (AD844, $BW = 20$ MHz, $V_{pp} = \pm 20$ V), OP (LF741A, $BW = 1.5$ MHz, $V_{pp} = \pm 15$ V), the proposed filter based on the proposed CDTA has some advantages in the number of active and passive elements, power consumption, bandwidth, parasitics etc. In particular, its p, n- terminal do not have parasitic capacitance, it expands circuit's bandwidth greatly. The actual passive LC ladder filter circuit and CDTA-based proposed filter are shown in Fig. 19, 20. The filter's cutoff frequency is 10 MHz and corresponding passive LC filter's component parameters [53] are: $C'_1 = 1.22$ pF, $L_2 = 0.29$ mH, $C'_3 = 2.94$ pF, $L_4 = 0.12$ mH.

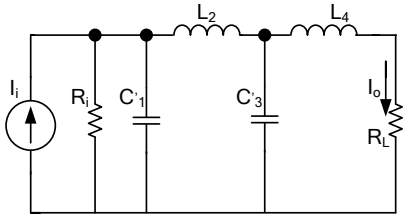

Fig. 19. Current-mode 4th-order passive LC ladder network.

Through comparative analysis of circuit parameters in Fig. 19 and 20, it is easy to get the value of C_i (Fig. 20)

from above parameter's value in Fig. 19 (g_{mi} = 64.8 μS): C_1 = 0.4 pF, C_2 = 0.96 pF, C_3 = 0.96 pF, C_4 = 0.4 pF. Fig. 21 shows the simulation results. It is noted that the theoretical and simulation results are in good agreement.

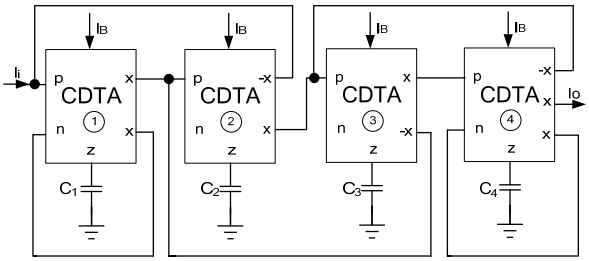

Fig. 20. Proposed CDTA-based current-mode 4th-order ladder filter.

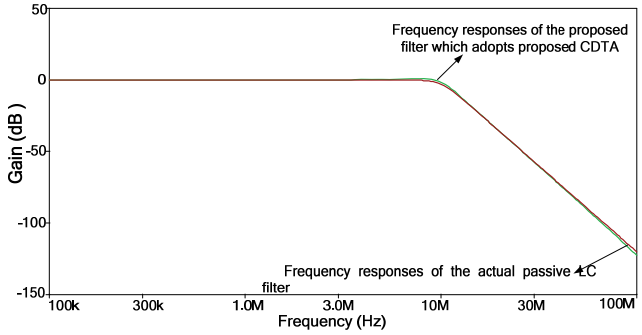

Fig. 21. Frequency responses of the proposed filter and actual filter.

6. Conclusion

A low-voltage high-linearity wideband CDTA is presented in this paper. The composition of the circuit is based on a current differencing circuit and a proposed cross-coupling transconductance circuit. The PSpice simulations of the proposed CDTA show a good performance: wide frequency bandwidth, low power consumption and high-linearity which are in good agreement with theory. A current-mode universal filter and a proposed high-order filter are also chosen as application examples and the results verify the validity of the proposed CDTA.

Acknowledgements

The authors would like to thank the National Natural Science Foundation of China for financially supporting this research under No. 61274020 and the Open Fund Project of Key Laboratory in Hunan Universities under No. 12K011.

References

[1] DELIYANNIS, T., SUN, Y., FIDLER, J. K. *Continuous-Time Active Filter Design*. USA: CRC Press, 1999.

[2] SEDRA, A., SMITH, K. C. A second generation current conveyor and its application. *IEEE Transactions on Circuit Theory*, 1970, vol. 17, no. 1, p. 132-134.

[3] ACAR, C., OZOGUZ, S. A new versatile building block: current differencing buffered amplifier suitable for analog signal processing filters. *Microelectron J*, 1999, vol. 30, p.157–160.

[4] BIOLEK, D., BAJER, J., BIOLKOVA, V. Z copy-controlled gain-current differencing buffered amplifier and its applications. *International Journal of Circuit Theory and Applications,* 2011, vol. 39, p. 257–274.

[5] AYDOGMUS, M. A., KUNTMAN, H. New CMOS realization of ZC-CG-CDBA and its filter application. In *Signal Processing and Communications Applications Conference (SIU)*, 2012, p. 1-4.

[6] BIOLEK, D., LAHIRI, A., JAIKLA, W. Realization of electronically tunable voltage-mode/current-mode quadrature sinusoidal oscillator using ZC-CG-CDBA. *Microelectronics Journal*, 2011, vol. 42, no. 10, p. 1116-1123.

[7] BAJER, J., BIOLEK, D. Digitally controlled quadrature oscillator employing two ZC-CG-CDBAs. In *Proceedings of the International Conference on EDS*. 2009, vol. 31, p. 126-132.

[8] BIOLEK, D. CDTA - Building block for current-mode analog signal processing. In *Proceedings of the European Conference on Circuit Theory and Design 2003 - ECCTD'03*. 2003, p. 397-400.

[9] JAIKLA, W., SIRIPRUCHYANUN, M. Current controlled CDTA (CCCDTA) based- novel floating and grounded inductance simulators. *Communications and Information Technologies*, 2006, p. 348-351.

[10] TANGSRIRAT, W. Current-mode multiphase sinusoidal oscillator using CDTA-based all-pass sections. *Int. J. Electron. Commun. (AEU)*, 2009, vol. 63, p. 616 –622.

[11] KESKIN, A. U., BIOLEK, D. Current mode quadrature oscillator using current differencing transconductance amplifiers (CDTA). *IEE Proc.-Circuits Devices Syst*, 2006, vol. 153, p. 248-252.

[12] JAIKLA, W., LAHIRI, A. Resistor-less current-mode four-phase quadrature oscillator using CCCDTAs and grounded capacitors. *Int. J. Electron. Commun. (AEU)*, 2012, vol. 66, p. 214 –218.

[13] YONGAN, L. A new single MCCCDTA based Wien-bridge oscillator with AGC. *Int. J. Electron. Commun. (AEU)*, 2012, vol. 66, p. 153 –156.

[14] SAKUL, C., JAIKLA, W., DEJHAN, K. New resistorless current-mode quadrature oscillators using 2 CCCDTAs and grounded capacitors. *Radioengineering*, 2011, vol. 20, p. 890-898.

[15] JAIKLA, W., PROMMEE, P. Electronically tunable current-mode multiphase sinusoidal oscillator employing CCCDTA-based allpass filters with only grounded passive elements. *Radioengineering*, 2011, vol. 20, p. 594 –600.

[16] SIRIPRUCHYANUN, M., JAIKLA, W. Electronically controllable current-mode universal biquad filter using single DO-CCCDTA. *Circuits System Signal Process*, 2008, vol. 27, p.113–122.

[17] SHAH, N. A., QUADRI, M., IQBAL, S. Z. CDTA based universal transadmittance filter. *Analog Integr. Circuits Signal Process*, 2007, vol. 52, p. 65–69.

[18] TANJAROEN, W., TANGSRIRAT, W. Current-mode second-order notch filter using CDTA-based allpass sections. In *SICE Annual Conference*. 2008, p. 1143-1146.

[19] TANJAROEN, W., DUMAWIPATA, T., TANGSRIRAT, W. TISO cascadable current-mode multifunction filter employing current differencing transconductance amplifiers. In *SICE-ICASE International Joint Conference*, 2006, p. 5703-5706.

[20] TANJAROEN, W., TANGSRIRAT, W. Resistorless current-mode first-order allpass filter using CDTAs. *Electrical Engineering, Electronics, Computer, Telecommunications and Information Technology*, 2008, vol. 2, p. 721-724.

[21] TANGSRIRAT, W., PUKKALANUN, T., SURAKAMPONTORN, W. Resistorless realization of current-mode first-order allpass filter using current differencing transconductance amplifiers. *Microelectronics Journal*, 2010, vol. 41, p. 178–183.

[22] PRASAD, D., BHASKAR, D. R., SINGH, A. K. Universal current-mode biquad filter using dual output current differencing transconductance amplifier. *Int. J. Electron. Commun. (AEU)*, 2009, vol. 63, p. 497 –501.

[23] UYGUR, A., KUNTMAN, H. Design of a current differencing transconductance amplifier (CDTA) and its application on active filters. In *Signal Processing and Communications Applications Conference*. 2005, p. 340-343.

[24] BIOLEK, D., HANCIOGLU, E., KESKIN, A. U. High-performance current differencing transconductance amplifier and its application in precision current-mode rectification. *Int. J. Electron. Commun. (AEU)*, 2008, vol. 62, p. 92–96.

[25] KACAR, F., KUNTMAN, H. H. A new, improved CMOS realization of CDTA and its filter applications. *Turkish Journal of Electrical Engineering and Computer Sciences*, 2011, vol. 19, p. 631 –642.

[26] PRASAD, D., BHASKAR, D. R., SINGH, A. K. Multi-function biquad using single current differencing transconductance amplifier. *Analog Integr. Circuits Signal Process*, 2009, vol. 61, p. 309 –313.

[27] BIOLEK, D., BIOLKOVA, V., KOLKA, Z. Current-mode biquad employing single CDTA. *Indian J. Pure Appl. Phys*, 2009, vol. 47, p. 535-537.

[28] KACAR, F., KUNTMAN, H. H. A new CMOS current differencing transconductance amplifier (CDTA) and its biquad filter application. In *Eurocon 2009: International IEEE Conference Devoted to the 150 Anniversary of Alexander S. Popov*. 2009, p. 189-196.

[29] SHAH, N. A., QUADRI, M., IQBAL, S.Z. High output impedance current-mode all-pass inverse filter using CDTA. *Indian J. Pure Appl. Phys*, 2008, vol. 46, p. 893-896.

[30] SHAH, N. A., QUADRI, M., IQBAL, S.Z. Realization of CDTA based current-mode universal filter. *Indian J. Pure Appl. Phys*, 2008, vol. 46, p. 283-285.

[31] SHAH, N. A., QUADRI, M., IQBAL, S.Z. Application of CDTA in the realisation of current-mode active filter. *Electronics World*, 2007, vol. 113, p.42-43.

[32] SHAH, N. A., QUADRI, M., IQBAL, S.Z. Current-mode multifunction filter using current differencing transconductance amplifier. *Indian J. Pure Appl. Phys*, 2007, vol. 45, p. 767-769.

[33] DUMAWIPATA, T., TANGSRIRAT, W., SURAKAMPONTORN, W. Cascadable current-mode multifunction filter with two inputs and three outputs using CDTAs. In *2007 6th International Conference Information, Communications & Signal Processing.* 2007, p. 10-13.

[34] TANGSRIRAT, W., PUKKALANUN, T. Structural generation of two integrator loop filters using CDTAs and grounded capacitors. *International Journal of Circuit Theory and Applications*, 2011, vol. 39, p. 31–45.

[35] UYGUR, A., KUNTMAN, H. Seventh-order elliptic video filter with 0.1 dB pass band ripple employing CMOS CDTAs. *Int. J. Electron. Commun. (AEU)*, 2007, vol. 61, p. 320–328.

[36] BEKRI, A., ANDAY, F. Nth-order low-pass filter employing current differencing transconductance amplifiers. In *Proceedings of the 2005 European Conference on Circuit Theory and Design*. 2005, p. 193–196.

[37] DOSTAL, T., SMEJKAL, V., SLEZAK, J. Realization of arbitrary transfer current characteristic using transconductors CDTA. In *18th International Conference Radioelektronika.* 2008, p. 24-25.

[38] TANGSRIRAT, W., DUMAWIPATA, T., SURAKAMPONTORN, W. Multiple-input single-output current-mode multifunction filter using current differencing transconductance amplifiers. *Int. J. Electron. Commun. (AEU)*, 2007, vol. 61, p. 209 –214.

[39] YONGAN, L. A Modified CDTA (MCDTA) and its applications: Designing current-mode sixth-order elliptic band-pass filter. *Circuits System Signal Process*, 2011, vol. 30, no. 6, p. 1383-1390.

[40] JAIKLA, W., SIRIPRUCHYANUN, M., BAJER, J., BIOLEK, D. A simple current-mode quadrature oscillator using single CDTA. *Radioengineering*, 2008, vol. 17, no. 4, p. 33–40.

[41] LAHIRI, A., CHOWDHURY, A. A novel first-order current-mode all-pass filter using CDTA. *Radioengineering*, 2009, vol. 18, no. 3, p. 300-306.

[42] BIOLEK, D., SENANI, R., BIOLKOVA, V., KOLKA, Z. Active elements for analog signal processing: classification, review, and new proposals. *Radioengineeing*, 2008, vol. 17, no. 4, p. 15-32.

[43] SIRIPRUCHYANUN, M., JAIKLA, W. Current controlled current differencing transconductance amplifier and applications in continuous-time signal processing circuits. *Analog Integr Circ Sig Process* , 2009, vol. 61, p. 247–257.

[44] UYGUR, A., KUNTMAN, H. Design of a current differencing transconductance amplifier (CDTA) and its application on active filters. *Signal Processing and Communications Applications Conference*, 2005, p. 340-343.

[45] KESKIN, A. U., BIOLEK, D., HANCIOGLU, E., BIOLKOVA, V. Current-mode KHN filter employing current differencing transconductance amplifiers. *Int. J. Electron. Commun. (AEU)*, 2006, vol. 60, p. 443–446.

[46] BIOLEK, D., HANCIOGLU, E., KESKIN, A. U. High-performance current differencing transconductance amplifier and its application in precision current-mode rectification. *Int. J. Electron. Commun. (AEU)*, 2008, vol. 62, p. 92–96.

[47] SIRIPRUCHYANUN, M., JAIKLA, W. CMOS current-controlled current differencing transconductance amplifier and applications to analog signal processing. *Int. J. Electron. Commun. (AEU)*, 2008, vol. 62, p. 277–287.

[48] KHATEB, F., BIOLEK, D. Bulk-driven current differencing transconductance amplifier. *Circuits System Signal Process*, 2011, vol. 30, p. 1071–1089.

[49] ALLAM, E. A., MANKU, T., TING, M. Impact of technology scaling on CMOS RF devices and circuits. In *Proceedings of the IEEE 2000 Custom Integrated Circuits Conference*. 2000, p. 361–364.

[50] TANGSRIRAT, W., KLAHAN, K., DUMAWIPATA, T., SURAKAMPONTORN, W. Low-voltage NMOS-based current differencing buffered amplifier and its application to current-mode ladder filter design. *International Journal of Electronics*, 2006, vol. 93, p. 777-791.

[51] [51] NEDUNGADI, A., VISWANATHAN, T. Design of linear CMOS transcenductance elements. *IEEE Transactions on Circuits and Systems*, 1984, vol. 31, p.891-894.

[52] KHATIB, F., KHATIB, N., KUBANEK, D. Novel low-voltage low-power high-precision CCII± based on bulk-driven folded cascode OTA. *Microelectronics Journal*, 2011, vol. 42, p. 622-631.

[53] WILLIAMS, B. *Electronic Filter Design Handbook*. New York: McGraw Hill Book Company, 1981.

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