DCCII-Based Novel Lossless Grounded Inductance Simulators with No Element Matching Constrains

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Abstract. *In 1996, the differential current conveyor (DCCII) was introduced as a versatile active element with current differencing capability. Therefore, in this study, the usefulness of the DCCII is shown on six novel lossless grounded inductance simulator circuits. Proposed circuits simultaneously employ minimum number of elements, i.e. single DCCII, one capacitor, and two resistors. No passive element matching restriction is needed and all solutions are electronically tunable in case that one of resistors is replaced by MOSFET-based voltage-controlled resistor. The internal structure of the active element has been implemented using the TSMC 0.25 μm SCN025 CMOS process BSIM3v3.1 parameters. Firstly, the performance of the selected inductor simulator is evaluated and subsequently verified in the design of 5^{th}-order high-pass ladder and 2^{nd}-order frequency filters. In addition, experimental results using commercially available AD844/ADs are given to verify the theoretical analysis and SPICE simulations.*

Keywords

DCCII, differential current conveyor, inductance simulator, ladder filter, lossless grounded inductor.

1. Introduction

In the literature several lossless (pure) synthetic inductance simulators have been proposed since direct physical implementation of inductors on an integrated chip may not satisfy performance requirements of the circuits in comparison to resistors and capacitors in the integrated circuit (IC) realization point of view. For example, they have larger chip area than other passive circuit elements when high inductance values are needed. Therefore, during last few decades the design of synthetic inductors has received considerable attention. The most famous inductance simulators were proposed by Ford & Girling [1] and Antoniou [2] in 1966 and 1969, respectively. Both realizations utilize two Op-Amps and four passive elements to obtain an inductor. However, compared to Op-Amps, current conveyors (CCs) and other high-performance active building blocks (ABBs) provide many advantages such as greater linearity, wider bandwidth, and better dynamic range [3]. In 1978, the Ford & Girling inductor equivalent using CCs was introduced by Soliman [4] and it became a key reference to many other inductance simulators available in the literature that have been obtained by its modification in order to realize an ideal inductor. During last few decades many lossless grounded synthetic inductor topologies have been proposed in the literature [5]–[18], [30] and their performance is summarized in Tab. 1. For example, the grounded lossless inductance simulators based on second and first-generation current conveyor in [5]–[7] employ single capacitor and respectively four, three, and four resistors. In [8] and [9], novel simulated inductors employing a single novel CCs so-called minus-type modified inverting first- and second-generation current conveyor (MICCI– / MICCII–) are introduced. These inductors employ minimum number of active and passive components, but both require passive component matching constraint. Another minimum active and passive elements-based grounded inductor with passive component matching constraint employing plus-type gain-variable third-generation current conveyor (GVCCIII+) is proposed in [10]. Although the single fully differential second-generation current conveyor (FDCCII)-based circuits reported in [11] also employ minimum number of components, passive component matching constraints and excessive number of transistors in the used FDCCII structure make these circuits unpractical. Similarly, the dual-X second-generation current conveyor (DXCCII)-based inductor simulators in [12]–[14] also require passive component matching. The operational transresistance amplifier (OTRA) has also received considerable attention, which resulted in recently published works [15]–[17]. Circuits in [15] employ two OTRAs, while in [16] and [17] one OTRA and voltage buffer (VB) or only single OTRA is used, respectively. As drawback of solutions [16] and [17] the usage of two capacitors can be mentioned. Finally, the single positive four-terminal-floating-nullor (PFTFN) based lossless grounded inductance simulation circuit is worth to be mentioned [18], in which a complex resistor matching can be highlighted as the drawback.

Reference	Year	No. and type of ABBs	No. of transistors	No. of capacitors	No. of resistors	Passive element matching constraints
[5] - Fig. 1	1978	1 CCII+	–	1	4	Yes
[6] - Figs. 2 (a), (b)	2004	1 CCI	12*	1	3	Yes
[7] - Fig. 2(a)	2012	1 CCI	26*	1	4	Yes
[8] - Fig. 1	2007	1 MICCI–	34	1	2	Yes
[9] - Fig. 2	2005	1 MICCII–	8	1	2	Yes
[10] - Fig. 3(a)	2006	1 GVCCIII+	26	1	2	Yes
[11] - Figs. 2(b)-(e)	2010	1 FDCCII	92*	1	2	Yes
[12] - Fig. 2(b)	2010	1 DXCCII	48	1	2	Yes
[13] - Figs. 2 (a), (c)-(f)	2011	1 DXCCII	28	1	2 / 3	Yes
[14] - Fig. 3(a)	2012	1 DXCCII	29*	1	3	Yes
[15] - Figs. 2(a), (b)	2011	2 OTRA	28	1	5	Yes
[16] - Fig. 5	2012	1 OTRA, 1 VB	*D*	2	2	Yes
[17] - Fig. 2	2013	1 OTRA	14	2	3	Yes
[18] - Fig. 1	2010	1 PFTFN	32*	1	4	Yes
[30] - Figs. 2(a), (b)	2012	1 DCCII	27*	1	2	Yes
This work - Figs. 2(a)-(f)	2013	1 DCCII	34	1	2	No

Tab. 1. Comparison of previously published lossless grounded inductance simulators (Notes: – Not mentioned; * Ideal current source(s) are assumed; *D* Direct ICs are used).

In 1996, the differential current conveyor (DCCII) was introduced by Elwan and Soliman as the first active element with current differencing capability [19]. In fact, the DCCII combines the simplicity of the classical CCII [20] with current differencing feature of the conventional current differencing buffered amplifier (CDBA) [21]. Therefore, the DCCII looks like a CDBA for current differencing operation, but it has an additional voltage terminal like CCII, which has high-input impedance. Unfortunately, in the literature it has not received as much attention as the CDBA yet and up to now only few DCCII-based applications are published [22]–[30]. Our short study showed that only [30] deals with lossless grounded inductance simulator design. Although the circuits in [30] seem to be very attractive inductance simulators, similarly to above discussed works [5]-[18], the passive element matching restriction brings a drawback to it. Therefore, the aim of this work is to increase the variety of DCCII circuits in the literature with introduction of six novel lossless grounded synthetic inductors that simultaneously provide the following important features:

(i) employ minimum number of active and passive components,

(ii) no passive element matching restriction is required in any of presented circuits,

(iii) circuits are electronically tunable, if the grounded resistor is replaced by metal–oxide–semiconductor field-effect transistor (MOSFET)-based voltage-controlled resistor (VCR) [31], [32],

(iv) and they show versatility of the DCCII in the inductance simulator configuration.

The performance of the active element and inductors are verified using SPICE software. The application possibility of selected inductance simulator is subsequently shown on the design of the 5$^{\text{th}}$-order high-pass and 2$^{\text{nd}}$-order three function filters. In addition, experimental results are given to prove the operation of a 2$^{\text{nd}}$-order high-pass Butterworth filter.

2. Circuit Description

The DCCII [19] is a five-terminal analog building block, whose circuit symbol is shown in Fig. 1. The difference of the currents at the X_P and X_N terminals is reflected to the Z terminals. The voltage potential of the Y terminal is copied to the X_P and X_N terminals. Considering the non-idealities caused by the physical implementation of the DCCII, it is described with the following hybrid matrix:

$$\begin{bmatrix} v_{XN} \\ v_{XP} \\ i_{Z+} \\ i_{Z-} \\ i_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_N \\ 0 & 0 & \beta_P \\ \alpha_P & -\alpha_N & 0 \\ -\alpha_N & \alpha_P & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{XP} \\ i_{XN} \\ v_Y \end{bmatrix} \tag{1}$$

where β_i and α_i for $i = \text{N}, \text{P}$ represent the voltage and current gains of the DCCII that are ideally equal to unity.

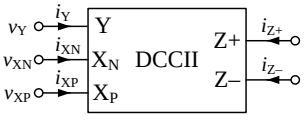

Fig. 1. Circuit symbol of the DCCII.

The proposed circuits realizing grounded inductor simulators employing single DCCII, single capacitor, and two resistors are shown in Figs. 2(a)–(f). Considering ideal DCCII ($\beta_N = \beta_P = 1$ and $\alpha_N = \alpha_P = 1$), routine circuit analyses yield the following input impedance for all six variants:

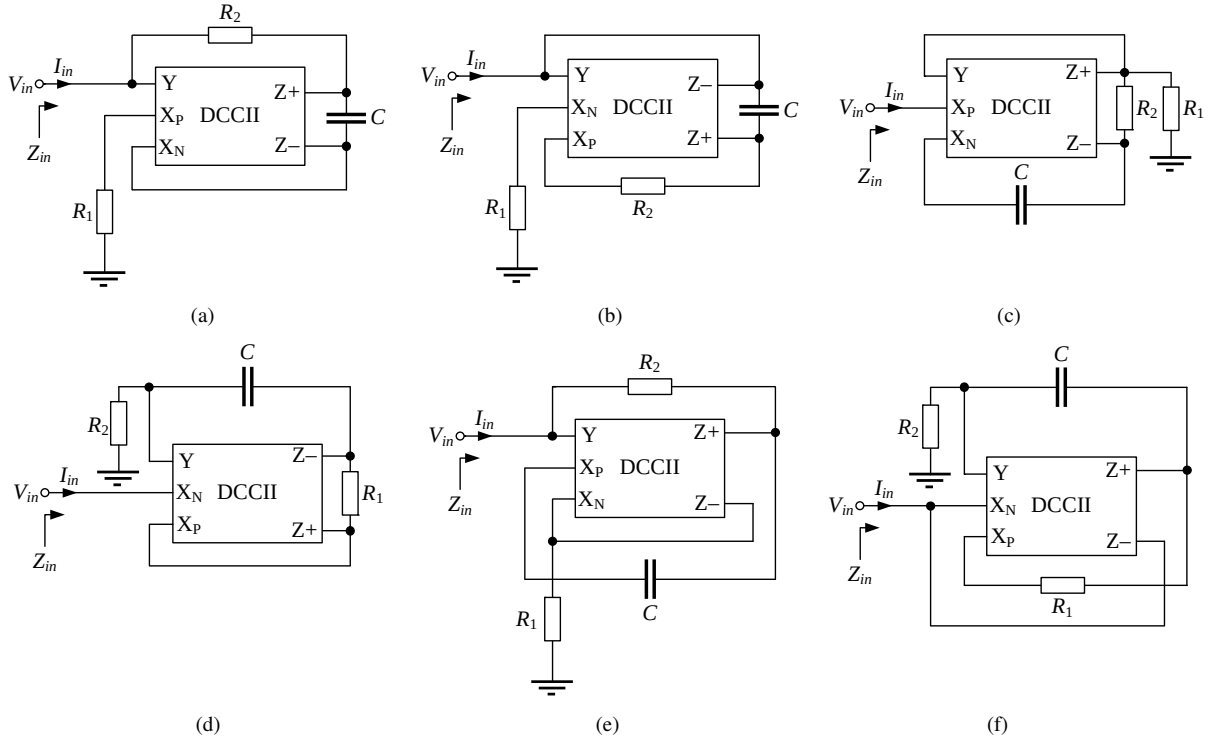

Fig. 2. Proposed lossless grounded inductance simulators using single DCCII.

$$Z_{in} = \frac{V_{in}}{I_{in}} = sL_{Eq} = sCR_1R_2. \quad (2)$$

Passive sensitivities of the proposed circuits are $|S^{L_{Eq}}_{R_1,\,R_2,\,C}| = 1$. In case of circuits shown in Figs. 2(c) and (e) the connected capacitor to the X-terminal of DCCII will affect circuit operation since it is in series with parasitic R_X, which is a disadvantage of these inductance simulator realizations. It is also worth noting that although each proposed circuit employs floating capacitor, but they can be realized easily with a current IC process that offers double poly (poly1-poly2) or metal-insulator-metal (MIM) capacitor [33].

3. Simulation Results

The CMOS implementation of the DCCII shown in Fig. 3 [26] was used to verify operation of the selected grounded inductance simulator. Unlike DCCII design that includes 21 transistors in [19], the DCCII in [26] uses 34 transistors. However, it has very high output impedance due to active feed-back cascade current mirrors. In Fig. 3, as explained in [26], the input currents i_{XN} and i_{XP} are applied to the drain of transistors M_{12} and M_{14}, respectively. The Y terminal voltage is applied to the gate of transistors M_2 and M_5. Because M_1, M_2, M_5, and M_6 are matched transistors; the voltage at Y terminal is conveyed to the terminals X_N and X_P. The difference between the X_P and X_N currents is conveyed to the Z terminals by the mirroring action of transistors M_{15}–M_{18} and M_{19}–M_{22}. Transistors M_{23}–M_{34} form the accurate active-feedback CMOS cascode current mirrors of the output stages. In the SPICE simulations TSMC 0.25 μm SCN025 CMOS process BSIM3v3.1 parameters were used [34]. The DC supply voltages used are $+V_{DD} = -V_{SS} = 1.25$ V and $V_b = 0.25$ V. The transistor aspect ratios are given in Tab. 2. The total power consumption of the DCCII is 22.8 mW.

Transistors	W(μm)/L(μm)	Transistors	W(μm)/L(μm)
$M_{1,2,5,6}$	50/0.5	Other PMOS	100/0.5
$M_{3,4,7,8}$	5/0.5	Other NMOS	10/0.5

Tab. 2. Aspect ratios of the MOS transistors in DCCII shown in Fig. 3.

Parameter	Value
Linearity v_{XN}/v_Y, v_{XP}/v_Y (V)	both –0.8 → +1.25
Linearity i_{Z+}/i_{XN}, i_{Z-}/i_{XP} (mA)	–0.8 → +0.9
Linearity i_{Z+}/i_{XP}, i_{Z-}/i_{XN} (mA)	–1.9 → +0.9
v_{XN}/v_Y, v_{XP}/v_Y gains (β_N, β_P)	both 1.007
i_{Z+}/i_{XN}, i_{Z-}/i_{XP} gain (α_N)	0.9645
i_{Z+}/i_{XP}, i_{Z-}/i_{XN} gain (α_P)	0.9885
v_{XN}/v_Y, v_{XP}/v_Y f_{-3dB} (GHz)	both 1.975
i_{Z+}/i_{XN}, i_{Z-}/i_{XP} f_{-3dB} (GHz)	2.099
i_{Z+}/i_{XP}, i_{Z-}/i_{XN} f_{-3dB} (GHz)	1.497

Tab. 3. Main parameters of the proposed DCCII given in Fig. 3.

The selected grounded inductance simulator from Fig. 2(d) was designed with the following passive element values: $R_1 = 4$ kΩ, $R_2 = 7.5$ kΩ, and $C = 10$ pF, which according to (2) corresponds to the value of the inductance of

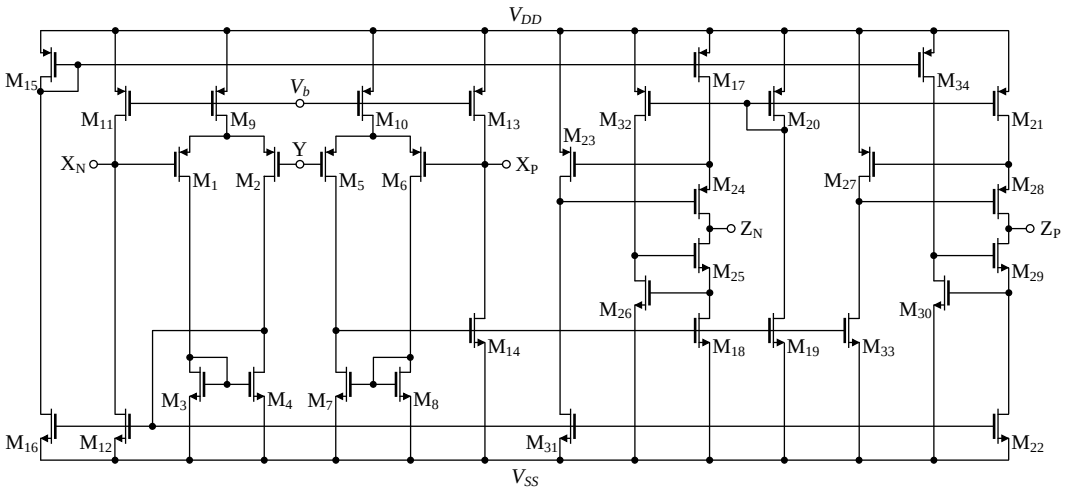

Fig. 3. A CMOS implementation of the DCCII [26].

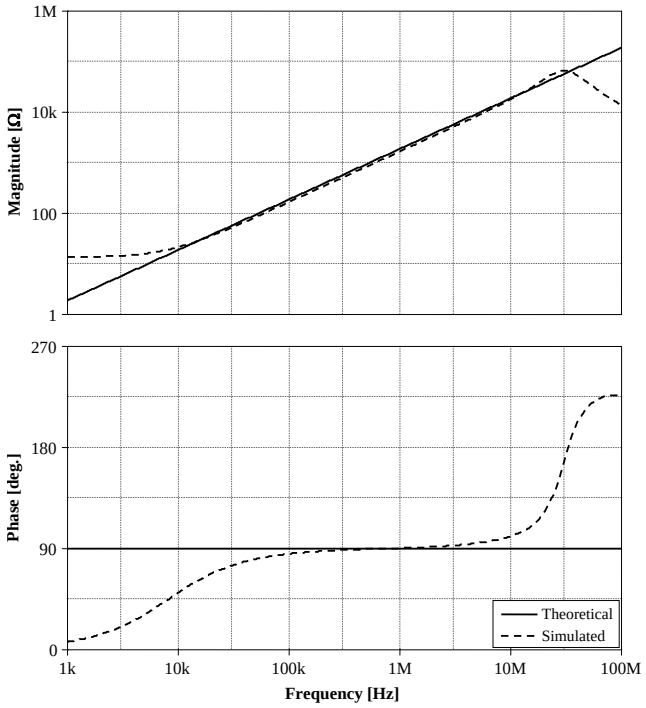

Fig. 4. Theoretical and simulated magnitude and phase responses of the impedance of the proposed lossless grounded inductance simulator shown in Fig. 2(d) relative to frequency for $L_{Eq} = 0.3$ mH.

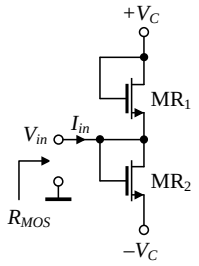

Fig. 5. Grounded resistor using two MOSFETs and two symmetrical power supplies [31], [32].

$L_{Eq} = 0.3$ mH. Note that capacitors with larger values than 10 pF are not practical because of the large substrate area consumed [35]. The theoretical and simulated magnitude and phase responses are shown in Fig. 4. As it can be seen from Fig. 4, the magnitude of impedance increases with the frequency and the useful frequency range for this circuit is approximately from 30 kHz to 10 MHz. Wider operating frequency range can be achieved using frequency improvement methods proposed in [36]–[38], where negative impedance converters (NICs) are with advantage used for eliminating the parasitic of simulated inductors and thus enhancing their frequency performance. As it can be seen from the referred equivalent inductor simulator circuits, the reduction of r_s effects is achieved by adding $-r_s$ in series connection, thus the low-frequency performance is improved considerably [36]–[38]. In the same way, $C'_p = C_p$ and $R'_p = R_p$ together with an additional NIC are used to improve high-frequency performance of the circuit.

All circuits in Fig. 2 have the advantage of employing grounded resistor, which can be replaced by two MOSFET-based VCR shown in Fig. 5 [31], [32] that resistance can be calculated as $R_{MOS} = V_{in}/I_{in} = L/[2\mu C_{OX} W(V_C - V_T)]$, where μ is carrier mobility, C_{OX} is the gate capacitance per unit area, V_T is threshold voltage, and W and L are the channel width and length, respectively. In simulations, W/L ratios of both MOSFETs were selected as $0.5\ \mu\text{m}/2\ \mu\text{m}$ while keeping values of R_1 and C given above. Fig. 6 shows impedance values relative to frequency of the circuit from Fig. 2(d) with three different values of control voltages V_C, while the controllability of L_{Eq} with respect to the control voltage V_C from 0.6 V to 1.8 V is shown in Fig. 7. Simulations confirmed that the simulated inductance can easily be adjusted by control voltage V_C from 2.1 mH to 0.34 mH.

The functionality of the proposed inductance simulator in Fig. 2(d) was tested on a 5$^{\text{th}}$-order high-pass LC passive ladder prototype shown in Fig. 8. In the design the passive elements were selected as $C_1 = C_2 = 5$ pF, $C_3 = 10$ pF, $R_L = 10$ kΩ, $R_S = 10$ kΩ, and synthetic inductors $L_{Eq1} = 400\ \mu$H,

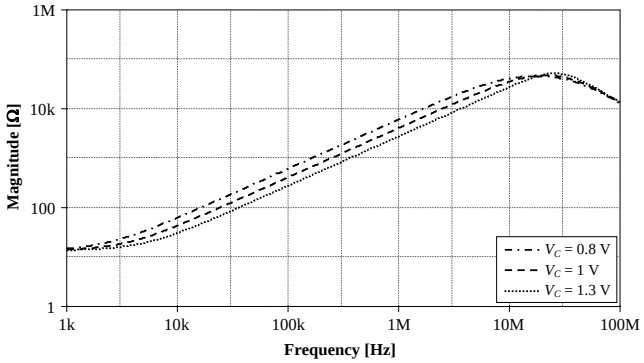

Fig. 6. Simulated magnitude responses of the impedance of the proposed lossless grounded inductance simulator shown in Fig. 2(d) relative to frequency for different V_C.

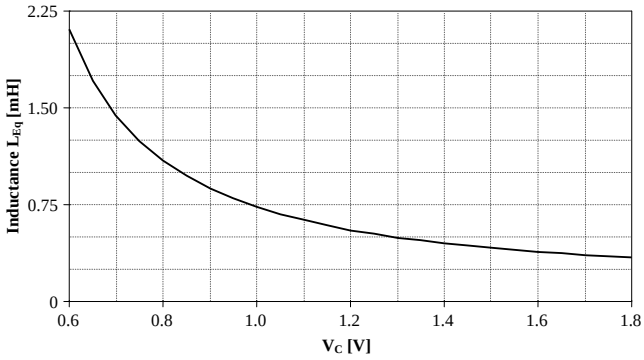

Fig. 7. Controllability of L_{Eq} with respect to the control voltage V_C.

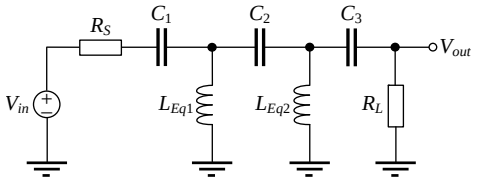

Fig. 8. 5th-order high-pass ladder filter prototype.

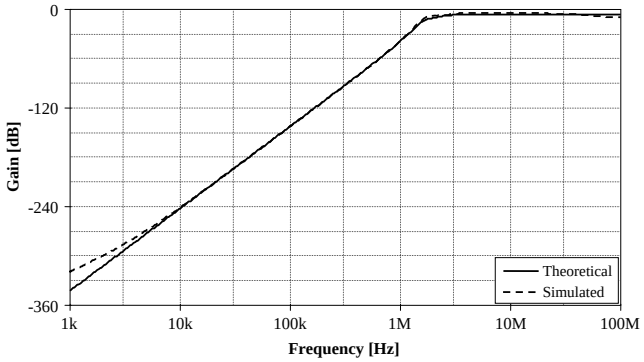

Fig. 9. Ideal and simulated frequency response of the 5th-order high-pass filter.

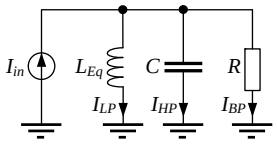

Fig. 10. Parallel resonant circuit prototype.

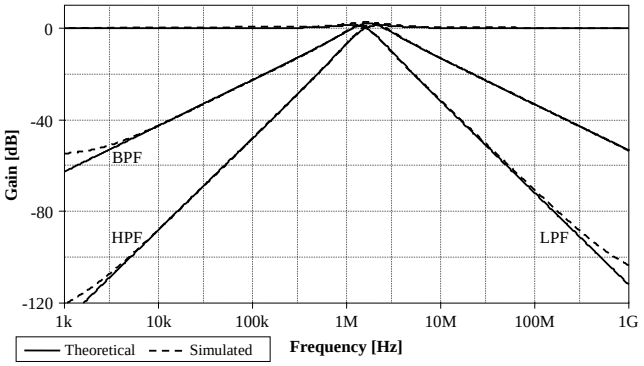

Fig. 11. Theoretical and simulated low-pass (LPF), high-pass (HPF), and band-pass (BPF) responses of the parallel resonant circuit.

$L_{Eq2} = 800\ \mu$H, which results in a cut-off frequency of 2.25 MHz. For the realization of L_{Eq1}, passive element values were chosen as $R_1 = 10$ kΩ, $R_2 = 40$ kΩ, and $C = 1$ pF while passive elements employed in L_{Eq2} had values $R_1 = 20$ kΩ, $R_2 = 40$ kΩ, and $C = 1$ pF. Both theoretical and simulated 5th-order high-pass ladder filter responses are shown in Fig. 9.

In addition, to show another application of the proposed inductance simulator a current-mode multifunction filter was designed and simulated. The basic cell is an inductor simulator L_{Eq} in parallel with a capacitor C and resistor R to form a resonant circuit as it is shown in Fig. 10. The resonant circuit is designed with element values: $C = 10$ pF, $R = 10$ kΩ, and $L_{Eq} = 1$ mH, which result in a pole frequency of $f_p \cong 1.59$ MHz. The L_{Eq} from Fig. 2(b) is composed by $R_1 = 20$ kΩ, $R_2 = 50$ kΩ, and $C = 1$ pF. Simulated low-pass (I_{LP}), high-pass (I_{HP}), and band-pass (I_{BP}) responses of the parallel resonant circuit are given in Fig. 11. The simulation results agree well with theoretical results.

4. Experimental Results

In addition to the simulations, in order to verify the above given theoretical analysis, the proposed inductor simulator in Fig. 2(d) is designed with passive element values of $R_1 = R_2 = 1$ kΩ, $C = 10$ nF. For the Butterworth high-pass filter prototype in Fig. 12, the passive element values are selected as $R_L = R_S = 1$ kΩ and $C_2 = 10$ nF, which are fabricated with 10 % tolerances. The cut-off frequency is 11.22 kHz. The DCCII is designed with the commercially available AD844/ADs of Analog Devices with supply voltages of $V_{DD} = +15$ V and $V_{SS} = -15$ V [39]. A sine waveform with a peak-to-peak voltage of 1.2 V is applied to the

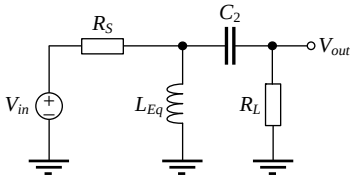

Fig. 12. 2nd-order high-pass Butterworth ladder filter prototype used in the experiment.

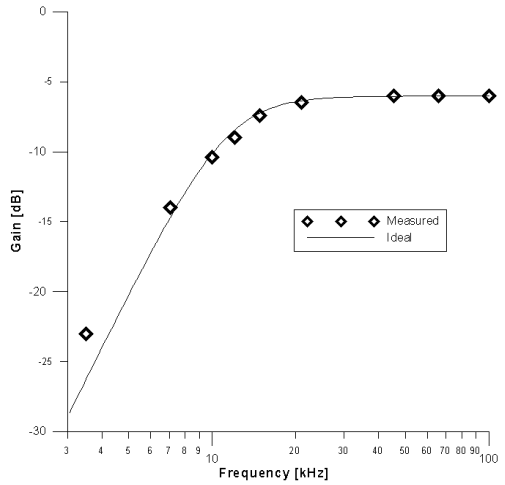

Fig. 13. Experimental results: Ideal and measured frequency responses of the 2nd-order Butterworth high-pass filter.

filter constructed with above mentioned passive element values. Theoretical and measurement data of the frequency responses are depicted in Fig. 13. The experimental results quite agree with theoretical results.

5. Conclusions

DCCII is an active element that combines features of current differencing unit and CCII. In this paper, we emphasized advantage of DCCII presenting six novel grounded inductor simulator topologies. The proposed circuits use minimum number of elements and do not have the element matching restriction. The performance of the selected inductor simulator was tested in 5th-order high-pass LC passive ladder prototype, in LCR parallel resonant circuit, and in high-pass filter prototype. Simulation and experimental results well confirm the theoretical analysis.

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