Maximum Bandwidth Enhancement of Current Mirror using Series-Resistor and Dynamic Body Bias Technique

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Abstract. *This paper introduces a new approach for enhancing the bandwidth of a low voltage CMOS current mirror. The proposed approach is based on utilizing body effect in a MOS transistor by connecting its gate and bulk terminals together for signal input. This results in boosting the effective transconductance of MOS transistor along with reduction of the threshold voltage. The proposed approach does not affect the DC gain of the current mirror. We demonstrate that the proposed approach features compatibility with widely used series-resistor technique for enhancing the current mirror bandwidth and both techniques have been employed simultaneously for maximum bandwidth enhancement. An important consequence of using both techniques simultaneously is the reduction of the series-resistor value for achieving the same bandwidth. This reduction in value is very attractive because a smaller resistor results in smaller chip area and less noise. PSpice simulation results using 180 nm CMOS technology from TSMC are included to prove the unique results. The proposed current mirror operates at 1 Volt consuming only 102 μW and maximum bandwidth extension ratio of 1.85 has been obtained using the proposed approach. Simulation results are in good agreement with analytical predictions.*

Keywords

Body effect, dynamic body bias, cascode current mirror, low voltage, high bandwidth, low power.

1. Introduction

The current mirrors (CM) are most commonly used in signal processing and conditioning analog circuits. Low voltage current mirrors having simple circuitry are very attractive for analog integrated circuit applications where large bandwidth and low power consumption are required. The current design trend of industry to reduce the supply voltage to sub-volt supplies and minimum gate size, places challenge to analog circuit designers. The shrinking sizes of semiconductor devices in CMOS technology entail the simultaneous reduction of supply voltage and threshold voltage of MOS transistor. Since the threshold voltage of a MOS transistor is not reduced at the same rate as the power supply, it becomes increasingly difficult to design wideband current mirror circuits because of the reduced voltage headroom. Analog signal processing circuits now operating from single 1.5 V supplies and dropping, are constantly demanding higher bandwidth and speed performances of current mirrors. The current mirror bandwidth performance degrades as power supply voltage is reduced. For a given bias point, the DC accuracy requirement fixes the power-speed ratio of the current mirror circuit and the tradeoff between the bandwidth, the accuracy and the power consumption is set by technology constants [1], [2].

Various techniques have been reported for bandwidth extension of low voltage current mirrors [3–8]. Throughout the bibliography many references [9–13] can be found considering series-resistor technique [3]. This technique improves the bandwidth of a current mirror by inserting a series-resistor between the gates of the primary pair transistors of current mirror. By appropriately choosing the resistor value, zero cancels a dominant pole thereby enhancing current mirror's bandwidth. The added resistor however increases the overall noise of the circuit owing to the additional thermal noise. Also, bandwidth enhancement is much smaller if the current gain is large. Hence this technique is not suitable for low noise high frequency applications. For full monolithic integration, resistor can be made of polysilicon or a diffusion resistor. The main drawback of integrated resistor is the large tolerance of its absolute values. Even with mature process, the passive and active components can have more than 10% variations. Although a MOS transistor can be used for active implementation of series-resistor but this results in penalty of extra power consumption and increase in chip area. Under very low supply voltages, the reduction of voltage headroom poses an important limitation on the power consumption in additional passive component/circuitry for improving bandwidth. Hence other techniques must be investigated.

In this work, we have proposed a new approach for bandwidth enhancement of a low voltage CMOS current mirror. The proposed approach is based on boosting the transconductance of a MOS transistor using dynamic body bias technique, while maintaining low power consumption. This approach also results in reduction of threshold voltage

(V_{TH}) of MOS transistor utilizing body effect. We have used the proposed approach along with series-resistor technique in a low voltage cascode current mirror circuit for maximum bandwidth enhancement. The parasitic resistance and capacitance due to dynamic body biasing introduces a zero in the transfer function of the proposed current mirror. This zero cancels one of the poles thereby enhancing the bandwidth of the proposed current mirror.

The dynamic body bias technique is implemented using triple well CMOS technology which is compatible with standard CMOS process. Triple well process can be achieved at the slightly higher cost process but without increase in any chip area. A triple well structure reduces the cross-talk in mixed systems-on-chip designs and is more robust to process and well junction capacitance variations [14]. The paper is organized as follows: Section 2 introduces conventional current mirror where series-resistor technique has been used for enhancing its bandwidth. Section 3 introduces dynamic body bias technique and circuit implementation of proposed current mirror. Bandwidth analysis is carried out using small signal analysis to predict its maximum theoretical bandwidth. Simulation results are presented in Section 4. Conclusions are summarized in Section 5.

2. Conventional Current Mirror

In modern sub-micron CMOS process the g_m/g_{ds} ratio is less than 100 and consequently a significant gain error results when more of the current amplifier stages are cascaded. This gain error is usually reduced by increasing the output impedance using different cascode topologies [15]. Fig. 1 shows a low voltage cascode current mirror. Here, the input voltage (V_{in}) depends solely on the biasing conditions of M1 and minimum V_{in} required to pump input current (I_{in}) into the input port of the mirror is given as [16].

$$V_{inmin} = V_{TH1} . \tag{1}$$

The other important factors that establish its capability to operate in a low-voltage environment are the minimum supply voltage and output voltage given by the following expressions

$$V_{DDmin} = V_{TH1} + V_{DSsat5} , \tag{2}$$

$$V_{outmin} = V_{DSsat2} + V_{DSsat3} . \tag{3}$$

Transistors M2 and M3 form output transistor cascode pair and due to the independent biasing of the transistor M3, provided by M4, the output voltage swing is not affected. Hence the output impedance of the structure can be increased to have high gain structures at low voltage levels. The input resistance of the mirror is decided by the transconductance (g_{m1}) of M1.The expression for input and output resistances is given as

$$R_{in} \cong \frac{1}{g_{m1}} , \tag{4}$$

$$R_{out} \cong g_{m3} . r_{o2} . r_{o3} . \tag{5}$$

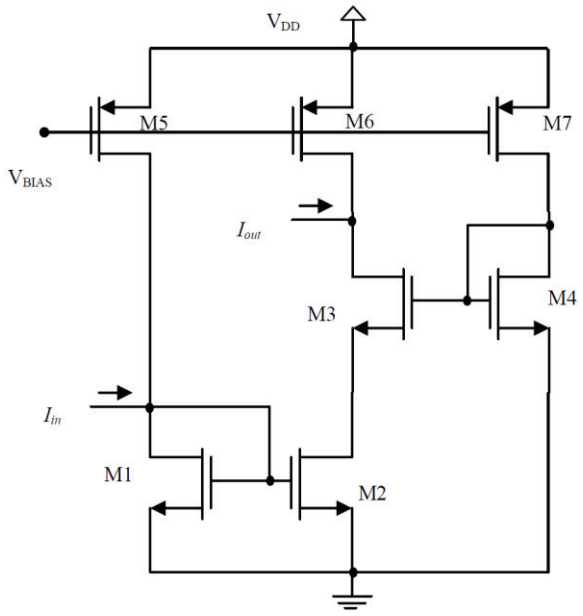

Fig. 1. Low voltage cascode current mirror.

Cascode current mirror suppress the effect of channel-length modulation and improves input-output isolation as there is no direct coupling from the output to input. The simple circuit structure of current mirror in Fig. 1 ensures a higher bandwidth. Its DC gain and -3dB frequency is given by the following expression [13]

$$Gain = \frac{g_{m2}}{g_{m1}} , \tag{6}$$

$$\omega_0 = \sqrt{\frac{g_{m1}(g_{m3})}{2\, C_{gs1} C_{gs3}}} . \tag{7}$$

From (7) we observe that the ratio between gate transconductance and gate-to-source capacitance of a MOS transistor dominates the frequency behavior. Thus g_m and C_{gs} are the main parameters that have major influence over the current mirror bandwidth.

The series-resistor technique to improve the bandwidth performance of low voltage cascode current mirror is shown in Fig. 2. Henceforth throughout this paper, we have considered current mirror in Fig. 2 as conventional current mirror under study. The introduction of R to the primary pair transistors of the current mirror results in a zero which cancels one of the poles when $R = 1/g_{m1}$ is selected, thereby enhancing its bandwidth. The expressions for DC gain and -3dB frequency is given as [13]

$$Gain_{CCM} = \frac{g_{m2}}{g_{m1}} , \tag{8}$$

$$\omega_{0,CCM} = \sqrt{\frac{g_{m1}(g_{m3})}{C_{gs1} C_{gs3}}} . \tag{9}$$

Comparing (7) and (9) we obtain

$$\omega_{0,CCM} = \sqrt{2}\, \omega_0 . \tag{10}$$

Thus from (6), (8) and (9), it is evident that series-resistor technique enhances the bandwidth by factor $\sqrt{2}$ without compromising DC gain.

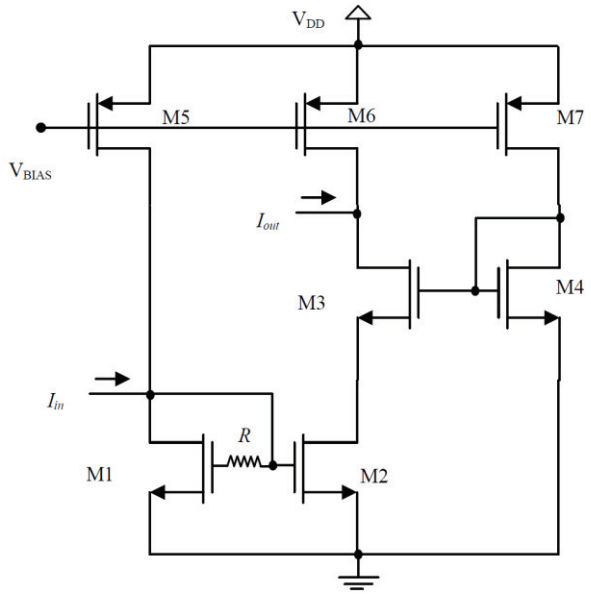

Fig. 2. Conventional current mirror.

We observe from Fig. 2 that in conventional CM, M3 suffers from body effect. In most of the current mirror analysis, generally body effect is neglected either for the sake of simplicity or due to its negligible effect, at higher power supply voltage. Some inaccuracy nevertheless arises due to the body effect present in a MOS transistor. Due to body effect, the ideal square-law behavior of MOS transistor in saturation region of operation approaches more closely to an ideal linear transfer function. As a result, high-order harmonics introduced to the drain current expression results in an error in its transconductance [17]. Due to this effect, there is non-negligible attenuation, which may not be neglected in the submicron circuits operating at low power supply voltage.

With the progressive reduction of MOS transistors minimum dimension and their associated supply voltages, use of body effect is becoming an attractive opportunity for improving the performance of low voltage analog integrated circuits [18]. In this paper we have utilized body effect in M3 using dynamic body bias technique for improving bandwidth and output resistance of conventional CM.

3. Proposed Current Mirror

In this section, we have briefly discussed dynamic body bias technique and a small signal model of MOS transistor biased with this technique is proposed. The circuit implementation of proposed current mirror using dynamic body biasing is suggested. Bandwidth analysis of proposed CM shows that the dynamic body bias technique has enhanced its bandwidth and output resistance.

3.1 Dynamic Body Bias Technique

For low voltage low power design, various techniques have been reported in the literature to overcome the difficulties introduced by the relatively high threshold voltage of a MOS transistor. One such reported technique in literature is bulk-driven technique, where input signal is applied at body/bulk terminal instead of gate terminal, after biasing the gate terminal to a sufficient voltage; thus the threshold voltage in this setup is removed from signal path. Unfortunately, the transconductance of a bulk-driven MOS transistor is substantially smaller and the equivalent input referred noise is higher than that of a conventional gate-driven MOS transistor, which may result in lower gain bandwidth and worse frequency response [19]. Another circuit technique which provides an important solution to the threshold voltage scaling limitation is body bias technique, which modulates the threshold voltage of a MOS transistor electronically using body effect, without any technology modification. Body effect enables a variety of effective body bias techniques [20].

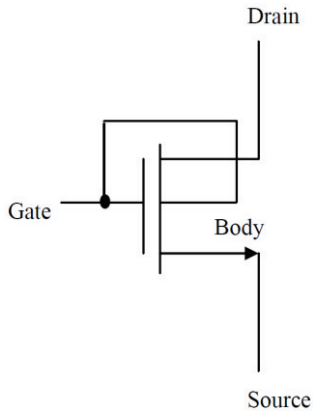

Fig. 3. MOS transistor using dynamic body bias technique.

In this work, our proposed approach is based on using both bulk/body and gate terminals of a MOS transistor as signal input. This concept, first presented in [21] is shown in Fig. 3. Due to gate and body terminals shorted together, threshold voltage (V_{TH}) of the transistor becomes function of input signal. With change in input, bias voltage at body terminal also changes dynamically as input changes hence known as dynamic body bias technique. The relation between input signal and V_{TH} is described using the following equation [22]

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{\psi_s + V_{SB}} - \sqrt{\psi_s}\right). \qquad (11)$$

where V_{TH} is threshold voltage due to body effect i.e. applied V_{SB} , V_{TH0} is the threshold voltage when V_{SB} is zero and mainly depends on the manufacturing process. γ is typically equal to 0.4 $V^{0.5}$ and depends on the gate oxide capacitance, silicon permittivity, doping level and other parameters. ψ_s is surface potential in strong inversion and typically is 0.6 V. ψ_s in (11) is assumed to $|\ 2\Phi_F\ |$, where Φ_F is Fermi potential.

In dynamic body bias technique, $V_{GS} = V_{BS}$ is maintained all the time and same bias voltage is applied at gate and body terminals. Here source-body junction gets slightly forward biased when input signal increases. Although source-body junction parasitic diode is slightly forward biased but any substantial conducting pn junction current is

absent as V_{TH} decreases due to the body effect as predicted by (11). The potential in the channel region is strongly controlled by the gate and body terminals, leading to a high transconductance owing to faster current transport.

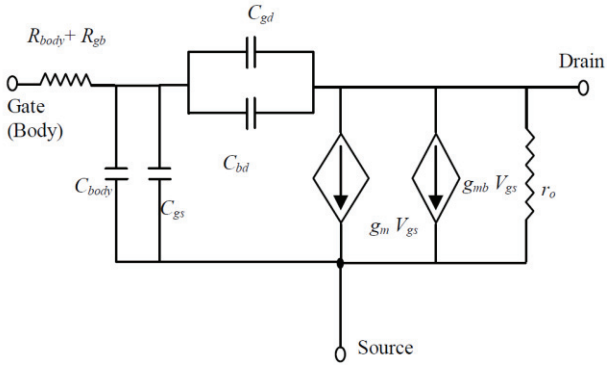

Fig. 4. Proposed small signal model of MOS transistor using dynamic body bias technique.

The proposed small signal equivalent circuit of MOS transistor using dynamic body biasing is shown in Fig. 4. It has two transconductances, the gate transconductance g_m and body transconductance g_{mb}. The relation between both transconductances is [22]

$$\frac{g_{mb}}{g_m} = \eta \approx (0.2 - 0.4) \tag{12}$$

where η is the specific parameter and its value depends on bias conditions and on the technology used. Dynamic body bias increases the effective transconductance from g_m to $(g_m + g_{mb})$ as $V_{SB} = V_{GS}$ is maintained all the time and both transconductance contributes to the conduction current. The effective transconductance is obtained as

$$g_{m,eff} = g_m(1 + \eta)\ . \tag{13}$$

Due to higher effective transconductance, the input referred noise power spectral density is also reduced, defined as

$$v_{noise}^2(f) = \frac{i_{ni}^2}{(g_m + g_{mb})^2} \tag{14}$$

where i^2_{ni} is the total drain current generated by noise sources.

The bulk of a MOS transistor has finite resistance and additional parasitic capacitance. The effective input capacitance from Fig. 4 is defined as

$$C_{eff} \approx C_{gs} + C_{body} \tag{15}$$

where C_{body} is body capacitance and C_{gs} is gate capacitance. The effective input resistance from Fig. 4 is defined as

$$R_{eff} \approx R_{gb} + R_{body} \tag{16}$$

where R_{gb} is gate-body contact resistance and R_{body} is bulk/body resistance.

Dynamic body bias technique is implemented using triple well CMOS technology hence latch-up is absent. This technique exhibits merits over other body bias techniques in terms of higher transconductance-to-drain current ratio and elimination of additional circuitry for bias voltage generation.

3.2 Circuit Implementation

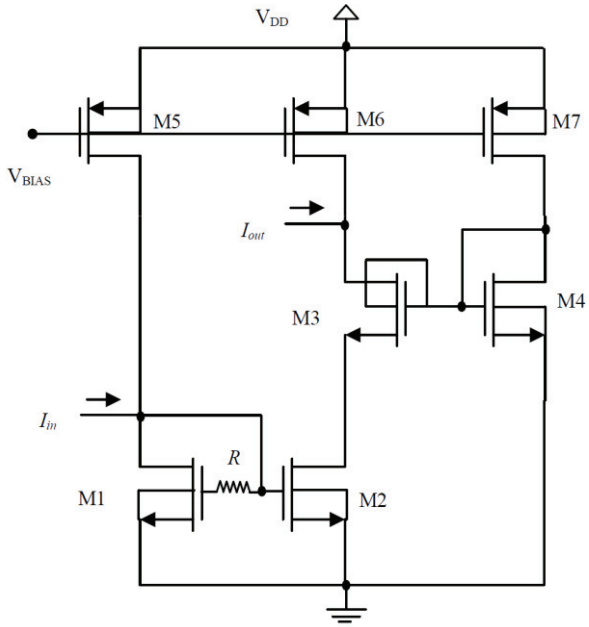

Fig. 5. Proposed current mirror.

The current mirrors using MOS transistors operating in saturation mode have higher transconductance than those based on MOS transistors operating in triode or sub-threshold mode. This leads to higher bandwidth and better input and output impedances. A convenient way to bring MOS transistor into saturation is by using body effect [23]. Fig. 5 shows the circuit implementation of proposed CM in which we have applied dynamic body bias technique in M3 and thus for any variation in load, M3 always remains in saturation, utilizing body effect. For remaining transistors, body and source terminals are connected together.

A current mirror may be characterized as having output impedance which affects the accuracy of the current replicated in the current mirror. High output impedance in current mirrors is required for accurate replication of currents. It can be seen from (4), (5) and (13) that due to dynamic body bias in M3, input resistance of proposed CM remains unaffected whereas output resistance is increased, given as

$$R_{out} \cong g_{eff}\,.\,r_{o2}.\,r_{o3}\ . \tag{17}$$

3.3 Bandwidth Analysis

The small signal model for bandwidth calculation of proposed CM is shown in Fig. 6. In the small signal analysis of proposed current mirror, short channel effects like drain-induced barrier lowering, hot carriers effects, velocity saturation are neglected for the sake of simplicity of hand calculations with the goal to give an idea on the order of magnitude of bandwidth improvement rather than finding

an exact value. The notations used in the analysis are as follows: C_{gsi} is gate-source capacitance, V_{gsi} is gate-source voltage and g_{mi} is gate transconductance for Mi where i = 1 to 4. Here, g_{mb3} is body transconductance, C_{eff} is total input capacitance and R_{eff} is total input resistance of M3. R is series-resistor between gates of M1 and M2.

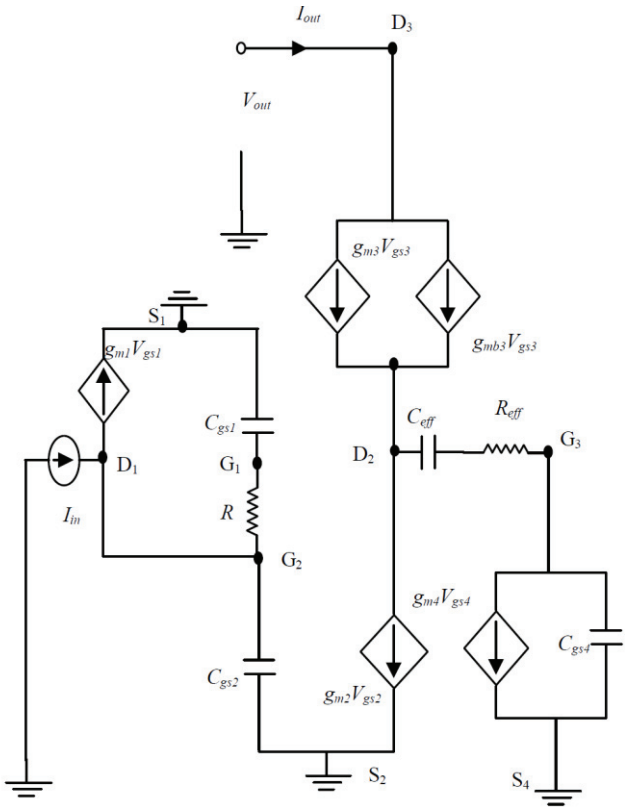

Fig. 6. Small signal model for calculating bandwidth of proposed CM.

Neglecting output conductance and capacitance in Fig. 6, equation for node D1 is given as

$$I_{in}(s) = g_{m1}V_{gs1} + s\,C_{gs2}V_{G2} + \frac{V_{G2}-V_{G1}}{R}\,. \tag{18}$$

Since both R and C_{gs1} are in series we get

$$\frac{V_{G2}-V_{G1}}{R} = V_{G1}s\,C_{gs1}\,. \tag{19}$$

Simplifying (19) we get

$$V_{G1} = \frac{V_{G2}}{(1+sRC_{gs1})}\,. \tag{20}$$

Substituting (19) in (18) we get

$$I_{in}(s) = V_{G1}\left(g_{m1} + s\,C_{gs1}\right) + s\,C_{gs2}V_{G2}\,. \tag{21}$$

Substituting (20) in (21) we get

$$V_{G2} = V_{gs2} = I_{in}(s)\left[\frac{(1+sRC_{gs1})}{g_{m1}+s\,C_{gs1}+s\,C_{gs2}(1+sRC_{gs1})}\right] \tag{22}$$

Writing equation at node S3

$$g_{m2}V_{gs2} = (g_{m3}+g_{mb3})V_{gs3} + \frac{V_{gs3}}{R_{eff}+\frac{1}{sC_{eff}}} \tag{23}$$

Because of mirror action $V_{gs1} = V_{gs2}$ and substituting (22) in (23) we get

$$I_{in}(s)\left[\frac{g_{m2}(1+sRC_{gs1})}{g_{m1}+s\,C_{gs1}+s\,C_{gs2}(1+sRC_{gs1})}\right] = \left(g_{m3}+g_{mb3} + \frac{1}{R_{eff}+\frac{1}{sC_{eff}}}\right)V_{gs3} \tag{24}$$

Writing equation for node D3 we get

$$I_{out}(s) = g_{m3}V_{gs3} + g_{mb3}V_{gs3}\,. \tag{25}$$

Simplifying (25) we get

$$V_{gs3} = \frac{I_{out}(s)}{g_{m3}+g_{mb3}}\,. \tag{26}$$

Substituting (26) in (24) we obtain transfer function as

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{g_{m2}(1+sRC_{gs1})(g_{m3}+g_{mb3})}{\left[\,g_{m1}+s\,C_{gs1}+s\,C_{gs2}(1+sRC_{gs1})\right]\left(g_{m3}+g_{mb3}+\frac{1}{R_{eff}+\frac{1}{sC_{eff}}}\right)} \tag{27}$$

Simplifying and rearranging (27) we get

$$\frac{I_{out}(s)}{I_{in}(s)} = \left[\frac{g_{m2}(g_{m3}+g_{mb3})\,RC_{gs1}\left(s+\frac{1}{RC_{gs1}}\right)}{RC_{gs1}C_{gs2}\left\{s^2+s\left(\frac{C_{gs1}+C_{gs2}}{RC_{gs1}C_{gs2}}\right)+\frac{g_{m1}}{RC_{gs1}C_{gs2}}\right\}}\right] \times \left[\frac{R_{eff}C_{eff}\left(s+\frac{1}{R_{eff}C_{eff}}\right)}{\{C_{eff}+R_{eff}C_{eff}(g_{m3}+g_{mb3})\}\left[s+\frac{g_{m3}+g_{mb3}}{C_{eff}+R_{eff}C_{eff}(g_{m3}+g_{mb3})}\right]}\right]. \tag{28}$$

Assuming M1 and M2 to be matched and substituting $C_{gs1} = C_{gs2}$ in (28), we get

$$\frac{I_{out}(s)}{I_{in}(s)} = \left[\frac{g_{m2}(g_{m3}+g_{mb3})\,RC_{gs1}\left(s+\frac{1}{RC_{gs1}}\right)}{RC_{gs1}{}^2\left\{s+\frac{1}{RC_{gs1}}\right\}^2}\right] \times \left[\frac{R_{eff}C_{eff}\left(s+\frac{1}{R_{eff}C_{eff}}\right)}{\{C_{eff}+R_{eff}C_{eff}(g_{m3}+g_{mb3})\}\left[s+\frac{g_{m3}+g_{mb3}}{C_{eff}+R_{eff}C_{eff}(g_{m3}+g_{mb3})}\right]}\right] \tag{29}$$

We observe from (29) that the introduction of R in the circuit has resulted in a zero at Z_R = -1/ RC_{gs1} and dynamic body bias technique has resulted in a zero at Z= -1/ R_{eff} C_{eff}.

Substituting $R = 1/g_{m1}$ in (29) then zero cancels one of the poles and simplified transfer function is written as

$$\frac{I_{out}(s)}{I_{in}(s)} = \left[\frac{g_{m2}(g_{m3}+g_{mb3})}{C_{gs1}\left(s+\frac{g_{m1}}{C_{gs1}}\right)}\right] \times \left[\frac{R_{eff}\left(s+\frac{1}{R_{eff}C_{eff}}\right)}{\{1+R_{eff}(g_{m3}+g_{mb3})\}\left[s+\frac{g_{m3}+g_{mb3}}{C_{eff}\{1+R_{eff}(g_{m3}+g_{mb3})\}}\right]}\right]. \tag{30}$$

Assuming $R_{eff}(g_{m3}+g_{mb3}) >> 1$, (30) can be further simplified as

$$\frac{I_{out}(s)}{I_{in}(s)} = \left[\frac{g_{m2}(g_{m3}+g_{mb3})}{C_{gs1}\left(s+\frac{g_{m1}}{C_{gs1}}\right)}\right]\left[\frac{\left(s+\frac{1}{R_{eff}C_{eff}}\right)}{(g_{m3}+g_{mb3})\left(s+\frac{1}{R_{eff}C_{eff}}\right)}\right]. \quad (31)$$

We observe from (31) that zero cancels one of the poles and transfer function becomes

$$\frac{I_{out}(s)}{I_{in}(s)} = \left(\frac{g_{m2}}{g_{m1}}\right)\frac{\frac{g_{m1}}{C_{gs1}}}{\left(s+\frac{g_{m1}}{C_{gs1}}\right)}. \quad (32)$$

Comparing (32) with standard equation of first order transfer function given as

$$T(s) = \frac{K}{1+\frac{s}{\omega_0}} \quad (33)$$

where ω_0 is -3dB frequency. DC gain and -3dB frequency of proposed CM is obtained as

$$Gain_{PCM} = \frac{g_{m2}}{g_{m1}}, \quad (34)$$

$$\omega_{0,PCM} = \frac{g_{m1}}{C_{gs1}}. \quad (35)$$

On the basis of analytical predictions for bandwidth from (35) and comparing it with (9), it is observed that the proposed approach enhances the bandwidth of current mirror. It is evident from the analysis that the bandwidth enhancement mechanism of dynamic body bias technique and series-resistor techniques differs fundamentally. This suggests that both techniques can be employed simultaneously for maximum bandwidth enhancement. From (5) and (17) we see that output resistance is also improved using the proposed approach as effective transconductance of M3 has increased. The dynamic body bias technique does not affect the current mirror's DC gain as evident from (8) and (34).

4. Simulation Results

Conventional current mirror in Fig. 2 and proposed current mirror in Fig. 5 have been designed in 180 nm CMOS technology from TSMC. The current mirror (CM) circuits have been simulated at V_{DD} = 1 V and V_{BIAS} = 0.35 V. All the transistors have the same channel length L = 180 nm and width parameters are given in Tab. 1.

MOS transistor	Type	W(µm)
M1	NMOS	8.3
M2,M3	NMOS	9
M4	NMOS	0.36
M5	PMOS	0.36
M6,M7	PMOS	9

Tab. 1. Width parameters for various transistors.

Fig. 7 shows simulated frequency response of conventional and proposed current mirror for R = 1 kΩ. -3dB frequency of conventional CM and proposed CM is obtained as 344.224 MHz and 538.987 MHz respectively with 0 dB peaking. Thus dynamic body bias technique boosts the bandwidth by a factor of 1.56 (R = 1 kΩ). Fig. 8 shows transfer characteristics. The approx. range of proposed CM is 0 to 250 µA. The simulated static power consumption of proposed CM is 0.102e-4 W.

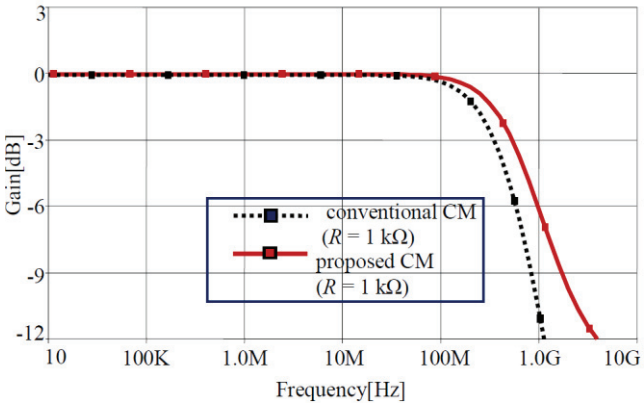

Fig. 7. Frequency response of conventional and proposed current mirror.

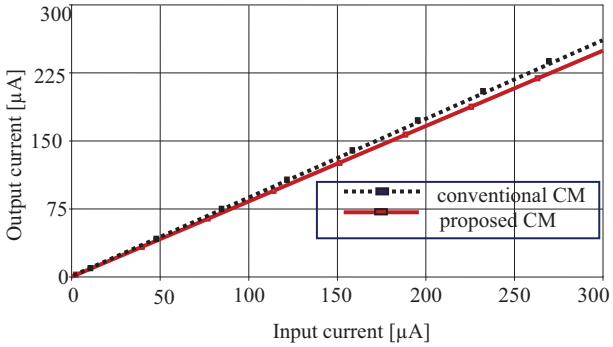

Fig. 8. Transfer characteristics of proposed current mirror.

The parasitic capacitances in CMOS circuits introduce zeros which results in peaks in frequency response. To maximize the bandwidth and avoid ringing in time domain response, the series-resistor is sized based on the criterion of the critical damping. Fig. 9 shows frequency behavior of conventional CM when R is varied from 1 kΩ to 60 kΩ, detailed in Tab. 2.

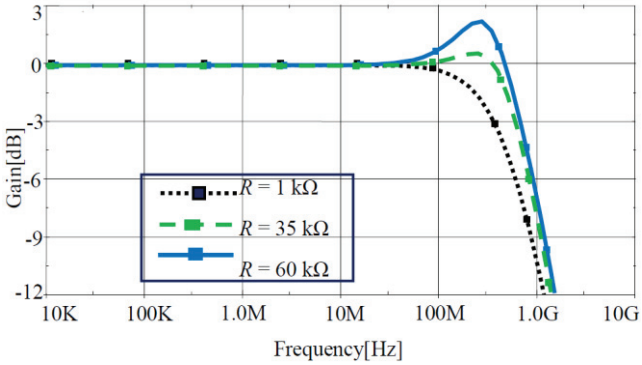

Fig. 9. Variation in frequency response of conventional current mirror with R.

R (kΩ)	Conventional CM (MHz)	Peaking (dB)	Proposed CM (MHz)	Peaking (dB)	BWER (bandwidth extension ratio)
1	344.224	0	538.987	0	1.565
5	370.186	0	608.429	0	1.643
10	417.881	0	765.741	0	1.832
15	471.719	0	875.195	0	1.855
20	526.081	0	941.204	0.245	1.789
25	565.759	0	964.296	0.766	1.704
30	586.706	0.221	976.053	1.263	1.663
35	601.100	0.580	976.053	1.727	1.623
40	608.429	0.961	976.053	2.148	1.604
45	615.848	1.331	976.053	2.528	1.585
50	615.848	1.658	976.053	2.835	1.585
55	615.848	1.947	976.053	>3	1.585
60	615.848	2.216	976.053	>3	1.585

Tab. 2. Comparison of -3dB frequency of conventional and proposed current mirror(CM) for different values of *R*.

It is observed from the table that the bandwidth increases as value of R increases and there is no peaking in frequency response up to $R = 25$ kΩ. The maximum bandwidth obtained without peaking and with peaking for conventional CM is 565.759 MHz and 615.848 MHz respectively.

Fig. 10 shows frequency behavior of proposed CM when R is varied from 1 kΩ to 50 kΩ, detailed in Tab. 2. It is observed from the table that the bandwidth increases as value of R increases and there is no peaking in frequency response up to $R = 15$ kΩ. The maximum bandwidth obtained without peaking and with peaking for proposed CM is 875.195 MHz and 976.053 MHz respectively.

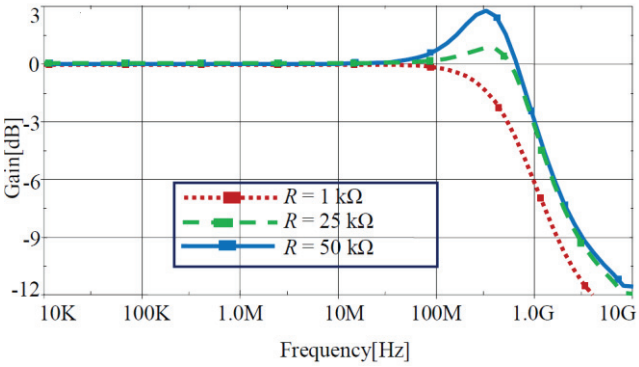

Fig. 10. Variation in frequency response of proposed current mirror with *R*.

It is seen from Tab. 2 that about 600 MHz bandwidth in conventional CM is obtained when $R = 45$ kΩ is used. In proposed CM the same bandwidth of about 600 MHz is achieved for $R = 5$ kΩ only. This reduction in value of R is very attractive because a smaller resistor results in smaller chip area and less noise. Further resistors with a smaller parasitic capacitance, such as non-silicide poly resistors, may be preferred over diffusion resistors for reducing peaking and achieving higher bandwidth.

It is observed from Tab. 2 that maximum bandwidth which can be achieved using dynamic body bias technique, without peaking, in the proposed CM is 875.195 MHz for $R = 15$ kΩ. For conventional CM, bandwidth of 471.719 MHz is obtained for $R = 15$ kΩ. Thus maximum BWER of 1.85 is obtained using dynamic body bias technique without peaking.

A current mirror having excellent static performance is more preferable for biasing applications. For signal processing applications, current mirrors lie along the signal path of a circuit and must have good dynamic performance. Fig. 11 shows simulated responses of the proposed and conventional current mirror to a step change in I_{in} from 25 µA to 175 µA. From this plot, it is evident that the step response of the proposed CM is much faster than that of the conventional CM.

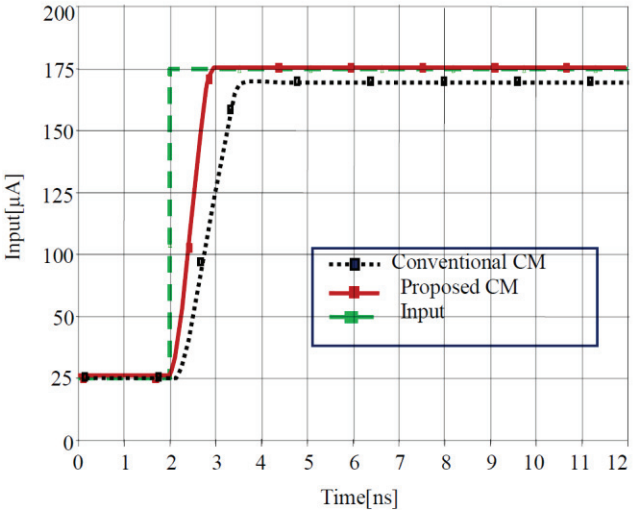

Fig. 11. Transient response of proposed current mirror.

Fig. 12 shows simulated frequency response of CM in Fig. 1, i.e. without any bandwidth extension technique and -3dB frequency of 340.341 MHz is obtained.

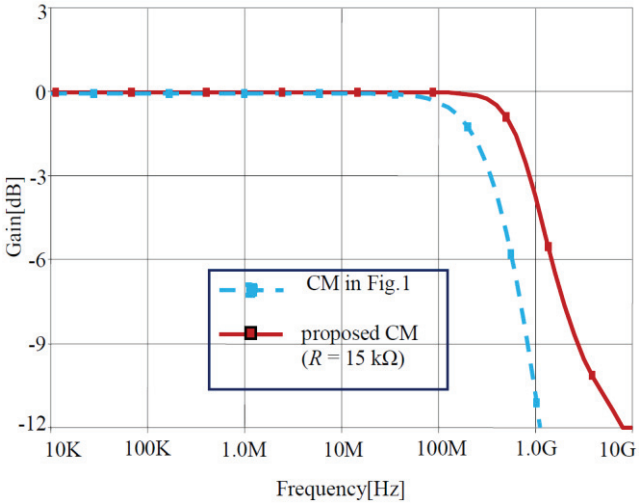

Fig. 12. Frequency response of proposed current mirror and current mirror (Fig. 1) without any bandwidth extension technique.

Tab. 4 compares the bandwidth extension ratio (BWER) achieved using series-resistor technique and combination of series resistor and dynamic body bias technique for $R = 15$ kΩ, without peaking (as observed in Tab. 2). It

is evident from Tab. 4 that BWER of 1.38 is obtained using series-resistor technique and BWER of 2.57 is obtained when both dynamic body bias technique and series-resistor technique are used simultaneously in low voltage cascode current mirror shown in Fig. 1.

Parameters	Conventional current mirror (Fig. 2)	Proposed current mirror(Fig. 5)
Supply voltage (V)	1	1
CMOS technology (nm)	180	180
Simulated maximum bandwidth without peaking (MHz)	565.759 (for R = 25 kΩ)	875.195 (for R = 15 kΩ)
Range (μA)	262	250
Input resistance (kΩ)	1.381	1.381
Output resistance (kΩ)	561.382	817.331
Power dissipation (W)	0.104e-4	0.102e-4

Tab. 3. Comparison of simulated parameters for conventional and proposed current mirror.

Parameter	Current mirror in Fig. 1	Bandwidth extension using only series-resistor technique (Fig. 2)	Bandwidth extension using both dynamic body bias technique and series-resistor technique simultaneously (Fig. 5)
-3dB frequency (MHz)	340.341	471.719	875.195
BWER obtained for CM in Fig. 1 without peaking for R = 15 kΩ		1.38	2.57

Tab. 4. Comparison of BWER using series-resistor and proposed technique.

5. Conclusion

In this paper, the authors have revealed a new approach of enhancing the bandwidth of a low voltage CMOS current mirror using dynamic body bias technique. The unique feature of this biasing technique is that no additional circuitry is required for bias voltage generation. The proposed approach boosts the bandwidth of the current mirror by a factor of 1.85 and output resistance by factor 1.45 at low supply voltage of 1 volt. The proposed approach does not add any noise owing to higher transconductance of MOS transistor. In emerging CMOS technologies, analog integrated circuits containing passive components are less preferred. It is due to the difficulty faced in fabricating high quality passive devices with tightly-controlled values or a reasonable physical size. This proposed approach reduces the value of series-resistor for achieving same bandwidth performance. This reduction in value of R is very attractive because a smaller resistor results in smaller chip area and less noise. It is pertinent to mention that the dynamic body bias technique virtually has no effects on the overall power consumption of the proposed current mirror and therefore any improvement is not at the expense of increased power consumption. The proposed approach is particularly attractive for low voltage CMOS current mirrors for higher bandwidth performance without degrading overall noise.

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